18 Summary of level-1 trigger latency

Latency is one of the key parameters of the LVL1 trigger that affects the design of all ATLAS front-end systems. Latency is defined (loosely) as the time taken to form and distribute the LVL1 trigger decision, measured from the time of the proton–proton interaction at the centre of the ATLAS detector until the time when L1A trigger signal is received in the detector front-end systems. It determines the required length of the pipeline memories within the front-end systems.

The maximum acceptable latency of the ATLAS LVL1 trigger is specified in a document [18-1] that has been endorsed by the detector system project leaders. All front-end systems must be able to accommodate a latency value of up to 2.5 μs. The latency is measured from the time of collision of the protons (assuming each proton is at the centre of its respective bunch), until the L1A signal is available as an electrical pulse at the output of the TTCrx ASIC (Chapter 16) in the front-end electronics.

Any detector that wishes to have one or more of the following:

- system-specific TTC distribution systems used in addition to the standard TTC backbone;
- non-optimal (from the point of view of latency) rack organization for the TTC crates in the USA15 counting room;
- non-optimal (from the point of view of latency) cable routing between the TTC crates in the USA15 counting room and the front-end electronics;

must be prepared to cope with latency beyond 2.5 μs. This flexibility in the latency requirements specification is necessary to allow each detector the possibility to make an overall optimization of their own sub-system. The target latency for the LVL1 trigger is 2.0 μs, leaving 500 ns as contingency. As discussed in the following, the present best estimate for the LVL1 latency is close to this target.

For the success of ATLAS it is vital that the LVL1 trigger and the detector systems respect the latency requirements that have been specified. A careful study of the LVL1 trigger latency has therefore been performed, as summarized in Table 18-1. Details of the calculations can be found elsewhere in this TDR, in the chapters dealing with the muon trigger, the calorimeter trigger, the CTP and the TTC system. It should be noted that, where necessary in the system, for example at the input to the CTP, signals that arrive relatively early are delayed to bring them into temporal alignment with the corresponding input that arrives last.

Typically, data are transmitted between LVL1 trigger sub-systems serially (or semi-serially) on fast optical or electrical links. The latency for each stage in the processing is calculated from the time when the last bit of serial data is available at the input until the last serial bit is available at the input to the subsequent subsystem. Hence, the latency for each subsystem includes the time required to transmit the data to the subsequent sub-system.

The following elements are included in the latency calculations:

- Time of flight of particles from the interaction point to the detector elements.
- Response time of the detectors and their associated analogue electronics.
- Propagation delays along cables used to transport analogue signals up to and within the detector front-end systems that are mounted on the detector.

Table 18-1 Summary of LVL1 trigger latency in bunch-crossing (BC) units

Item	Contribution to latency (BC)		Comment
Muon trigger	**54.0**		
RPC-specific part		36.0	Including worst-case 80 m fibres to USA15
TGC-specific part		46.0	Including worst-case 80 m fibres to USA15
Interface to CTP		8.0	
Calorimeter trigger	**56.1**		
Signal processing and cables up to input of trigger preprocessor		20.6	Including worst-case 60 m cables to USA15
Preprocessor (e/γ, τ/h)		15.0	
Preprocessor (jet,E_T)		17.0	
Electron/gamma finding		14.0	
Tau/hadron finding		14.0	
Jet finding		18.0	
Missing E_T		18.5	
Total scalar E_T		18.5	
CTP	**4.0**		
TTC	**3.1**		Includes cable from CTP
Fibres to FE electronics	**16.0**		Using worst-case 80 m fibres
TTC receiver (in FE electronics)	**3.0**		
TOTAL	**82.2**		

- In the case of the muon trigger, propagation delays along cables used to transport digital data (patterns of hits) from the detector front-end electronics to the trigger electronics that are mounted on the detector.
- Propagation delays along cables used to transport analogue signals (calorimeter trigger) or digital data (muon trigger) from the on-detector electronics to the USA15 counting room.
- In the case of the calorimeter trigger (liquid-argon calorimeter inputs), delays introduced by detector analogue electronics that receive the trigger-tower signals in USA15, as well as propagation delays for transmitting the signals on to the trigger front-end preprocessor.
- Propagation decays associated with any patch panels required to re-order cable groups for input to the trigger or to facilitate installation and maintenance.
- Time required to perform digitization, where relevant allowing for the need to adjust the clock phase locally in order to sample the analogue pulse optimally (e.g. to sample the peak of calorimeter pulses).

- Propagation delays for digital values along internal cabling, and over backplane and circuit-board connections, within the LVL1 system.
- Delays in the pipelined processing electronics, determined by counting the number of pipeline steps, taking into account the relative phase of the clock signals to different stages in the processing chain.
- Time required to fan out and transmit the L1A signal to the TTC crates associated with the detector sub-systems. This is based on a realistic model for the rack layout of the LVL1 system and the TTC crates that has been optimized to minimize the latency. As discussed above, detector systems may decide to organize their TTC crates differently, at the expense of increased-latency requirements on their front-end systems.
- Delays in the TTC electronic system and the associated electrical-to-optical conversion.
- Propagation delays along the fibres and over other optical elements that connect the TTC crates to the detector front-end systems. The fibre length assumed for the calculation (see Table 18-1) is 80 m, which is a conservative estimate. In the case of the calorimeter electronics, which uses analogue pipelines with critical latency requirements, the fibres could follow the same path as the cables that bring the trigger-tower signals to USA15 (length 60 m or less). The shortest possible fibre path to the inner-detector electronics would be even less (approximately 45 m), but here a different routing will be used in practice.
- As discussed above, detector sub-system groups may decide to route their fibres differently, at the expense of increased-latency requirements on their front-end systems. This will be the case for the inner detector.
- Delays in receiving and making available the L1A signal in the detector front-end electronics, including optical-to-electrical conversion and delay in the TTCrx ASIC (see Chapter 16).

The cable lengths for signal transmission between the detector and USA15 and for the return path have been calculated by the ATLAS Technical Coordination group, taking into account the constraints imposed by installation and access scenarios.

Given the critical importance of the LVL1 latency, a thorough check will be made for the detailed final LVL1 trigger design as part of the Production Readiness Review. Similar checks will be made in the PRRs for the front-end electronics of other ATLAS systems.

18.1 References

18-1 *Trigger and DAQ Interfaces with Front-End Systems: Requirement Document (version 2.0)*, ATLAS note DAQ–NO–103, June 1998.
http://www.cern.ch/Atlas/GROUPS/FRONTEND/FEreq980310.ps