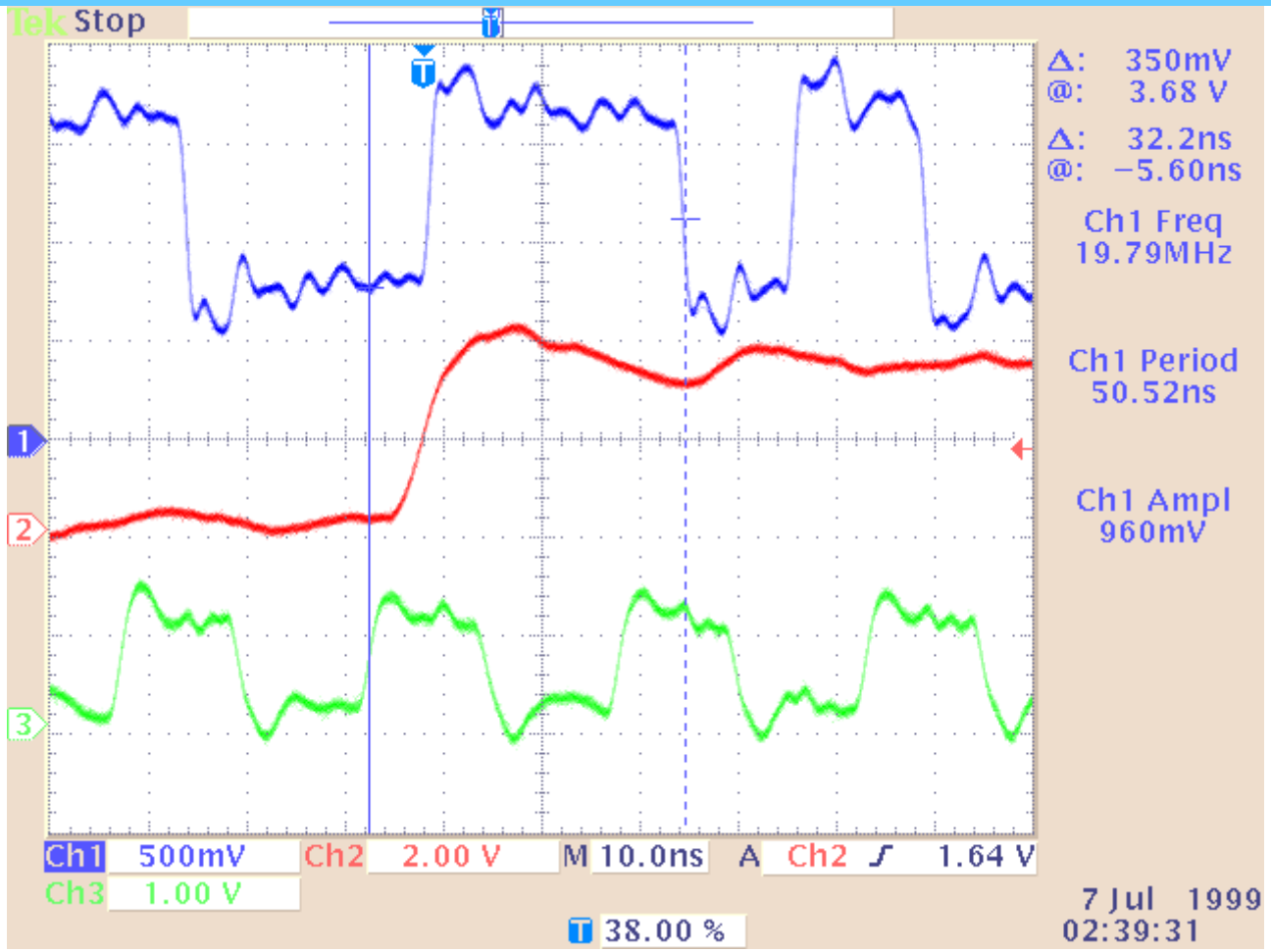
BPM Test Results

Niki Kundu

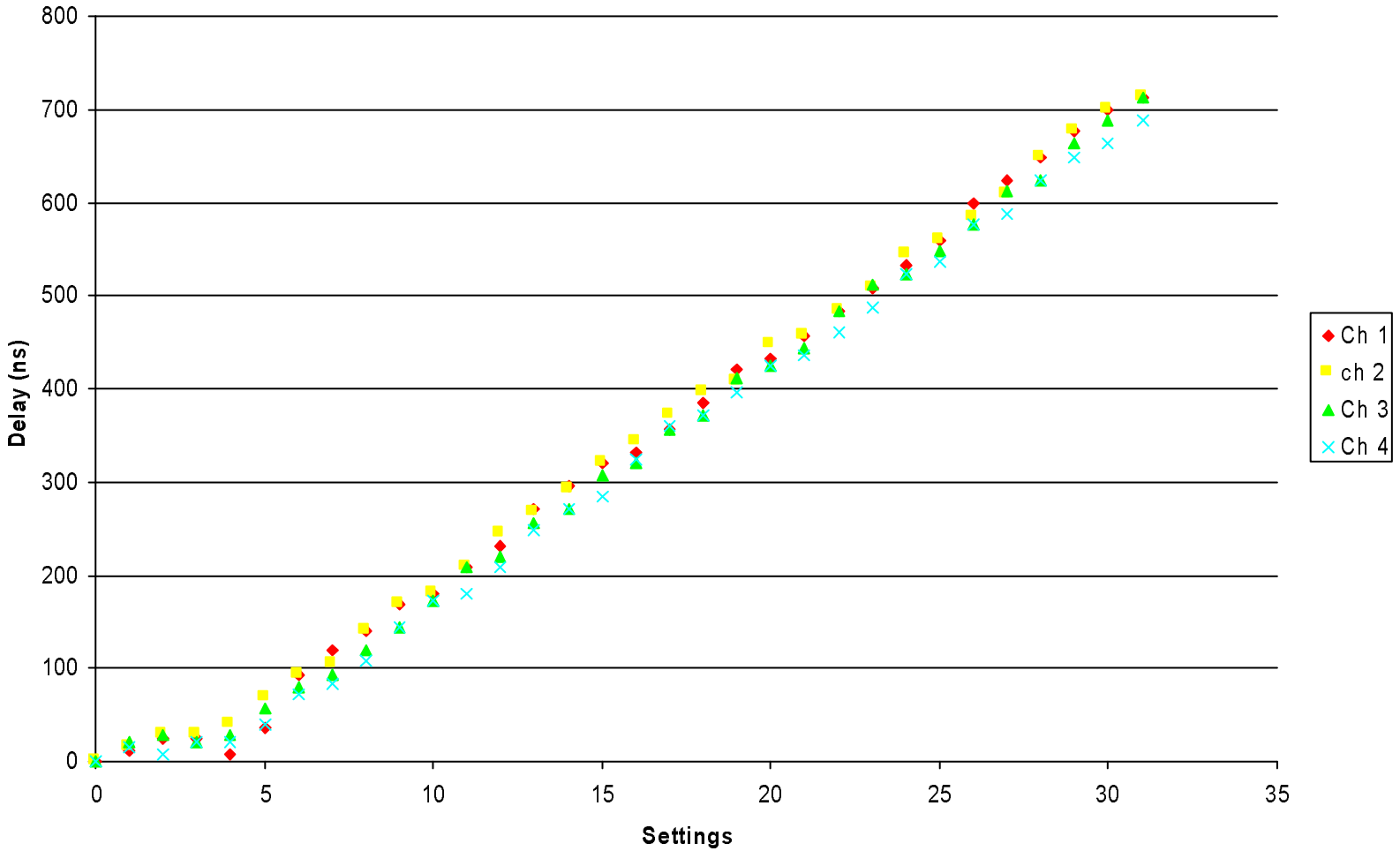
Overview

- Ten Chips tested
- All functionality tested @5v 40Mhz
- Internal test modes.
- Tested with DORIC4

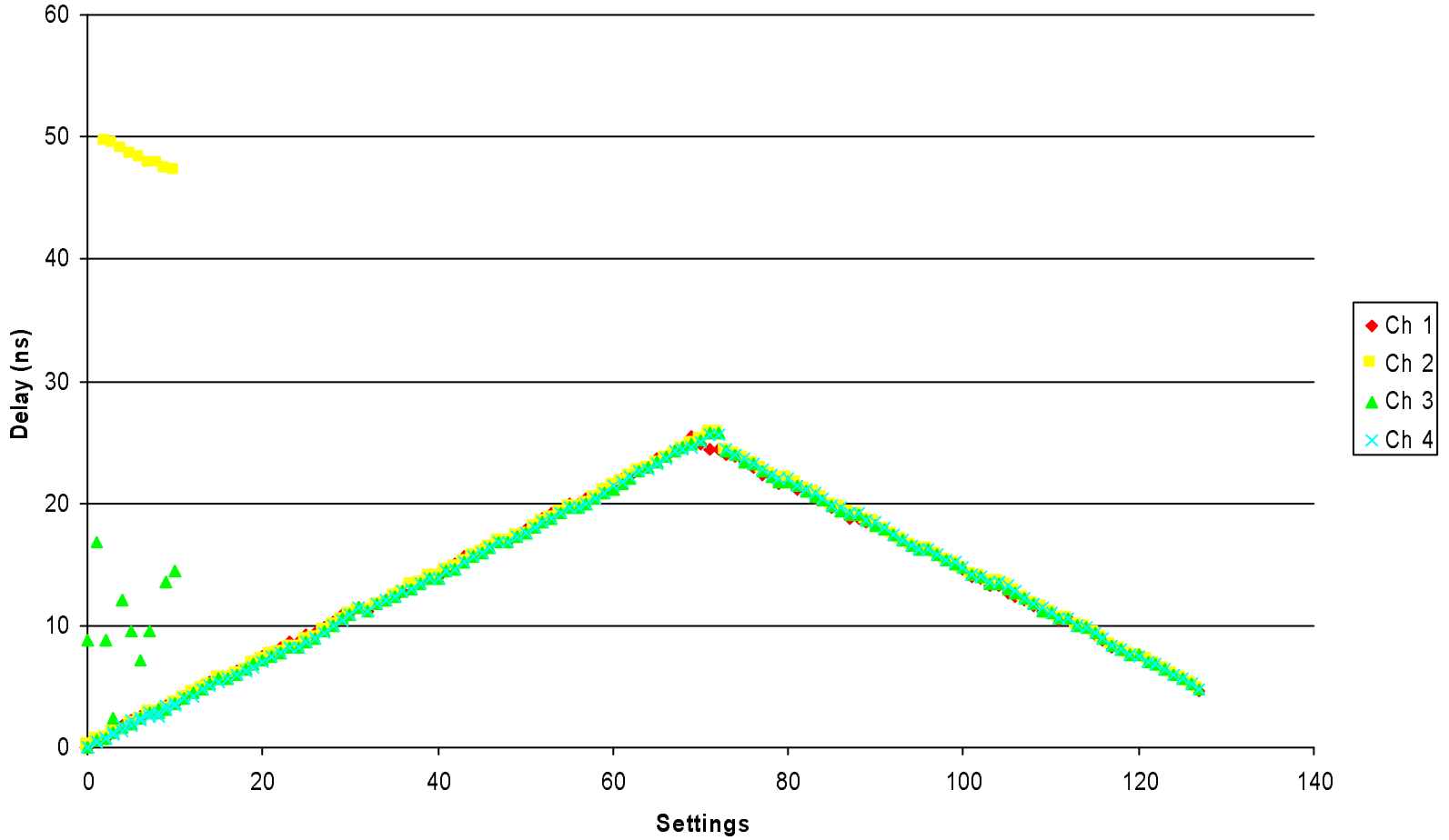
BPM Latency

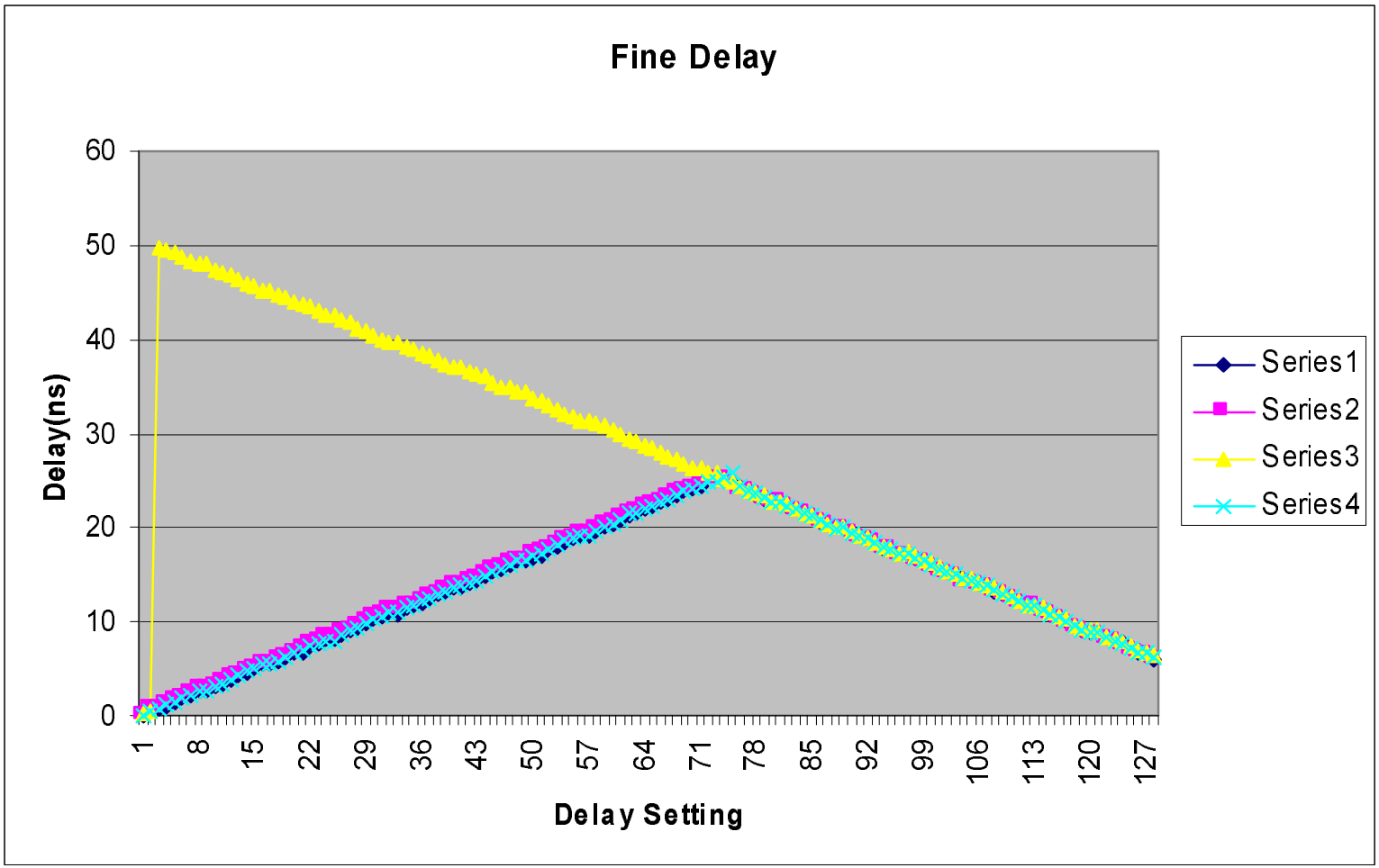

Tek Stop
Δ: 350mV
@: 3.68 V
Δ: 32.2ns
@: −5.60ns
Ch1 Freq
19.79MHz
Ch1 Period
50.52ns
Ch1 Ampl
960mV
1
2
3
Ch1 500mV
Ch2 2.00 V
M 10.0ns
A Ch2 1.64 V
Ch3 1.00 V
38.00 %
7 Jul 1999
02:39:31

Coarse Delay

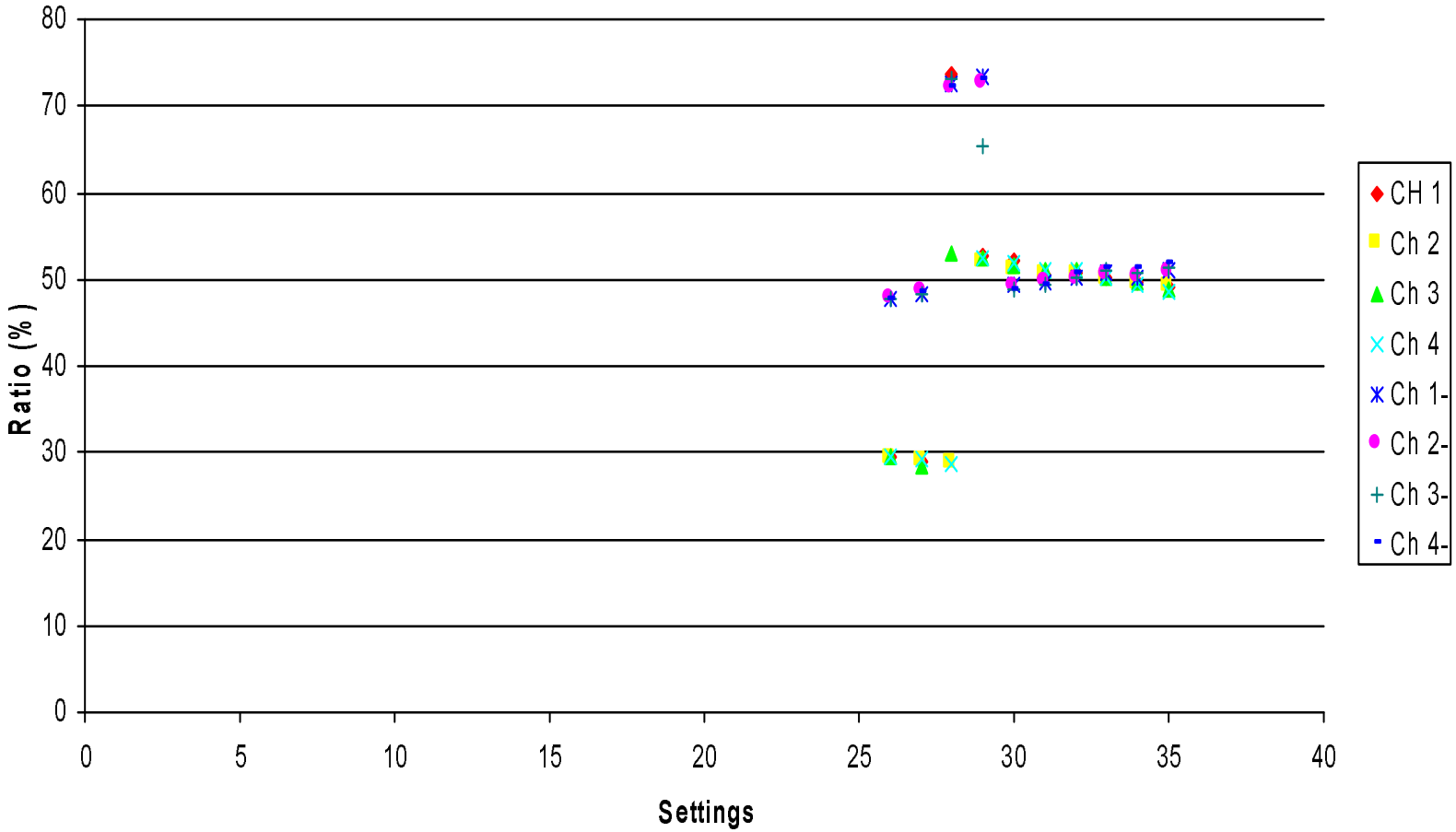


Fine Delay

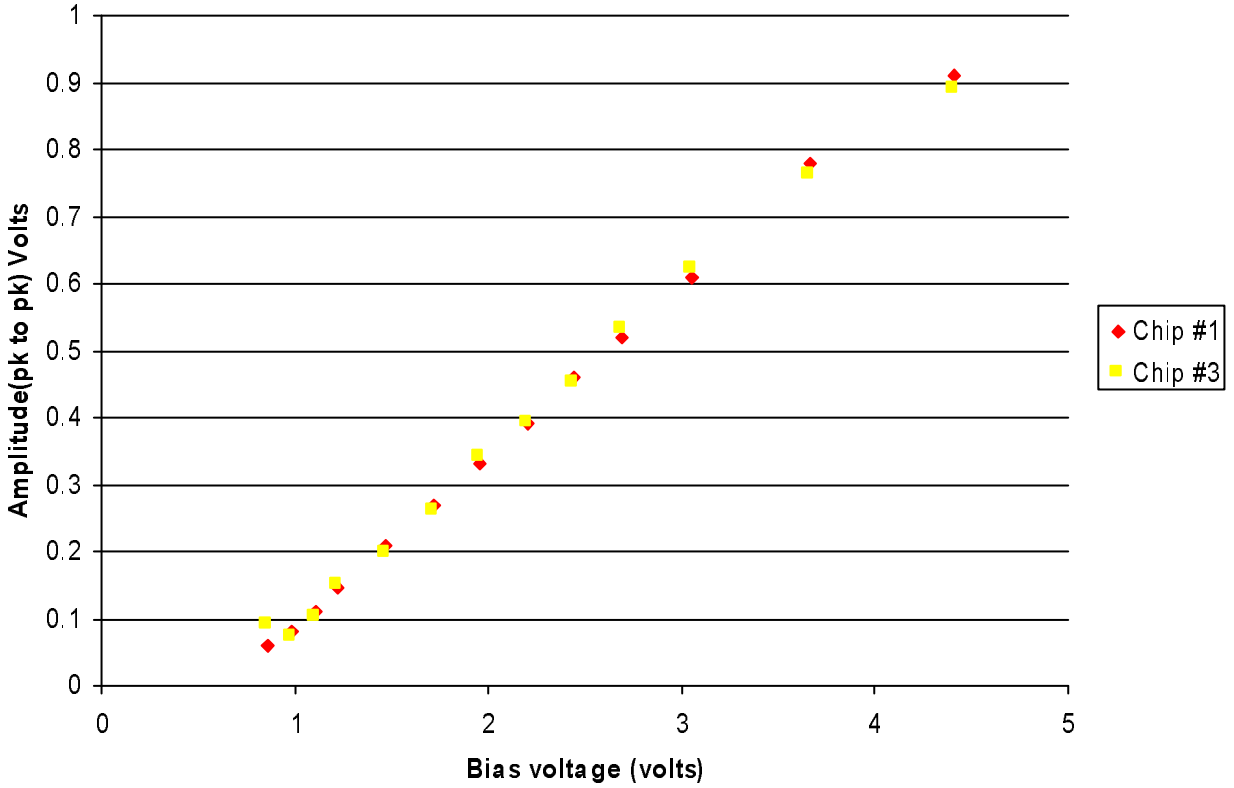

Delay (ns)
60
50
40
30
20
10
0
0
20
40
60
80
100
120
140
Settings
Ch 1
Ch 2
Ch 3
Ch 4


Fine Delay
Delay(ns)
60
50
40
30
20
10
0
1
8
15
22
29
36
43
50
57
64
71
78
85
92
99
106
113
120
127
Delay Setting
Series1
Series2
Series3
Series4

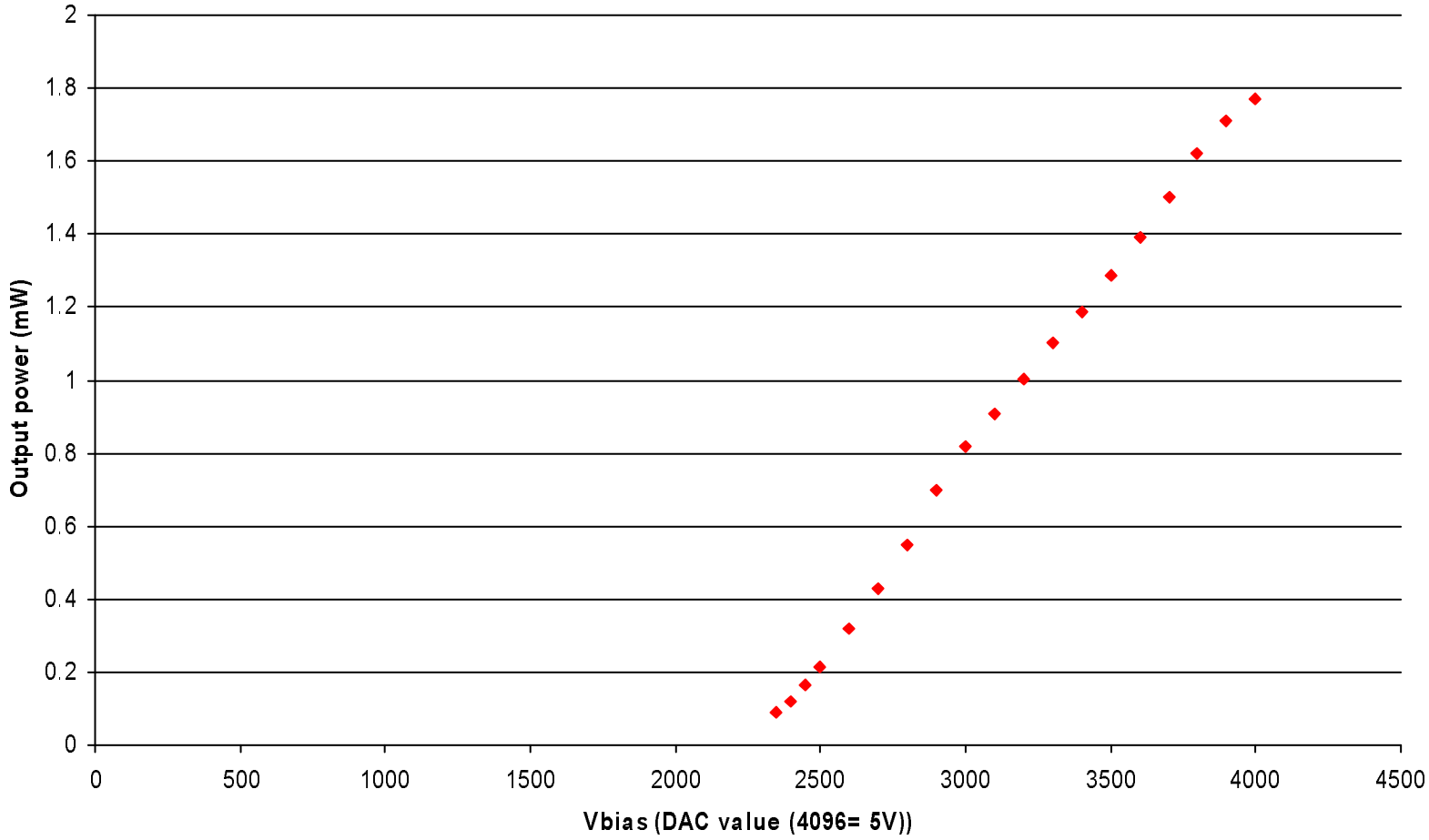
MS ratio


80
70
60
50
40
30
20
10
0
Ratio (%)
0
5
10
15
20
25
30
35
40
Settings
CH 1
Ch 2
Ch 3
Ch 4
Ch 1-
Ch 2-
Ch 3-
Ch 4-

Vbias vs output (Using 27 ohm resistive load)



Laser power output vs vbias



Measured characteristics

- Fine delay step 350ps over 44.45ns
- Course delay 31 whole cycle steps
- Mark/space Ratio 48% to 52%
- BPM Jitter 200ps
- Latency 32ns
- Logic Supply Current @5v ≈130mA 4 channels
- Driver Supply current 180mA 4 channels
- VCSEL drive current up to 32mA
- Power Dissipation in chip 1.3W