Proposed changes in data acquisition for runs in 2001 - 2002 years

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The project described in this paper will allow to rise upper limit on the volume of data accepted by DIRAC data acquisition at least three times. At the same time, this project will allow to do this with minimal changes in currently used data acquisition software and hardware, without revising our data distribution scheme.

Current state (July 2000)

DIRAC data acquisition software[1] was written in 1998 and is used till now without significant changes. It was developed for handling two bursts in the accelerator super-cycle, with up to 2 MB of data in each burst. The main feature of DIRAC DAQ is that all data for one burst are collected in VME buffer memory modules without any software intervention.

However, conditions have been changed significantly since 1998. The most important changes are mentioned below.

- *Changes in beam conditions for DIRAC*

  Starting from June 2000, PS delivers to DIRAC setup 3 bursts per super-cycle during nights and weekends. Three successive accelerator pulses are used for this purpose for keeping similar time structure in bursts. Typical structure of super-cycle as seen by DIRAC setup is shown on figure 1.

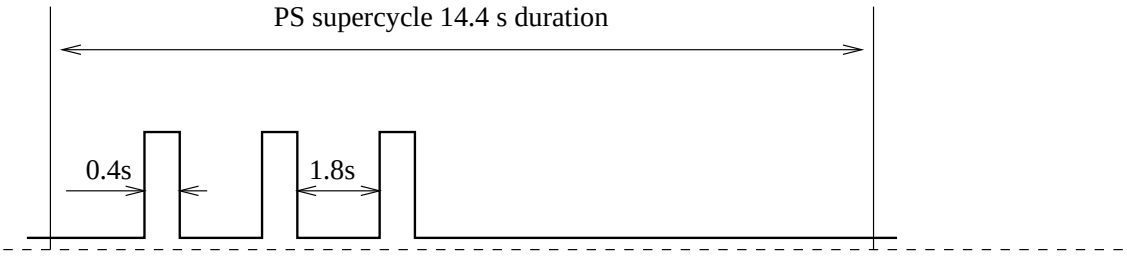

Figure 1: *PS super-cycle as seen by DIRAC setup.*

- *Changes in event size*

  Due to permanent development of the DIRAC setup (adding new data blocks, handling different triggers simultaneously, etc.) the event size

now is about 1.3 KB at beam intensity $10 \cdot 10^{10}$. This is 50 % more than we expected in 1998.

- *Replacement of VME buffer memory modules*

  At the beginning of summer 2000 run we reached saturation of LeCroy VME buffer memories. Since the data for one burst are collected on hardware level, the volume of buffer memories sets an upper limit on the amount of data, which can be collected in one burst. To a moment we replaced 4 of 7 buffer memories (most loaded) with CES modules, which have 8 times more capacity. We plan to replace the rest 3 modules at the beginning of 2001. MSGC (micro-strip gas chambers) VME modules used in our setup, are filled to a moment on 30 % (average), so they also have space for at least triple increasing of data sample.

Due to these reasons, at the beginning of the summer 2000 run we reached the saturation of DIRAC DAQ. The highest data rate at which we still could work was 8 MB/super-cycle.

There are three bottlenecks in current implementation of DAQ, which should be eliminated for further increasing of number of accepted events. They are discussed below, together with proposed solutions.

1. Capacity of VME buffer memories

   As it was mentioned above, this limitation will be eliminated soon after replacing of all VME buffer memories with new ones with higher capacity.

2. Bandwidth of currently used network links

   The current layout of network links in experimental area is shown on figure 2. Two most critical of them are the 10 Mb/s ethernet link between VME processor board and main DAQ host and the 10 Mb/s ethernet link between DIRAC setup and central data recorder (CDR). With current state of setup, the amount of raw data sent via these links is about 7 MB/super-cycle (average, with 3 bursts), or about 0.5 MB/s. The guaranteed speed of data transfer for our dedicated link to CDR is 0.8 MB/s, the practical limit for the link between VME processor and main DAQ host is of the same order. So with these links we can increase the size of our data sample only by 50 %.

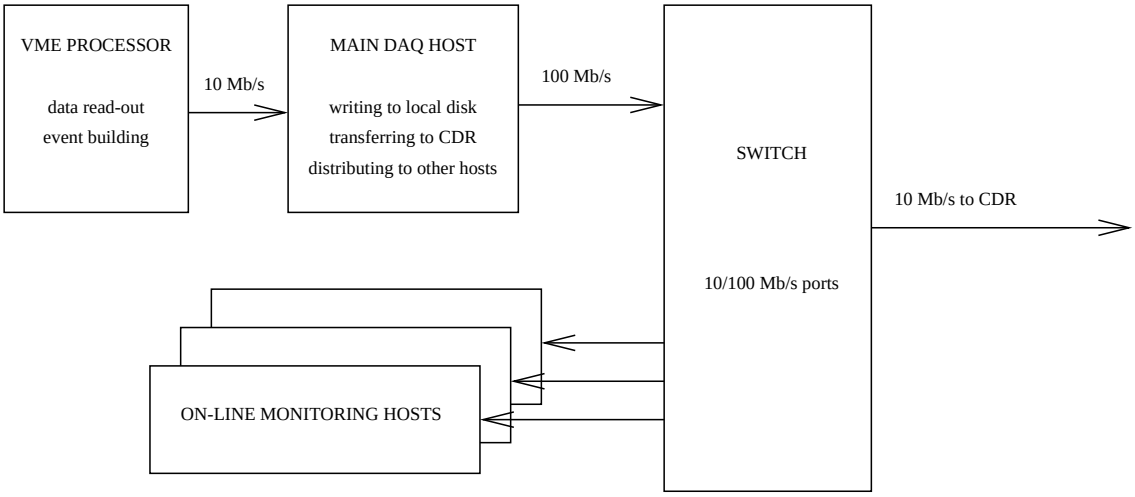

Figure 2: *Current layout.* Two critical ethernet links are the 10 Mb/s link between VME processor and main DAQ host, and the 10 Mb/s link to CDR.

For eliminating this limitation, it is necessary to replace both critical network links used by DIRAC with new 100 Mb/s ones. Also, it is necessary to replace network interface cards in monitoring hosts with 100 Mb/s ones.

3. CPU performance and memory requirements for DAQ computers

   With current implementation of DIRAC DAQ, the VME processor board performs both the readout of data from VME buffers, and the event building. The time interval between successive bursts in one super-cycle is about 2 seconds. This time is insufficient for readout, event building and data transfer to the main host, and therefore data taking program uses queue of buffers for bursts. However, even now the memory overhead for buffering bursts data is significant, and situation will be worth with increasing of the amount of data in burst.

   At the same time, the main DAQ host (Pentium II, 400MHz, 15 SpecInt95) is twice more faster than our VME processor (PowerPC 180 MHz, 7 SpecInt95), and has twice more memory.

   For removing this bottleneck we propose to move layer of event building from VME processor to main DAQ host. This solution not only will reduce the load of VME processor board, but also will give other

benefits:

- Changes in software will not affect data distribution scheme and therefore will be transparent for on-line monitoring programs.
- Personal computers are several times cheaper than VME processor boards with the same performance. If in future we will need more CPU and memory resources for event building and/or on-line analysis of raw data, the upgrade of hardware will be less expensive.
- With current DAQ software, event building is performed by data taking program running on the VME processor, so we are limited with only one data source - the VME crate. After moving the layer of event building to the main DAQ host, it will be possible to implement reading of data from several data sources with minimal changes in the overall scheme of DAQ software. Due to this, the proposed solution will leave more space for possible further improvements of DIRAC DAQ.

The schematic layout of the proposed new scheme for data acquisition is shown on figure 3.

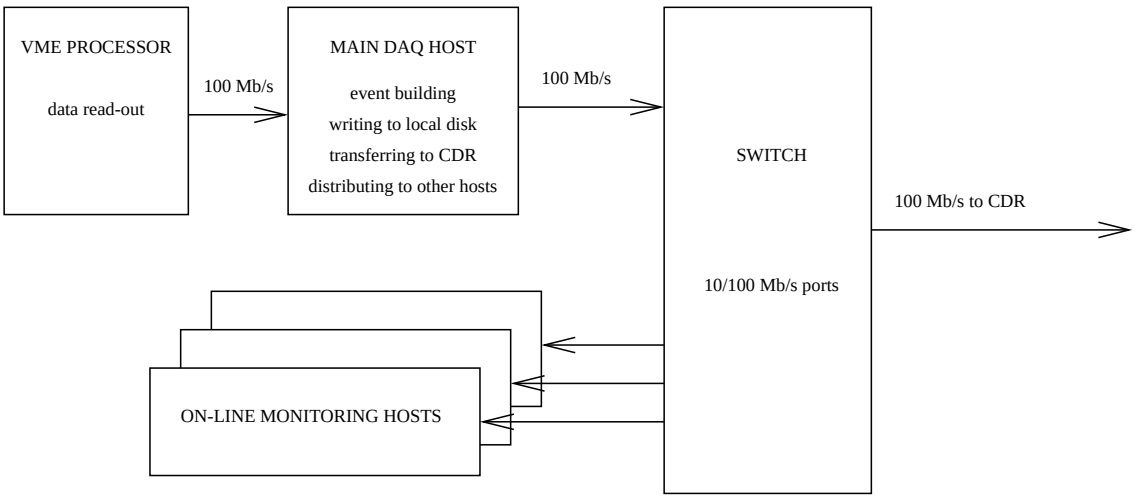

Figure 3: *New layout.* Critical ethernet links changed with 100 Mb/s ones. Layer of event building moved to main DAQ host.

It is possible to make described above changes in software before the beginning of 2001 runs during already planned visits of DAQ group members. The replacement of hardware (network links, interface cards and so on) can be done independently of software changes without affecting functionality of data acquisition.

References

[1] Olshevsky V.G., Trusov S.V. JINR E10-2000-150, Dubna, 2000.