RNA trigger simulation

A. Benelli L. Tauscher

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The aim of this work is to present the RNA software simulation and it's effect on the data analysis.

1 RNA trigger

The RNA trigger has been implemented in the trigger hardware since the 2001 data taking. Since run number 3865 RNA has been active in OR with the DNA trigger [M. Jabitzki - e-mail].

Its design followed the idea of the DNA trigger. In the latter the Ionisation Hodoscope was used to position the pions, in the RNA the Scintillator Fibre were used.

The input for the RNA trigger were SFD Vertical plane, Vertical Hodoscope Right and Left. The hit slabs from these detectors were send to a Neural Network box, which provides an output that is subsequently transformed in a trigger decision. All these informations may be found in : The Revised Neural Atomic trigger, 21/09/00 by S.Vlachos.

1.1 A little about the RNA

The most elaborate part in the RNA trigger simulation is the preparation of the hits to be sent to the NN algorithm RNA front-end. Thus we spend some time on this issue.

1.1.1 T0

In order to start the RNA front-end reading of the SFD information the T0 signal was used, like for the DNA. In contrast the T1 was used to latch the SFD signal in the TDCs. [A. Kulikov e-mail]. This may lead to differences when comparing trigger decision and SFD information (TDCs) in the offline.

1.1.2 SFD

All the information described here has been kindly given by M. Steinacher via e-mail and papers, see appendix.

The SFD vertical (X) has 240 column of fibres to be read out. Since the read-out cards could store only 64 bit, 4 cards (FDR CARDS) were used. FDR-Card number 1 contains the information about the first 64 column, the 2nd cards contains the information from the 65th column to the 128th, and so on. Later I will refer to "hit" as a column of the SFD that has been fired.

The number of hits in each of these FDR Cards are counted. In order to find the closest pair of hits additional C-Cards were installed after the FDR-Cards. In the first C-Card were stored the first 64 columns of the first FDR-card plus the first 16 columns of the second FDR card. The second C-Card was storing column 65 to 128+16, in this

way we always have an overlap of two neighboring FDR cards to calculate the minimum distance between columns, without risking to loose information.

After this two layers of Cards we have for each Cards the following information :

- Number of hits.
- Minimum distance of two hits.

Particular cases are issued when there are:

- 1) no hits present in the card (Empty Flag)
- 2) more than 5 hits (Overflow Flag)
- 3) the minimal distance between hits is greater than 15 columns.

1.1.3 VH

For each VH detector (Left or Right) the slabs hit are collected. The information is kept if there are 1 or 2 slabs for each arm. Otherwise a special flag is set (overflow or empty).

1.2 Decision

The RNA decision was considered positive if :

- There was one overflow signal (OR between the VH Left - VH Right and SFD) That means more than 2 hits in VHR or VHL or more than 5 hits in SFD (sum of the 4 FDR Cards).
- The NN decision is positive. The input is : two SFD hits and one VHR and one VHL. In case there are more hits then all the combination are taken into account between the two SFD hits and the VH L and R.

The decision was considered negative if :

- There was an empty flag (Or of the SFD VHL and VHR).
- DEB15 Flag. This happens when the minimum distance found on ALL four C-Crads has a separation of 15 column at least.
- SHOM flag. Single Hit On Multiple C-Cards is activated if a single hit (distance 0) is detected in two or more C-Cards. If it is detected in only one Ccard, then the same hit is sent twice to the NN algorithm.

1.3 Possible error / malfunctioning

1.3.1 T0 and gate

The SFD is read out for the offline with a TDC signal while for the trigger the SFD is started by the ADC signal (TmTrigToADC). In Ariane, after the 2001 data taking the two signals coincide, but for the 2001 they are different. The literature recommends to use TmTrigToADC. As a test the TDC signals (TmTriggHodDC) were used, and not significant difference was found.

A gate of 40 ns is opened in order to read out the SFD columns, but the starting point of this 40ns is tuned by hand and nowhere written, and could vary inside an interval of 60ns. Thus this could introduce a different number of hits seen by the trigger as compared to the offline. The opening of the gate was fixed at hoc at 0, and closed at 40 ns. Thus a hit is seen by the trigger if $0 < (TmTrigToADC - TimeHitScifi) < 40ns$.

1.3.2 MASTER card

The logic of the trigger and all the possible cases are stored in the Master cards, no documents are available on how to read it again, and how exactly it was functioning.

1.3.3 The NN code

One version of the Neural Network code has been found by S. Vlachos (private communication) but he could not remember wether this was the one used for the training of the actual trigger in 2001.

2 Comparison with Data

- Data selection.

  In order to evaluate the RNA simulation of the trigger, real data were selected when the RNA trigger was not in the decision of the trigger but the flag for it was in the hardware (T0+T4 data in 2003). Then on this data the RNA trigger simulation was applied. The simulation takes as input the offline values of the variables, since the real hardware input is not stored in the data. The hardware decision was compared with the simulation decision and the number of coincidence counted. The events have to satisfy the Vertex Fit Tracking conditions using the DownStream and UpStream detectors.

- Comparison of hardware - software for RNA.

  Of a total of 840198 events, 235059 events were reconstructed with the Vertex Fit Stream. Table 1 shows the result with the vertex Fit conditions. The RNA is apparently less well simulated than DNA. The main cause of the RNA simulation

	Software = 1 Hardware = 0	Software = 0 Hardware = 1
DNA alone	5.6 % (13215)	2.4 % (5596)
RNA alone	12.9 % (30289)	7.3 % (17289)

Table 1: Inefficiency of the DNA and RNA trigger simulations.

  failure (in 19291 events out of 30289) is due to cases of too many hits seen by the simulation and not by the hardware trigger. In this particular case the software would give a positive decision while for the hardware it is negative. The cause could be multiple, an error in the choice of the gate for the aquisition of the hits in SFD, something missing in the Mother Card, or just a different limit in the overflow Flag, ie. more hits were allowed in the hardware.

- Comparison of hardware - software for DNA or RNA

  Things are going much better for the OR of the simulations for DNA and RNA, that was actually used in the running.

RNA OR DNA	Vertex tracking	Down Stream tracking
all Q_l and all Q_x and Q_y	93.4 %	93.4 %
$Q_l < 22Mev$ and $abs(Q_x) < 10Mev$	99.7 %	99.6 %
$Q_l < 15Mev$ and $abs(Q_x) < 4Mev$ and $abs(Q_y) < 4Mev$	99.7 %	99.5 %

Table 2: Efficiency of the DNA OR RNA trigger simulations.

For this test the Vertex tracking and the DownStream tracking were compared, see Table 2. The result are very similar.

2.1 Effect of RNA simulation on the MC data.

Sofar, in the analysis of the 2001 data only DNA was simulated in the MonteCarlos. Doing this we have lost some events and they show a Q_l dependence, similar for Q, of less than 0.3% for Q,$|Q_l| \leq 15$ MeV, figure 1. This difference leads to a 0.5% more CC-background than with DNA simulation alone.

If we compare the MC events where the trigger simulations of T0 and T4 alone have been applied with the full trigger: T0 + T4 + (RNA or DNA) we obtain figure 2. We conclude that DNA.or.RNA introduce a slight Q/Q_l dependance of less than 0.1% for Q,$|Q_l| \leq 15$ MeV.

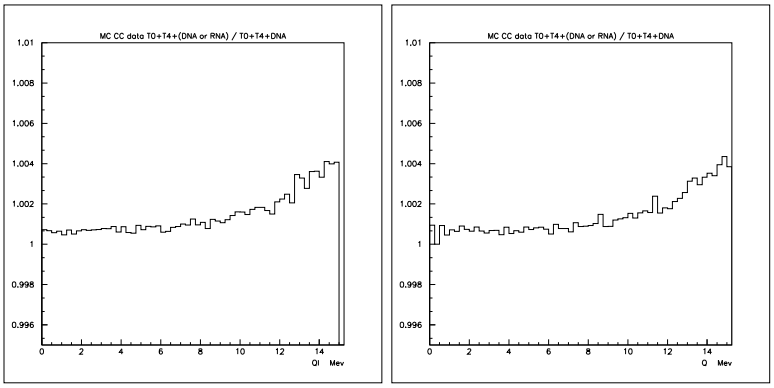


Figure 1: Coulumb Correlated MonteCarlo events. Ratio of events selected with the T0+T4+(DNA or RNA) / T0+T4+DNA as function of Q_l and Q.

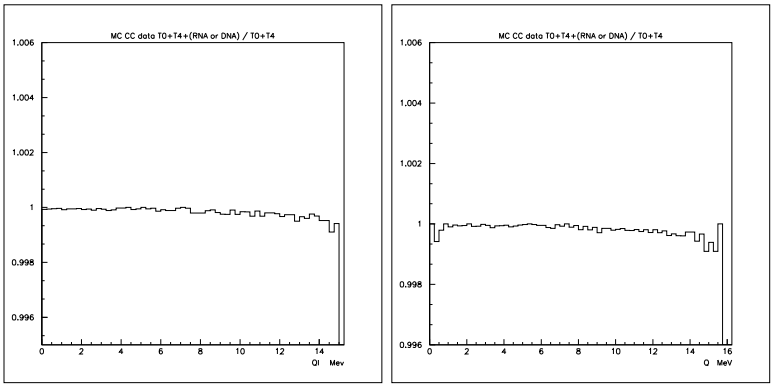


Figure 2: Coulumb Correlated MonteCarlo events. Ratio of events selected with the T0+T4+(DNA or RNA) / T0+T4 as function of Q_l and Q.

3 Documentation

- Jabitzki e-mail of the: Mon, 14 Nov 2005 18:22:53

  Dear Colleagues,

  After our last meeting the check of data-taking periods in 2001 with different triggers was performed. To find out active triggers content of trigger TDC3377 was checked with 2 different maskes:

  - trigger itself
  - trigger !(ee—Lambda—Kaon—DNA(OR)—DNA1—DNA2) = trigger !0x604a4

  The last combination reveals whether some trigger in OR mode with DNA was active. The found periods were found to be consistent with 2001.run.logbook:

  - T1pipicopl (T3—DNA) T4 ...-3477]
  - T1pipicopl T4 [3480-3862]
  - T1pipicopl (RNA—DNA) T4 [3865-...

  Have a good day, Mikhail

- E-mail from Kulikov

  Date: Fri, 18 Nov 2005 16:03:27 +0300 (MSK) From: Kulikov ¡kulikov@nusun.jinr.ru¿ To: Angela Benelli ¡benelli@mail.cern.ch¿ Subject: Re: Rna

  Dear Angela, In order to latch the SFD signals in TDC we used T1. But to RNA system the SFD signals come independently. I suppose that for the RNA gating the same T0 was used like for DNA. The needed cabling for RNA was done not by me but by somebody else, most probably by Sotiris.

  Regards, Anatoly

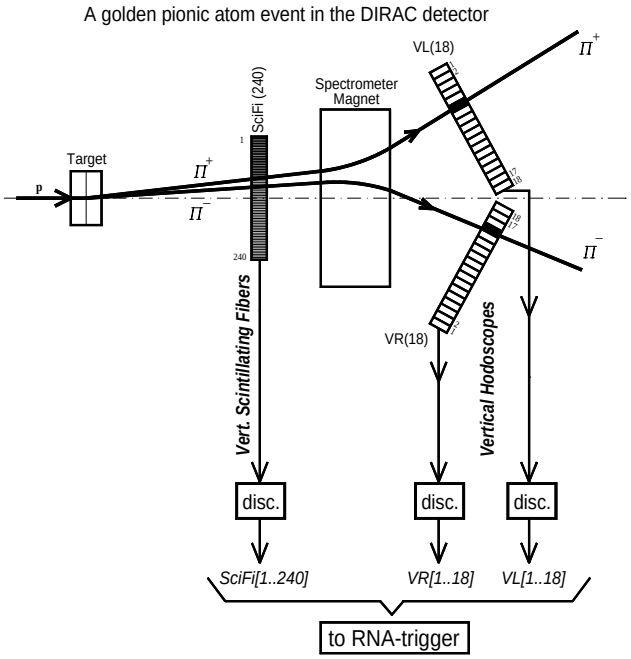
DIRAC RNA-Trigger
Hardware Overview

Revision 1.3

Physics Basel, 14. December 2000, M. Steinacher

1. Introduction:

This paper gives an overview of the hardware needed for the *Revised Neural Atomic* trigger (*RNA*-trigger) at the *DIRAC* experiment (*CERN / PS212*). This trigger works similar to the already installed *DIRAC Neural Atomic* trigger (*DNA*-trigger); instead of the 16 channel *Ionizing Hodoscope* the 240 channel *Vertical Scintillating Fibers* (*SciFi[1..240]*) are used to locate the pion-pair in front of the *Spectrometer Magnet*. After the *Spectrometer Magnet* the hit-maps of the two 18 channels *Vertical Hodoscopes Left* (*VL[1..8]*) and *Right* (*VR[1..18]*) are used to track the two pions. The analog detector signals are digitized with discriminators and preprocessed by the *Preformat & Decision Electronics* (*PDE*) before the appropriate *NN*-patterns are transferred to the four *NN-CARDs* (built for the *CP-LEAR* experiment / CERN / *PS195*). The four *NN*-decisions are wired to the *PDE* where the final *RNA*-decision is made. To reach a *RNA*-decision time of only several hundred nanoseconds, the whole *PDE* must be realized with fast digital electronics. The *PDE* as well as the *NN-CARDs* are located in the *RNA-CRATE* and they are loaded and controlled via the *J1-VMEbus*. *Figure 1* shows the origin of the *DIRAC* detector-signals used for the *RNA* trigger.



For an introduction to the *RNA*-trigger see the paper *'The Revised Neural Atomic trigger'*, S.Vlachos, Basel, 21. September 2000.

The already installed *DNA*-trigger is documented in the following papers:

- *'The Dirac Neural Atomic trigger'*, S. Vlachos, Basel, 18. November 1998.
- *'Interface & Decision CARD'*, M. Steinacher, Basel, 9. August 1999.
- *'The neural network first-level trigger for the DIRAC experiment'*, P. Kokkas et al., will be published in Nucl. Instr. and Meth. A

Figure 1 ***DIRAC detectors used for the RNA trigger:*** *The analog signals from the Scintillating Fibers (SciFi[1..240]) and the Vertical Hodoscopes Left and Right (VL[1..18], VR[1..18]) are discriminated and the digital signals are connected to the RNA-trigger.*

2. Layout:

The *RNA*-trigger hardware can be subdivided into two main parts: The *Preformat & Decision Electronics (PDE)* and the *Neural Network (NN)*. The description of the *NN*-electronics is not part of this article; it can be found in the following papers: 1) *'NN-CARD DESIGN'*, M. Steinacher, Basel, 11. September 1992. 2) *'NN-CARD PROTOTYPE'*, M. Steinacher, Basel, 27. September 1993.

The *PDE* converts each of the three detector hit-maps [*SciFi(240), VL(18), VR(18)*] into two binary numbers, representing the position of the hits. The two positions extracted from the 240 channel *SciFi* are coded in two 8 bit numbers [*SciFi_POS1/2(16)*] representing the two closest hits. The two positions of the 18 channel *VL* are coded in two 5 bit numbers [*VL_POS1(5), VL_POS2(5)*] and the same scheme is also used for *VR* [*VR_POS1(5), VR_POS2(5)*]. These six binary number are combined to build the four different *NN*-patterns. Each of the *NN*-patterns holds the two *SciFi* positions and a combination of one *VL*-and one *VR*-positions. This results in four different 26 bit wide *NN*-patterns. All *NN-CARDs* are loaded with the same weights, optimized to distinguish from a good and bad event. Further the *PDE* forms the final *RNA*-decision (*RNA_DEC*), manages the correct internal timing of the *RNA*-trigger sequence (*SciFi_GATE, NN_CLK, V_CLK)* and the communication with the 'DIRAC Trigger Control' via the following signals: *T0_START, BUSY, VETO, RNA-DEC* and *STRB.*

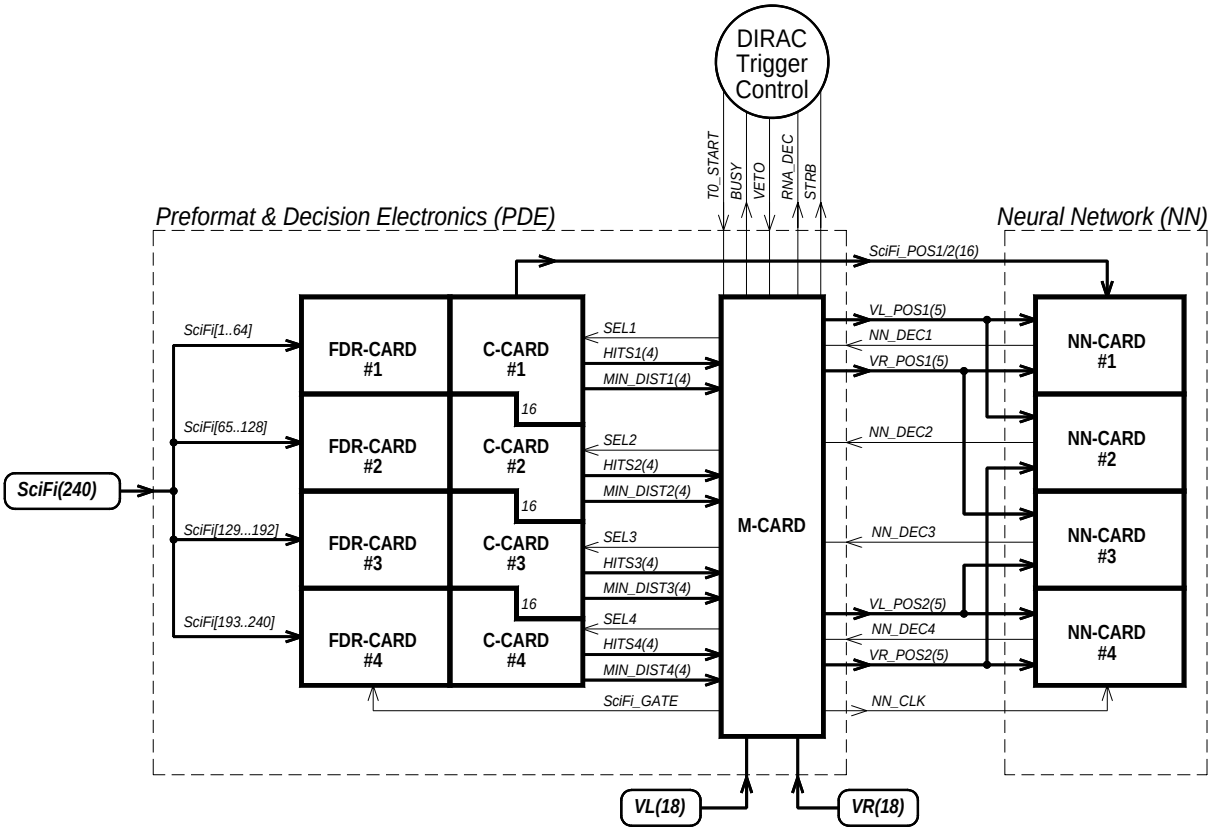


Figure 2 ***The Layout of the RNA hardware:*** *The main block is the PDE part, which converts the detector hit-maps into four different NN-patterns. It also manages the correct internal timing as well as the communication with the 'DIRAC Trigger Control'. The NN is trained to be selective between good and bad events.*

The *PDE* itself consists of total nine *VME*-cards (4 *FDR-CARDs*, 4 *C-CARDs*, 1 *M-CARD*) from three different types with the following functionality:

2.1 Fanout / Delay / Register Card (FDR-CARD):

The name *Fanout / Delay / Register Card* already implies its functionality: First the *FDR-CARD* receives/fanout the *SciFi*-signals arriving in *differential ECL* (*dECL*) level on the frontpanel. Since the *SciFi*-signals are not only used for the *RNA*-trigger, the fanout is necessary.

Then the received *SciFi*-signals are delayed by an adjustable amount of time (around 150..200ns). This is inevitable because the *SciFi*-signals are valid prior the lowest level trigger (*T0_START*) of the DIRAC experiment. The adjustable delay step-size can be around 5..10ns because the *SciFi_GATE*, coming from the *M-CARD*, can be adjusted with a resolution of 0.5ns (via the *VMEbus*) with respect to *T0_START*.

Finally the *FDR-CARD* registers the delayed *SciFi*-signals during the *SciFi_GATE* (*dECL*) is active. This is needed due to the fact that the *SciFi*-signals arrive in a time-window of about 40ns. The *SciFi_GATE* signal is generated on the *M-CARD* and it is connected to the *FDR-CARDs* via the frontpanel. Since the same *SciFi_GATE* signal is used on all of the four *FDR-CARDs*, it is necessary that the 110Ω termination resistors can be removed; the *SciFi_GATE* signal is daisy-chained from *FDR-CARD #4..#1* and it is terminated on the last *FDR-CARD #1*.

The entire 240 *SciFi*-signals are covered by four identical *FDR-CARDs*. One *FDR-CARD* is able to handle 64 *SciFi* inputs connected via the frontpanel. Since the *FDR-CARD #4* uses only 48 inputs out of the 64 inputs, the *SciFi* inputs which are left open should be defined low.

The *TTL* level outputs of the *FDR-CARDs* are connected via the *J2*-connector (96 pin, DIN41612) to the dedicated *RNA*-backplane where they are distributed to the *C-CARDs*. The outputs of the *FDR-CARDs* are able to drive termination on the *C-CARDs* of 180Ω to *+5V* and 330Ω to *GND*. Since the first 16 *SciFi*-signals are wired to two different *C-CARDs* these outputs are duplicated and buffered separately. Therefore 80 pins out of the 96 pins on the *J2*-connector are used; the remainder are connected to *GND*.

2.3 Concentrator Card (C-CARD):

Each *Concentrator Card* (*C-CARD*) processes in parallel 80 registered *TTL SciFi*-signals from two adjacent *FDR-CARDs*. To get a continuos and constant detection performance over the whole width of all 240 *SciFi* channels, an overlap of 16 channels between two adjacent *C-CARDs* is implemented. The *C-CARD #1* processes the 64 registered *TTL SciFi*-signals from the *FDR-CARD #1* and the lowest 16 registered *TTL SciFi*-signals from *FDR-CARD #2*. The same scheme is also used for the *C-CARD #2* and *#3*; the *C-CARD #4* treats only the 48 registered *TTL SciFi*-signals from *FDR-CARD #4*. Nevertheless all *C-CARDs* are completely identical.

The three main tasks of the *C-CARD* are:

- Find in the 80 bit hit-map the two hits which has the smallest distance (closest together). Send the detected minimum distance [*MIN_DIST(4)*] via *dECL* signals on the frontpanel to the *M-CARD*. If a single hit is detected set the minimum distance to zero. Two adjacent hits correspond to a minimum distance of one. Up to a distance of 14 the algorithm is linear. The minimum distance of 15 indicates that the distance is equal or bigger than 15 or no hit is detected in the 80 bit hit-map.

- Count the number of hits in the lower 64 bit of the hit-map; this restriction makes sure that each hit is counted only once. Send the number of hits [*HITS(4)*] via *dECL* signals on the frontpanel to the *M-CARD*. If more than 15 hits are counted, it saturates at 15.

- If the *C-CARD* is selected, the two absolute positions (each 8 bit) of the two closest hits are presented on the tri-state bus [*SciFi-POS1/2(16)*]. If there was only a single hit, two times the same position is presented. The absolute positions of the hits are calculate by using the *VME* address of the selected *C-CARD*. The select signals [*SEL1..4, dECL*] are generated on the *M-CARD* and they are connected to the *C-CARDs* via the frontpanels. The outputs of the *C-CARD* are able to drive terminations on the *NN-CARDs* of 180Ω to +5V and 330Ω to GND.

The distribution of the registered *TTL SciFi*-signals from the *FDR-CARDs* to the *C-CARDs* and the interconnection of the tri-state *TTL* bus [*SciFi-POS1/2(16)*] to the *NN-CARDs* are realized on the *RNA*-backplane. All the 96 pins of the *J2*-connector are used for the signal interconnection [input: *TTL SciFi*-signals(80), output: *SciFi-POS1/2(16)*].

2.3 Master Card (M-CARD):

The *Master Card* (*M-CARD*) receives and processes the information from the four *C-CARDs*. All the signals from the *C-CARDs* are transmitted to the *M-CARD* in *dECL* format and are connected via the frontpanel. The *M-CARD* selects the *C-CARD* which has sent the smallest minimum distance [*MIN_DIST1..4(4)*]. This selection is accomplished by the outputs *SEL1..4* (*dECL*) on the frontpanel of the *M-CARD*. If two or more *C-CARDs* send the same minimum distance the first *C-CARD* in the order #1, #2, #3, #4 is selected. Out of the four number of hits [*HITS1..4(4)*] the *Total Number of Hits* (*TNH*) in the *SciFi* detector can be calculated. If *TNH* is zero (no hit) the *SciFi_EMPTY* is activated; if *TNH* is bigger than 5 the *SciFi_OVR* is activated. A smallest minimum distance of 15 and the *SciFi_EMPTY* not activated, indicates one or more hit-pairs with a *Distance Equal or Bigger than 15* (*DEB15*). By combining the four minimum distances [*MIN_DIST1..4(4)*] and the four number of hits [*HITS1..4(4)*], *Single Hits 0n Multiple* (*SHOM*) *C-CARDs* can be detected. The four facts *SciFi_EMPTY*, *SciFi_OVR*, *DEB15* and *SHOM* are needed for the final *RNA*-decision.

The *M-CARD* processes also the two detector hit-maps *VL(18)* and *VR(18)*. The *dECL* signals are connected to the *M-CARD* via the frontpanel; the 110Ω termination resistors can be removed and the signals can be daisy-chained to the already installed *DNA*-trigger. The *M-CARD* registers the *VL* and *VR* hit-maps on the rising edge of the *V_CLK* signal which is adjustable with a resolution of 0.5ns (via *VMEbus*) with respect to *T0_START*. For each side of the *Vertical Hodoscope*, up to two hits can be processed. The *M-CARD* determines, separately for *VL* and *VR*, the position of the hit(s) and they are coded in four 5 bit values [*VL_POS1(5)*, *VL_POS2(5)*, *VR_POS1(5)*, *VR_POS2(5)*]. If only one hit is registered two times the same position is readout. Further the *VL_EMPTY*, *VR_EMPTY* (no hit) and *VL_OVR*, *VR_OVR* (more than 2 hits) are build to perform the final *RNA*-decision. The four positions of the *Vertical Hodoscope* are distributed to the *NN-CARDs* via the *J2*-connector and the *RNA*-backplane. Because each of the position is used on two different *NN-CARDs* they are duplicated and buffered separately. The outputs are able to drive terminations on the *NN-CARDs* of 180Ω to +5V and 330Ω to GND. The *NN_CLK* signals [*NN_CLK1..4*] are buffered for each *NN-CARD* separately and are able to drive terminations of 82Ω to +5V and 120Ω to GND. Therefore 44 pins out of the 96 pins on the *J2*-connector are used; the remainder are connected to *GND*.

The signal *T0_START* (*dECL*) is connected via the frontpanel and starts the programmable sequencer which steers the timing of the *RNA*-trigger sequence. An active *VETO* input signal (*dECL*) prevents the *RNA*-trigger from processing new events. The timing of the *RNA*-trigger is controlled by the signals *Sci_Fi_GATE*, *V_CLK*, *NN_CLK* and *STRB*. During the *RNA*-trigger is running the signal *BUSY* (*dECL*) on the frontpanel of the *M-CARD* is activated.

The four *NN*-decisions [*NN_DEC1..4, dECL*] are connected to the *M-CARD* via the frontpanel. The final *RNA*-decision is a *dECL* signal available on the frontpanel of the *M-CARD* and a 20ns *STRB* signal (*dECL*) indicates that the *RNA*-decision is valid. The final *RNA*-decision is carried out on the *M-CARD* using the following algorithm:

EMPTY = *SciFi_EMPTY* **or** *VL_EMPTY* **or** *VR_EMPTY*
SPREAD = *DEB15* **or** *SHOM*
OVR = *SciFi_OVR* **or** *VL_OVR* **or** *VR_OVR*
NN_OR = *NN_DEC1* **or** *NN_DEC2* **or** *NN_DEC3* **or** *NN_DEC4*

RNA_DEC = OVR or (NN_OR and not EMPTY and not SPREAD)

3. Signal Interconnections:

Figure 3 shows the signal interconnection diagram of the *RNA*-trigger. The most connections between the 13 cards are realized on the dedicated *RNA*-backplane with single ended *TTL* signals. The *dECL* detector signals are connected via the frontpanels of the *FDR-CARDs* and *M-CARD*. For daisy-chain purpose all *dECL* 110Ω termination resistors can be removed.

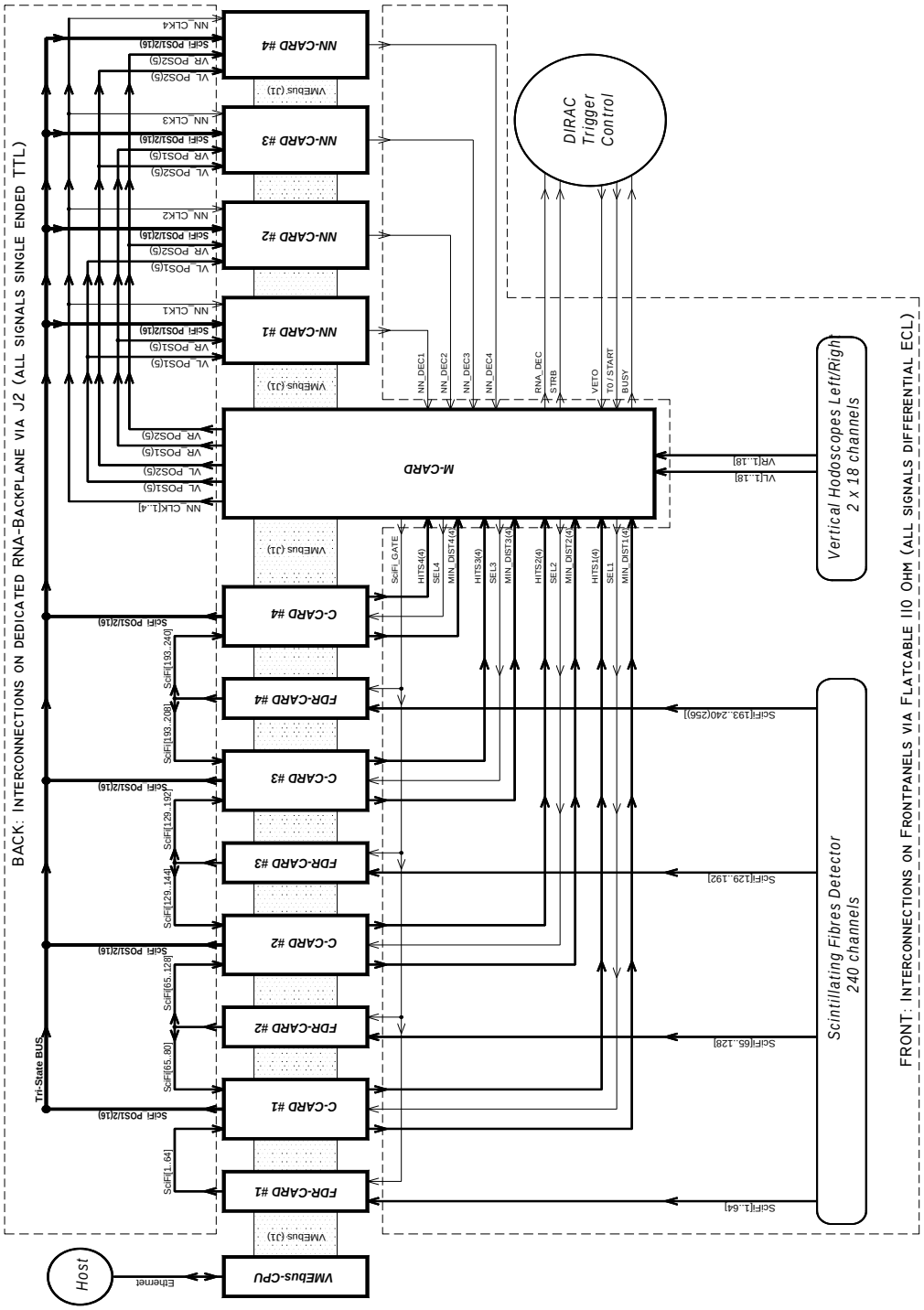


Figure 3 ***Signal Interconnection Diagram of the RNA-trigger:*** *On the left side the interconnections on the RNA-backplane are shown (single ended TTL signals), and on the right the interconnections via the frontpanels (dECL signals). For loading, testing and debugging all cards are connect via the J1-VMEbus to the commercial available VMEbus-CPU.*

4. Timing Diagram:

Figure 4 shows the typical timing diagram of the main signals during a complete *RNA*-trigger sequence. All the delay times are first rough estimations. To have all the signals valid after the *T0_START* the *SciFi_DATA* shows the delayed *SciFi TTL* detector-signals on the *FDR-CARDs*. The *RNA*-decision (*RNA_DEC*) stays valid until the next event (*T0_START*) is processed. The timing parameters *SciFi_DELAY*, *SciFi_GATE* and *V_DELAY* are programmable via the *VMEbus* with a resolution of 0.5ns in a range of 12.5ns to 140ns. The *VL* and *VR* detector signals need a minimum time-delay of 20ns with respect to the rising edge of the *T0_START*-signal. If a *SciFi_DELAY* of zero is programmed, the rising edge of the *SciFi_GATE* signal is delayed about 18ns with respect to the rising edge of *T0_START*.

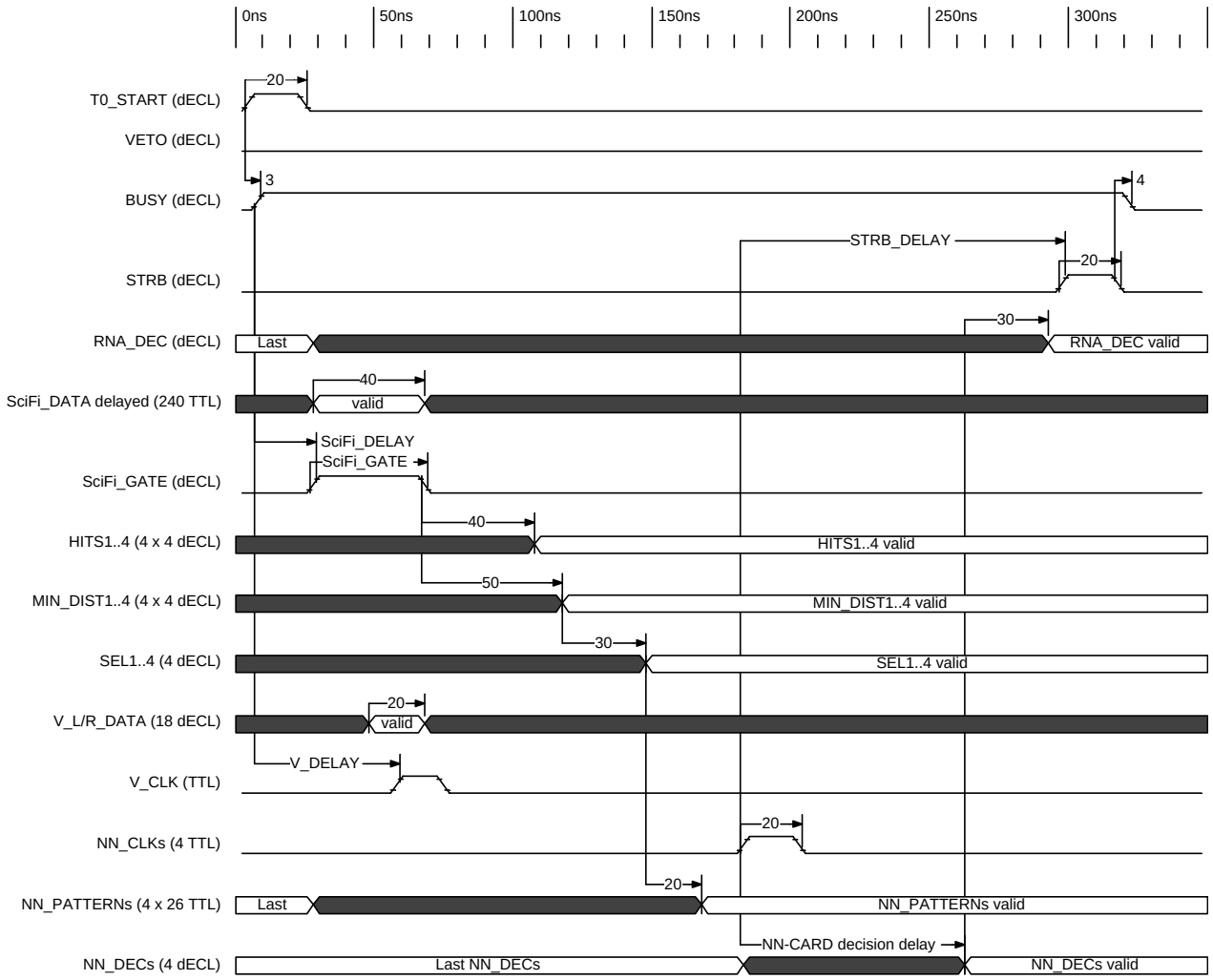


Figure 4 ***Timing Diagram of the RNA-trigger:*** *The RNA-trigger sequence is started by the T0_START signal; the STRB signal, which marks a valid RNA-decision, terminates the sequence. During the RNA-trigger is running, the BUSY signal is activated. All the delay times are prospective and not exactly defined yet.*

5. RNA-CRATE:

The complete electronics for the *RNA*-trigger is installed in the *RNA-CRATE* with the following dimensions: width=482mm, height=440mm and depth=650mm. As shown in *Figure 5* the crate is subdivided into two parts: 1) The left part has 3 slots with a height of 6U and the standard *VME* depth of 160mm. In this part the commercial available *VMEbus-CPU* for loading, testing and debugging is installed. 2) The right part provides 16 slots with a height of 9U and a depth of 220mm. In this part the *FDR-*, *C-*, *M-* and *NN-CARDs* are installed. Between the two parts of the crate the communication is enabled via the *J1-VMEbus*. The *RNA-CRATE* is a modification of the old *L3-NN-CRATE* (SP746d) which is no longer used for the L3 experiment.

Three main things need to be modified before the crate can be used for the *RNA*-trigger

- The –5.2V power supply has a maximum current of 5A only, which is to small for the *RNA*-trigger; therefore a stronger –5.2V power supply has to be installed. The +5V power supply has a maximum current of 300A, which should be sufficient for the *RNA*-trigger.
- The frontpanel with the power on/off switch and the control *LEDs* must be changed, so that all supply voltages (+5V, -5.2V, +12V, -12V) are indicated.
- The dedicated *RNA*-backplane has to be installed instead of the *L3 Distribution Backplane*.

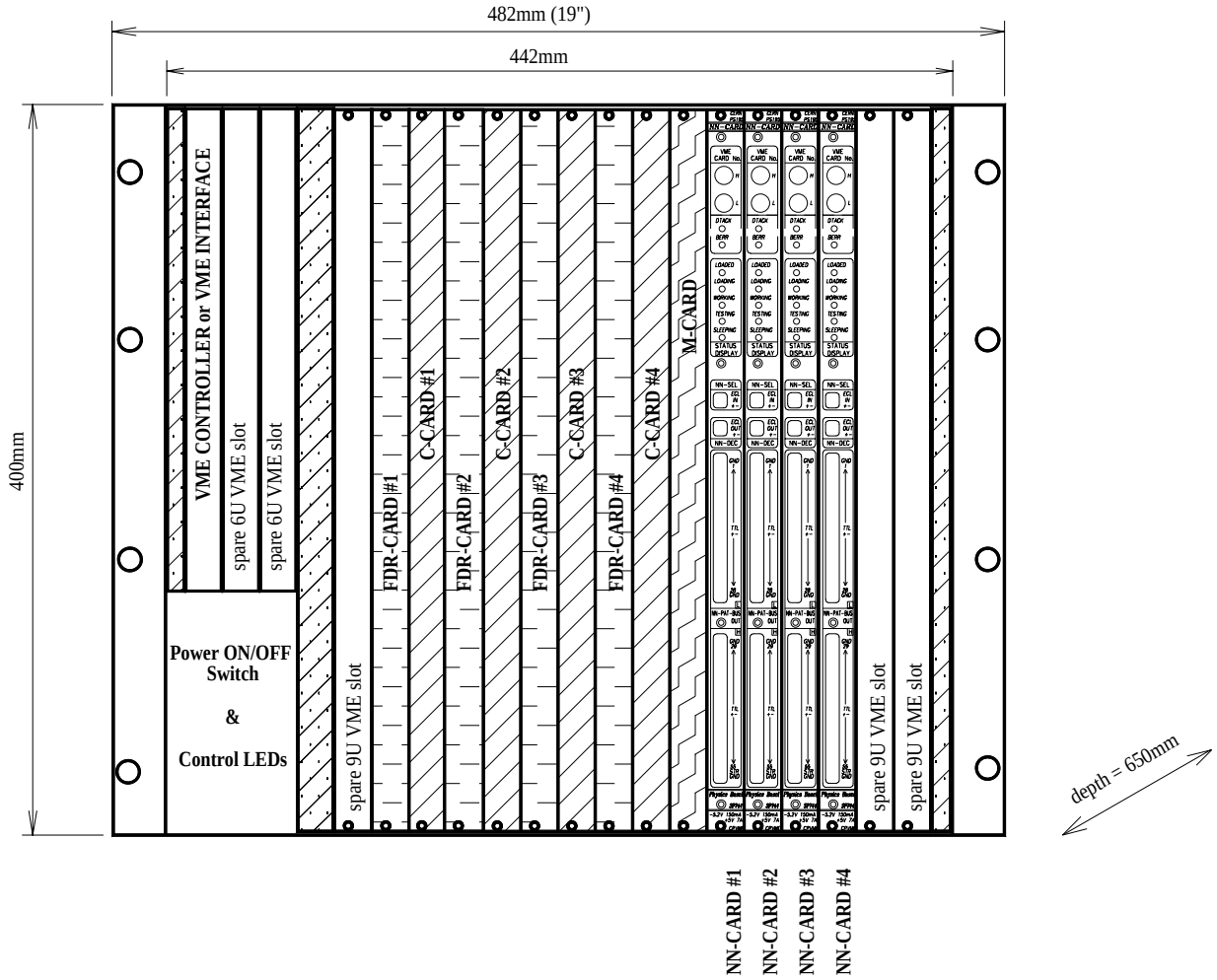


Figure 5 ***The RNA-CRATE:*** *The 16 slots in the right part have a height of 9U and a depth of 220mm. To reach short interconnections on the dedicated RNA-backplane, each FDR-CARD is followed by a C-CARD. All slots on the left and right part of the RNA-crate are interconnected via the J1-VMEbus. Two 6U slots and three 9U slots are spare.*

6. Board Specifications:

All three new *CARDs* for the *RNA*-trigger (*FDR-*, *C-* and *M-CARD*) are 9U *VME* boards with the dimensions of 366.7mm x 220mm. The *J1* connector (96 pin) is used for the standard *VMEbus* communication with the *CPU*, located in the left part of the *RNA-CRATE*. The *J2* connector (96 pin) is application specific; it is used for single ended *TTL* data in/output. The pin allocation is different for each of the three board types and is not defined yet. Unused pins of the *J2* connector are wired to GND. The *J3* connector (2 x 16 pin = 32 pin) is a high current connector for the supply voltages +5V, -5.2V and GND. The connector type is a DIN41612 / D / 0904-132-6921. The boards have a mechanical coding system which prevents the user from placing a wrong cards to the different slots of the *RNA-CRATE* and possibly destroying the system. A recess on the back of the *PCBs* at different positions for the different card types makes this feature possible (see *Figure 6*). The *RNA-CRATE* is equipped with corresponding bolts at the different locations; for example a *C-CARD* fits only in the slots foreseen for this card type. The *NN-CARDs* are coded by the missing *J3* connector.

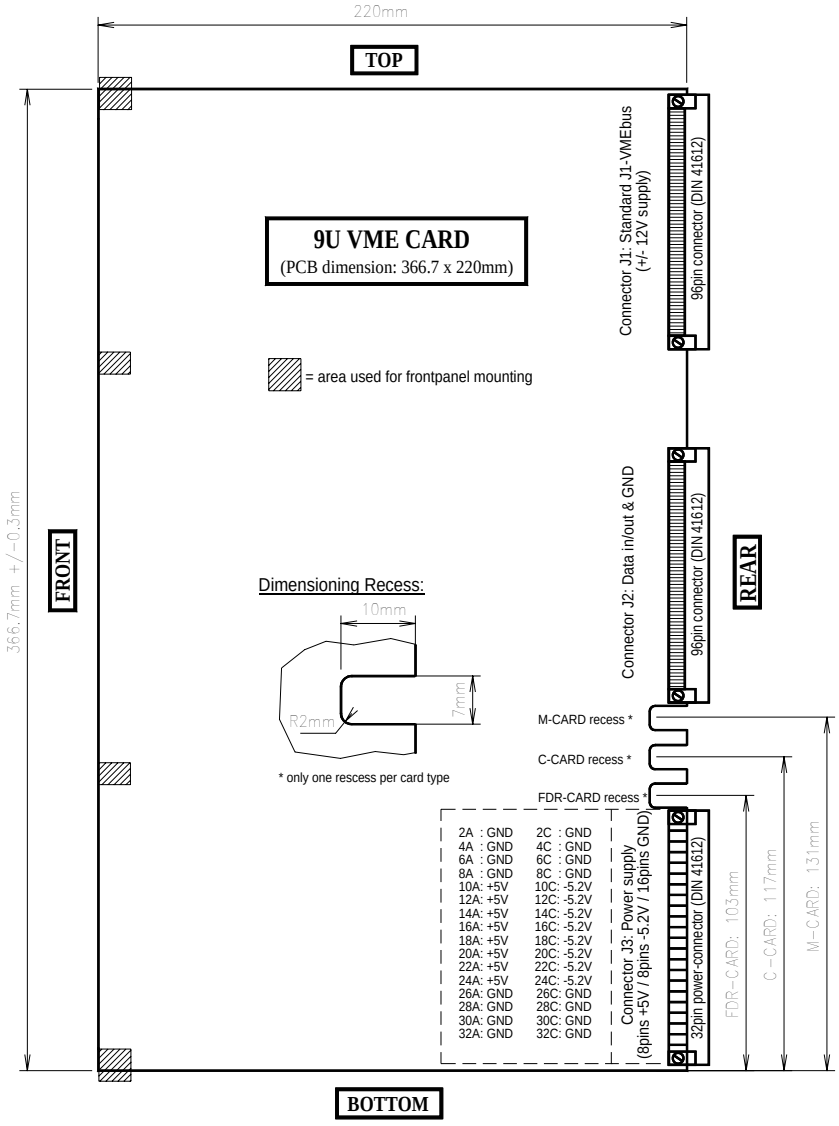


Figure 6 ***9U VME board:*** *A recess on the back of the PCB at different positions for the different card types makes sure that only the appropriate CARDs fits in the corresponding slots. The pin connections of the high current connector J3 are given at the bottom.*

7. Main Tasks:

Several tasks has to be executed before the *RNA*-trigger can be successfully utilize in the *DIRAC* experiment. At the moment the following main tasks can be identified (no entitlement to completeness). The order of the tasks is more less in sequence of time.

1. ***FDR-CARD:*** The detailed design (specifications, schematic diagram, *PCB*-layout, frontpanel, *CPLDs*), the production and the test of six *FDR-CARDs* have to be performed.

2. ***C-CARD:*** The detailed design (specifications, schematic diagram, *PCB*-layout, frontpanel, *CPLDs*), the production and the test (software required) of six *C-CARDs* have to be performed.

3. ***M-CARD:*** The detailed design (specifications, schematic diagram, *PCB*-layout, frontpanel, *CPLDs*), the production and the test (software required) of two *M-CARD* have to be performed.

4. ***C-, M- and NN-CARDs LUTs:*** All the *LUT*-files for the *C-*, *M* and *NN-CARDs* have to be generated. The *LUT*-files for the *C-*, *M-CARDs* are needed for complete testing and debugging the *C-* and *M-CARDs*. The *LUT*-files for the *NN-CARDs* are used for the final test of the *RNA*-trigger in the lab.

5. ***RNA-BACKPLANE:*** The detailed design (specifications, schematic diagram, *PCB*-layout), the production and the test of two *RNA-BACKPLANEs* have to be performed.

6. ***RNA-CRATE:*** The two *L3-NN-CRATEs* have to be modified to meet the requirements of the *RNA*-trigger (see section 5 of this paper).

7. ***RNA Extension Board:*** The design (specifications, schematic diagram, *PCB*-layout) and the production of four *RNA Extension Boards* have to be performed. The *RNA Extension Boards* make possible to test and debug the different *RNA*-boards (*C-*, *M* and *NN-CARDs*), plugged into the slots of the *RNA-CRATE.*

8. ***Test-patterns:*** Reasonable test-patterns for the final test in the lab (see next task) have to be created from good and bad events.

9. ***Final test in the lab:*** Software for testing and debugging the complete *RNA*-trigger has to be written. The *RNA-CRATEs* equipped with all *RNA*-boards will be tested in the lab. The final test is carried out with a fast pattern generator loaded with the test-patterns generated in task 8.

10. ***Installation and commissioning:*** The *RNA-CRATE* with the all *RNA*-boards have to be installed and cabled to the *DIRAC* experiment. The test-software written in task 9 has to be adapted to the *VMEbus CPU*. The proper functioning of the *RNA*-trigger with real detector signals has to be demonstrated.

Master-CARD (M-CARD) SP 827

The Design

(For DIRAC RNA-Trigger / CERN PS212)

Revision 2.0

Basel, 15. June 2001, M. Steinacher

1. Introduction:

This paper describes the design of the *Master-CARD* (*M-CARD*) SP 827 of the *Revised Neural Atomic* trigger (*RNA*-trigger). As *Figure 1* shows, the *M-CARD* is the heart of the *RNA*-trigger. It processes the information from the four *Concentrator CARDs* (*C-CARDs*), it selects the *C-CARD* which has found the smallest minimum distance and it controls the correct timing of the *RNA*-trigger sequence. Further the *M-CARD* is needed to store and preprocess the digital detector-signals of the two *Vertical Hodoscopes* (left *VL*, right *VR*) before they are sent to the four *NN-CARDs* (built for the *CP-LEAR* experiment / PS195). The four *NN-DECISIONs* are wired to the *M-CARD* where the final *RNA-DECISION* is made. The *M-CARD* is realized with fast electronics to reach a *RNA*-trigger decision-time below 300ns. The *M-CARD* is loaded, controlled and tested via the *VMEbus*. For an overview of the complete hardware needed for the *RNA*-trigger see '*DIRAC RNA-Trigger; Hardware Overview* / M. Steinacher / Basel, 14. December 2000'.

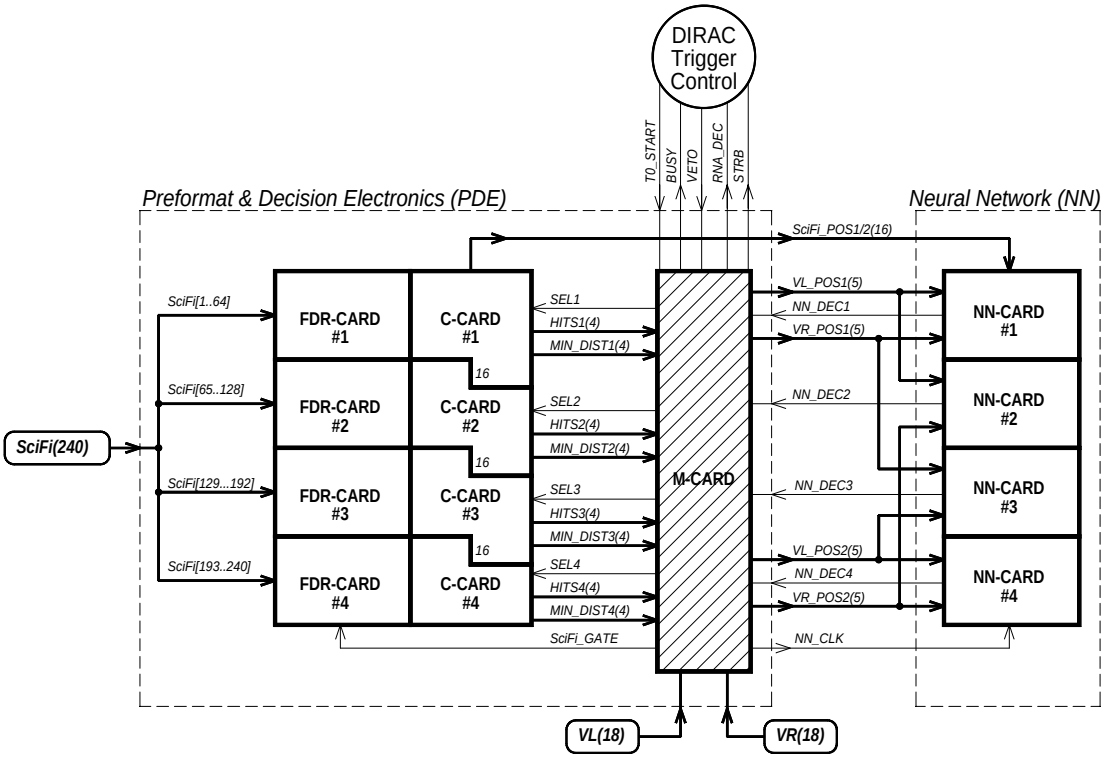


Figure 1 ***The layout of the complete RNA hardware:*** *Total 13 triple height VME-cards are needed. The M-CARD receives the information from the C-CARDs and the NN-CARDs and it interacts with the 'DIRAC Trigger Control'.*

2. Topographical description:

The printed circuit board (*PCB*) of the *M-CARD* is a eight layer board and has the same dimensions as the *NN-CARDs*. The height of 366.7mm corresponds to *FASTBUS* (triple height *VME*) and the depth of 220mm is an *EURO-standard* (see *Figure 2*).

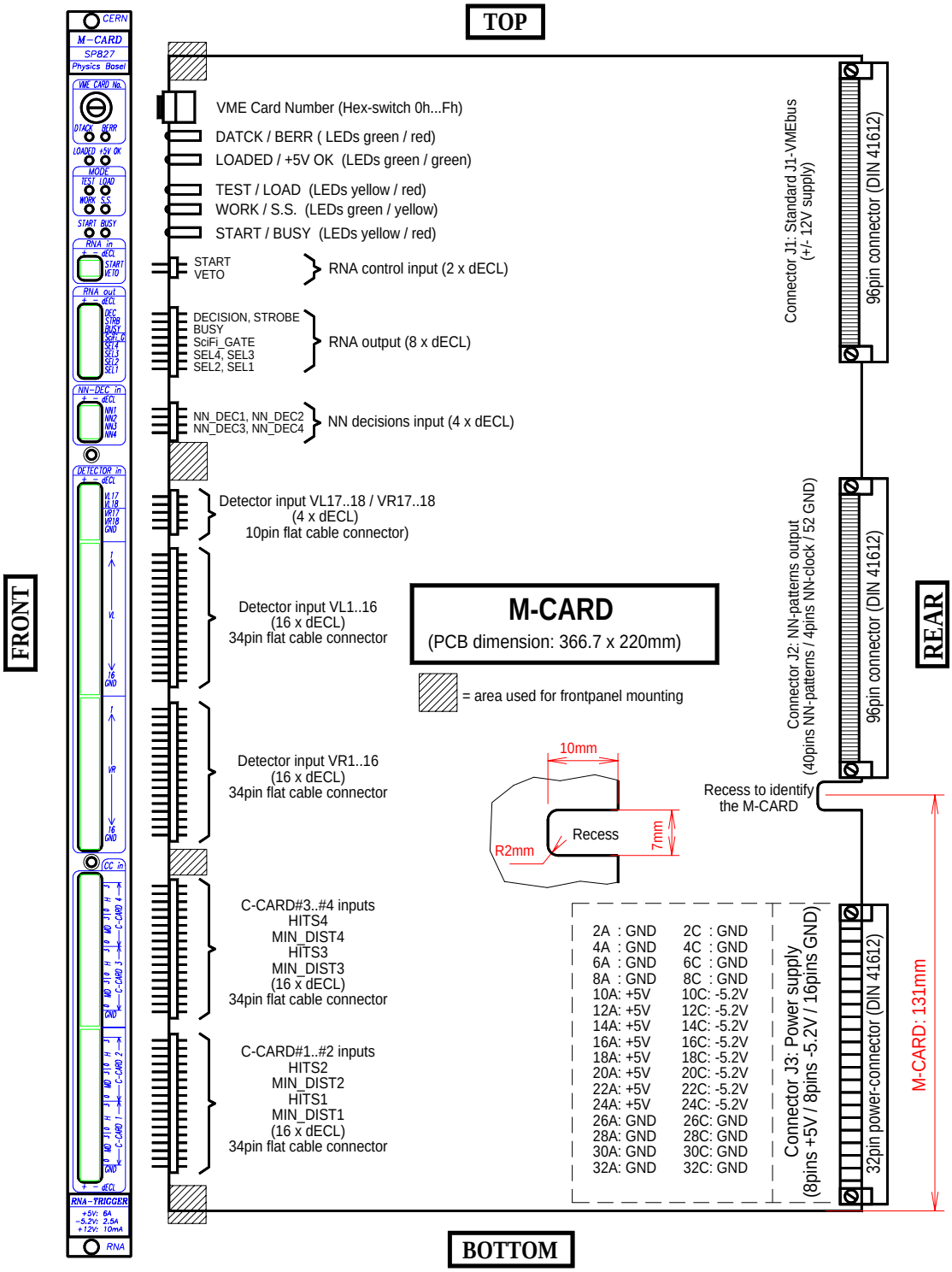


Figure 2 ***Topography of the M-CARD:*** *The detector-signals, the C-CARD in/output-signals, the RNA control in/output-signals and the NN-decisions are connected via the frontpanel. On the rear side the J1-connector is used for the VMEbus and the +12V/10mA supply, the J2 connector for the NN-PATTERNs and NN-CLOCKs, and the J3 connector for the supply voltages (+5V/4.5A; -5.2V/2.5A; 0V).*

2.1 Frontpanel description:

All the input-signals on the frontpanel of the *M-CARD* accept differential *ECL* (*dECL*) levels are normally terminated with 110Ω. For *daisy-chain* options the 110Ω terminations (56Ω networks) can be removed and the signals have to be terminated with 110Ω at the end of the chain. All the output-signals on the frontpanel provide also *dECL*-levels and are able to drive 110Ω lines (twisted pair flat cable). For *wired-OR* options the pull-down resistors (270Ω networks) of the *dECL* output drivers can be removed.

The 18 detector-signals from the *Vertical Hodoscope Left* (*VL1..18*) are distributed to a standard 34pin flat cable connector (*VL1..16*) and to a standard 10pin flat cable connector (*VL17..18*) which holds also *VR17..18* from the *Vertical Hodoscope Right*. The same scheme is also used for the 18 detector-signals from the *Vertical Hodoscope Right* (*VR1..18*).

The four *NN-DECISIONs* (*NN1..4*) have to be connected to the *M-CARD* with four short twisted pair cables (110Ω) to the four 2pin-connectors. Also the two *RNA* control-inputs *START* and *VETO* are connected with 2pin-connectors. If the *VETO* is not used it can be left unconnected and the *START* is enabled. The activation of the *START* signal is indicated with a yellow *LED* and the *BUSY*-signal with a red *LED*.

The eight *RNA* control-outputs *RNA_DECISION, STROBE, SciFi_GATE, BUSY, SEL4, SEL3, SEL2 and SEL1* have to be connected to the *M-CARD* via short twisted pair cables (110Ω) with 2pin-connectors.

The *VME Card Number* can be set by a *Hex Switch* in a range from *0h* to *Fh*. The *VMEbus* communication is indicated with the green *LED DTACK* (data transfer acknowledge) and the red *LED BERR* (bus error).

The different modes of the *M-CARD* are indicated with the following *LEDs*:

- ***LOADED*** green: This *LED* shows that the look up tables (*LUTs*) and the registers are loaded and the *M-CARD* is now ready to switch to the *WORK* mode.
- ***+5V OK*** green: This *LED* is activated if the +5V supply is present and the *RESET* is not active.
- ***TEST*** yellow: This *LED* indicates that the *M-CARD* is in one of the six *TEST* modes. Different tests can be carried out via the *VMEbus.*
- ***LOAD*** red: This *LED* indicates that the *M-CARD* is prepared for loading the *LUTs* via the *VMEbus.*
- ***WORK*** green: This *LED* indicates that the *M-CARD* is working. This mode can only be reached after the *LOADED* is set. In this mode the *M-CARD* is ready to process events on the rising edge of the *START*-signal.
- ***S.S.*** yellow: This *LED* shows that the *M-CARD* is in the *SINGLE SHOT* mode. In this mode single events under real-time conditions can be analyzed via the *VMEbus*.

2.2 Rear description:

The rear of the *M-CARD* holds the two standard 96pin connectors *J1*, *J2* and one 32pin *J3* power-connector (DIN 41612/D/0904-132-6921). The connector *J1* (upper) is used for the *VMEbus* and the +12V/10mA supply. The connector *J2* (middle) holds the *NN-PATTERNs* (40pins), the *NN-CLOCKs* (4pins) and several GND connections (52pins). The connector *J3* (lower) holds the power supply voltages +5V/4.5A (8pins), -5.2V/2.5A (8pins) and GND (16pins).

3. Functional Description:

Figure 3 shows the blockdiagram of the *M-CARD*; for clarity also the four *NN-CARDs* and the selected *C-CARD* (one of the total four *C-CARDs*) are also shown. The digital detector-signals of the two *Vertical Hodoscopes* (*VL1..18, VR1..18*) are converted into four positions and they are combined with the two *SciFi* positions to the four different *NN-PATTERNs*.

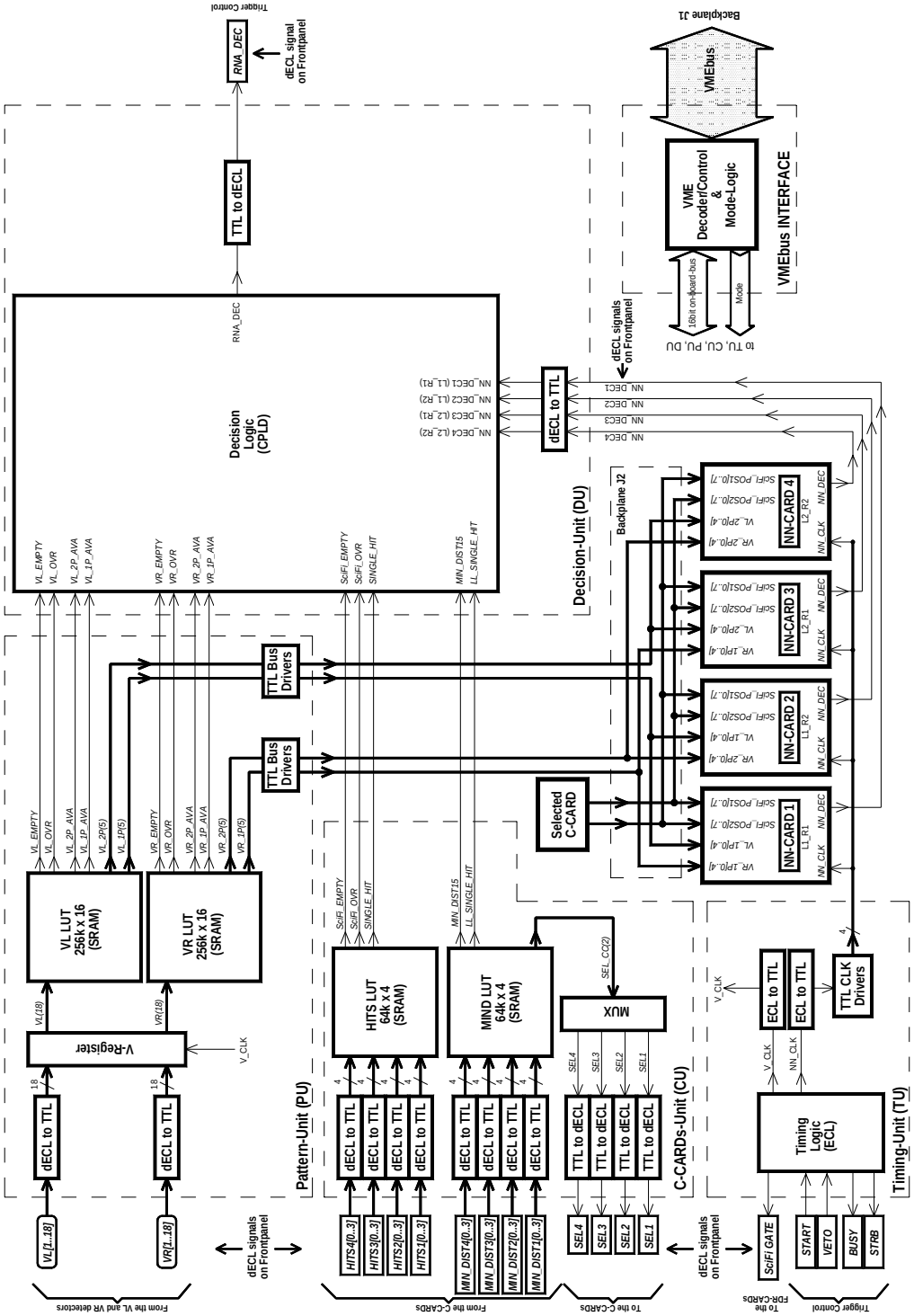


Figure 3 ***Blockdiagram of the M-CARD:*** *In the Pattern-Unit the four V-positions are generated from the detector-signals. The four minimum distances and the four number of hits (send by the four C-CARDs) are processed in the C-CARD-Unit. These values are used to select the C-CARD with the smallest minimum distance and to generate empty, overflow and single hit information.*

Each *NN-PATTERN* (26bit) holds information about two possible tracks in the two arms of the detector: Two *SciFi-positions* (each 8bit), one *VL-position* (5bit) and one *VR-position* (5bit). Each of the four off-line trained *NN-CARDs* searches for a good event in its pair of tracks.

The conversion of the detector hit-map to the *V-positions* is realized in the ***Pattern-Unit* (*PU*)** with two fast look up tables (*VL LUT, VR LUT*). The *PU* also detects if a hit-pattern has no hit (*VL_EMPTY, VR_EMPTY*) or more than two hits (*VL_OVR, VR_OVR*). These four flags are connected to the *Decision-Unit.*

The two *SciFi-positions* are directly transmitted (via a three-state bus) from the selected *C-CARD* to the four *NN-CARDs*. The ***C-CARDs-Unit* (*CU*)** receives the four minimum distances (*MIN_DIST1..4[0..3]*) and the four numbers of hits (*HITS1..4[0..3]*) from the four *C-CARDs*. It selects (*SEL1..4*) the *C-CARD* which has send the smallest minimum distance and it generates several flag signals used in the in the *Decision-Unit*.

All the flag signals, coming from the *PU* and *CU*, are used for the final *RNA-DECISION* in the ***Decision-Unit* (*DU*).** Also the four *NN-DECISIONs* (*NN_DEC1..4*) are fed to the *DU* where they are combined with the *AVAILABLE* flags (*VL_1/2P_AVA, VR_1/2P_AVA*) send by the *PU*. A valid *RNA-DECISION* is indicated by the strobe signal (*STRB*).

The ***Timing-Unit* (*TU*)** controls the correct synchronization of the *Vertical Hodoscope* input-register (*V_CLK*), the *Scintillator Fiber* gate signal (*SciFi_GATE*) and the *NN-CLK*s with respect to the *START* signal (see timing diagram in *Figure 4*). All detector-signals need a minimum time-delay of 20ns with respect to the rising edge of the *START*-signal (see *Figure 4*).

The ***VMEbus INTERFACE*** is the junction between the *VMEbus* and the *16bit on-board-bus* (*16bit OBB*). The *16bit OBB* is connected to all units and is used for loading and testing purpose.

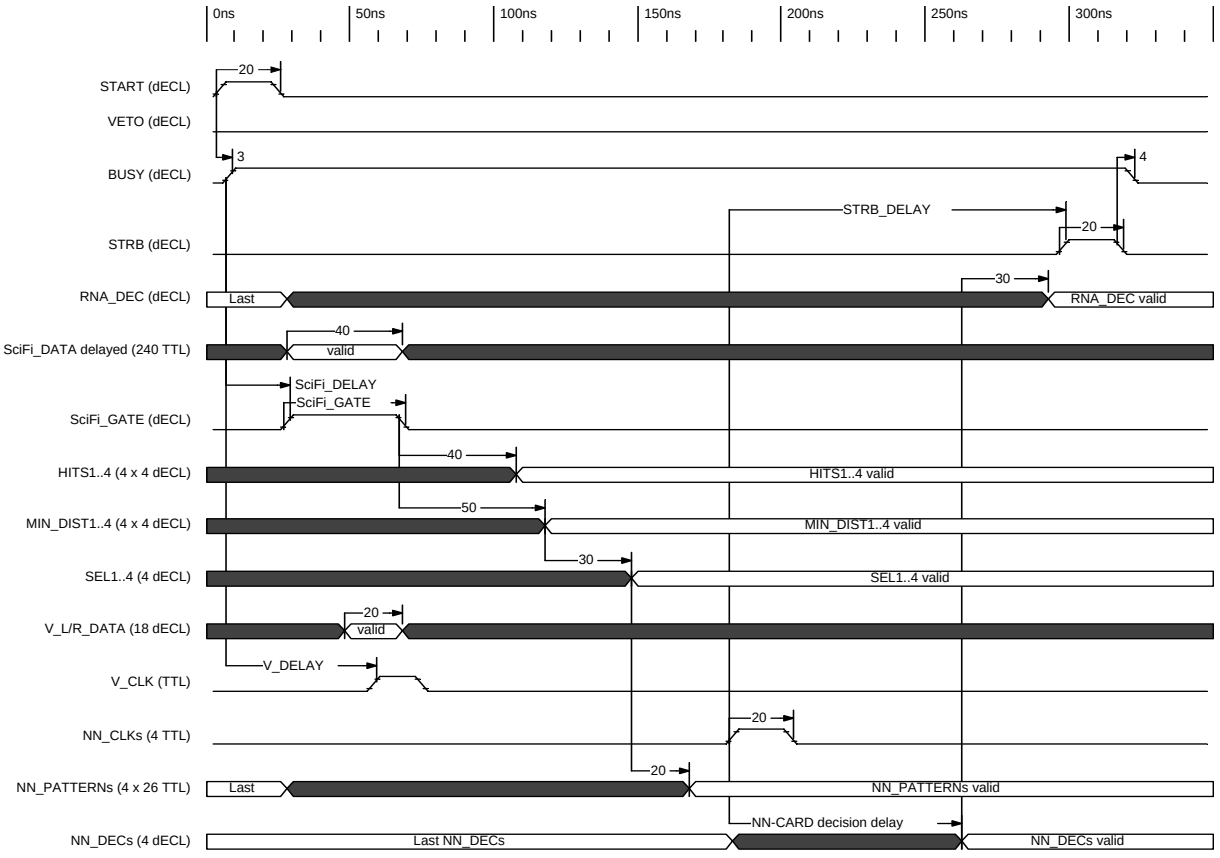


Figure 4 ***Timing Diagram of the RNA-trigger:*** *All the dECL signals are available on the frontpanel and the internal TTL signals are shown for clearness. The V_DELAY, the SciFi_DELAY and the SciFi_GATE are programmable with a fine resolution of 0.5ns.*

3.1 Timing-Unit (TU):

The *Timing-Unit* (*TU*) controls the complete *RNA*-trigger sequence which is started by the rising edge of the *START*-signal and the *STRB*-signal indicates the end of the sequence. During an event is processed the *BUSY*-signal is activated and any further *START*-signals are ignored during this time. *Figure 5* shows the block diagram of the *TU.*

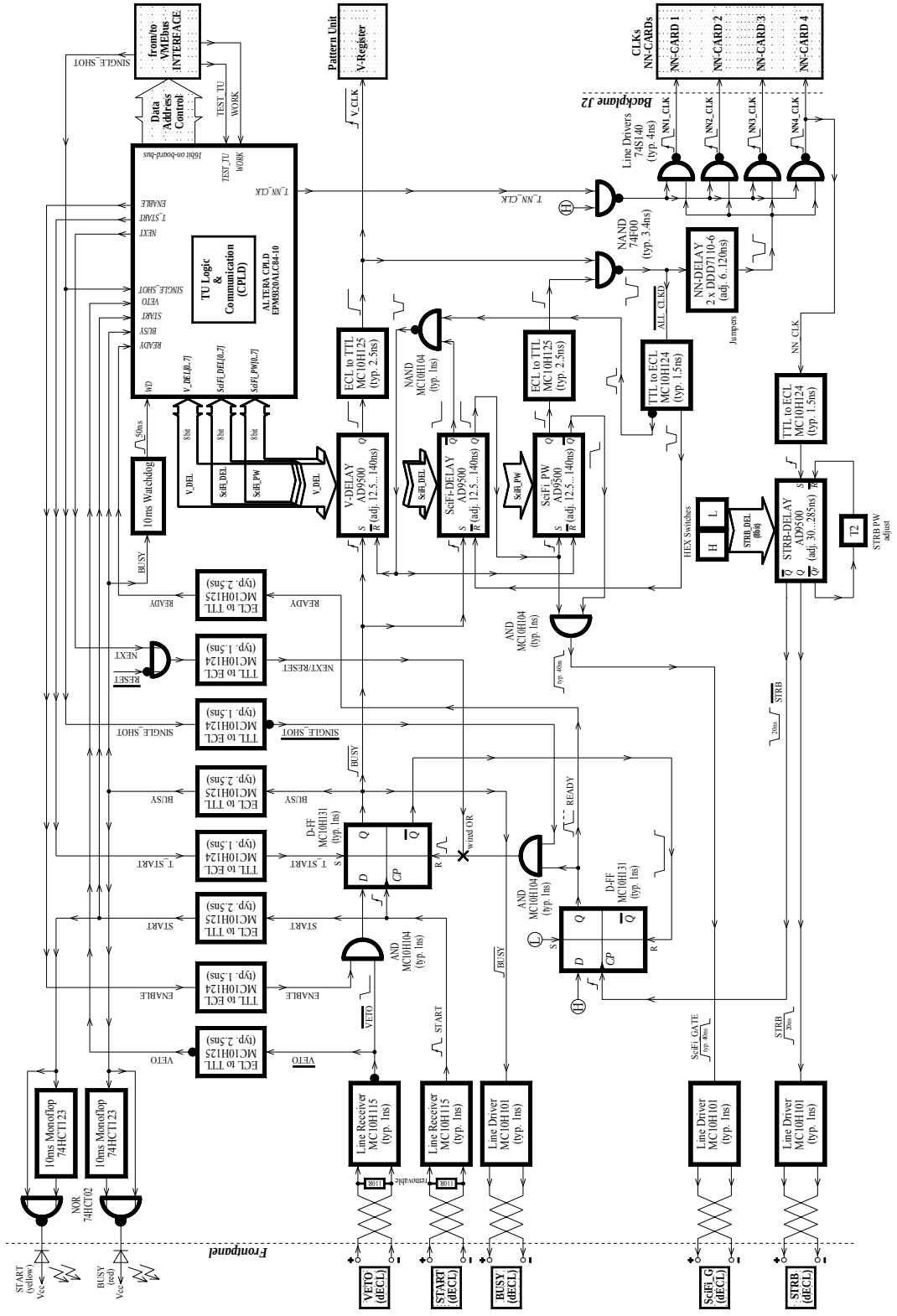


Figure 5 ***The block diagram of the Timing-Unit:*** *For fastest response all critical paths are realized with ECL logic. Several digital delays are used to adjust the proper timing of the signals.*

The *TU* generates the synchronized signals for the *V* input-registers (*V_CLK*), for the *Scintillator Fiber* registers (*SciFi_GATE*) and for the *NN-CARDs* (*NN_CLK*). The two input-register delays (*V-DELAY*, *SciFi-DELAY*) and the *SciFi_GATE PW* are *VMEbus*-programmable from 12.5ns..140ns with a resolution of 0.5ns (8bit). The two delays are started by the rising edge of the *BUSY*-signal and the *SciFi_GATE PW* by the rising edge of the *SciFi-DELAY* signal. At the minimum delay (12.5ns) all the corresponding detector-signals have to be valid at the latest 20ns after the rising edge of the *START*-signal. At the maximum *DELAY* (140ns) all the corresponding detector-signals have to be valid at the latest 147.5ns after the rising edge of the *START*-signal.

The time-delay from the rising edge of *V_CLK* or the falling edge of *SciFi_GATE* (the one which is the latest) to the *NN-CLK* is on-board programmable from 6ns..120ns (*NN-DELAY*) via a jumper with a resolution of 6ns. A longer delay can be reached by changing the corresponding delay-chips. The *NN-DELAY* delay is adjusted during test procedures and should not be changed during normal operation.

The *STRB*-signal is released after a certain time delay (*STRB-DELAY*) which is started by the rising edge of the *NN-CLK*. The *STRB-DELAY* is programmable via on board HEX-switches from 30ns..285ns with a resolution of 1ns (8bit). This *STRB-DELAY* is adjusted during test procedures and should not be changed during normal operation. The width of the *STRB*-signal is set by a capacitor-trimmer to 20ns and should not be changed.

The *TU* also provides a *BUSY*-signal which indicates that the *RNA*-trigger is processing an event. The state of the *BUSY*-signal is shown with a red *LED* on the frontpanel. The *TU* also accepts a *VETO*-signal which disables the *RNA*-trigger from accepting new events (the *START* signal is suppressed).

To prevent the *TU* from blocking due to spikes or power supply glitches a *Watchdog* is installed. If the *BUSY*-signal is longer than 10ms activated a reset is signal is released via the *NEXT*-signal.

In the ***WORK* mode** the *TU* is activated via the *ENABLE-output* and the test-outputs (*T_START, T_NN_CLK*) are inhibited.

In the ***SINGLE SHOT* mode** the normal *RNA*-trigger cycle is stopped after an event is completely processed. This is indicated by the *READY*-signal and a complete readout of the *M-CARD* and *C-CARDs* via the *VMEbus* can be carried out. A new event is only accepted after the *NEXT/RESET*-signal has been driven (high/low).

In the ***TEST_TU* mode** the *TEST START*-signal (*T_START*) and the *TEST NN-CLK* (*T_NN_CLK*) can be controlled from a test-register of the *TU Logic & Communication*.

The high-speed part of the *TU* is realized with *ECL* logic (Motorola 10k family) and *FAST TTL* logic (74F family). The control logic is implemented in a *CPLD* (Complex Programmable Logic Device). For further details see the *CPLD* documentation *TU-CHIP*.

3.2 Pattern-Unit (PU):

The *Pattern-Unit* (*PU*) converts the incoming detector-signal (*VL1..18, VR1..18*) from *dECL* to *TTL* and stores them on the rising edge of the *V_CLK*, generated by the *Timing-Unit* (*TU*). To register the detector hit-patterns is necessary, because the detector-signals are typically valid for only 20ns.

The *VL* hit-pattern (*VL1..18*) is processed by a fast 256k x 16bit *SRAM* working as look up table. The *VL-LUT* holds the two positions *VL_1P* (5bit) and *VL_2P* (5bit), the *VL_EMPTY*, the *VL_OVR*, the *VL_1P_AVA* and the *VL_2P_AVA* information corresponding to the applied *VL* hit-pattern. If no hit is registered in the *VL* hit-pattern, the *VL_EMPTY*-bit is activated. If more than two hits are registered in the *VL* hit-pattern, the *VL_OVR*-bit is activated. If only one hit is registered in the *VL* hit-pattern *VL_1P* holds the position number, *VL_2P* is set to zero (00000b) and only the *VL_1P_AVA* flag is activated. If two hits are registered in the *VL* hit-pattern, *VL_1P* holds the lower, *VL_2P* the higher position number and both *VL_1P_AVA* and *VL_2P_AVA* flag are activated. If only one position is valid the non valid position is zero. All this information is needed by the *Decision-Unit*. The position *VL_1P* (5bit) is distributed to the *NN-CARD 1* and to the *NN-CARD 2* via *TTL Bus Drivers* and the *RNA Backplane* via the *J2* connector. The position *VL_2P* (5bit) is distributed to the *NN-CARD 3* and to the *NN-CARD 4*.

The *VR* hit-pattern (*VR1..18*) is processed in the same way as the *VL* hit-pattern, only the distribution of the positions (*VR_1P*, *VR_2P*) to the *NN-CARDs* is different: The position *VR_1P* (5bit) is distributed to the *NN-CARD 1* and to the *NN-CARD 3* and the position *VR_2P* (5bit) is distributed to the *NN-CARD 2* and to the *NN-CARD 4*.

Before the *PU* is able to work, the look up tables (*VL-LUT, VR-LUT*) have to be loaded with the precalculated values via the *VMEbus*. To speed-up the *VL/VR-LUT* loading process, first the *LUTs* can be completely filled with the *OVERFLOW*-bit set and afterwards only *LUT*-addresses with a different value than *OVERFLOW* can be written; the *LUTs* holds only around 1‰ of different values than OVERFLOW.

Figure 6 shows the block diagram of the *Pattern-Unit*. The high-speed part of the *PU* is realized with *ECL* logic, fast *SRAMs* and *FAST TTL* (74F family) logic. The *PU Logic & Communication* is implemented in a *CPLD* (Complex Programmable Logic Device). For further details see the *CPLD* documentation *PU-CHIP*.

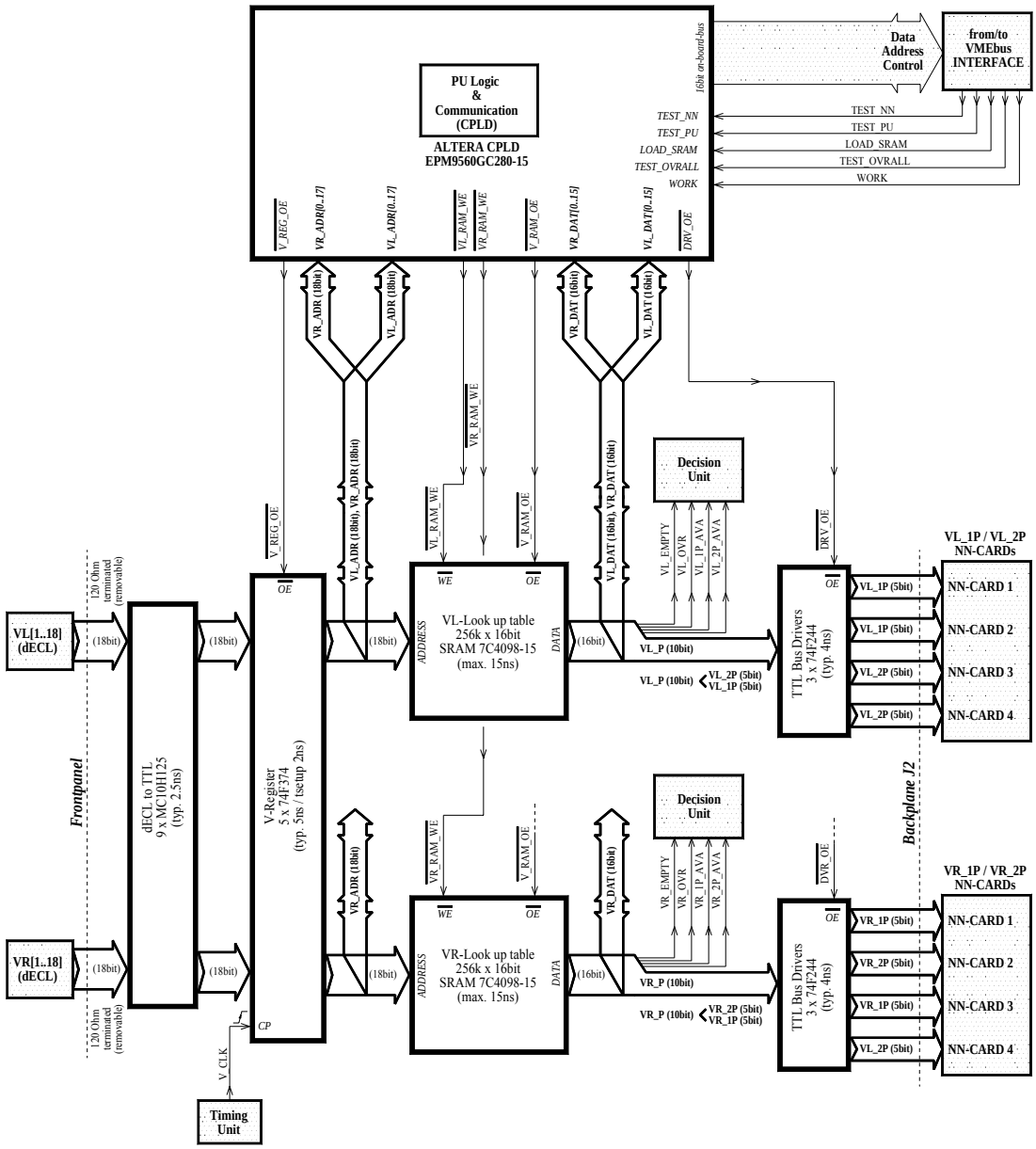


Figure 6 ***Pattern-Unit (PU) block diagram:*** *The detector hit-patterns are converted from dECL to TTL and are registered on the rising edge of the clock-signal (V_CLK). The precalculated relation between the hit-patterns (ADDRESS) and the two positions plus additional information (DATA) is stored in look up tables. This scheme leads to a very fast generation of the NN-patterns.*

The *PU* can be operated in different modes, which are selected via the *M-Mode register* (see also the part *VMEbus INTERFACE*):

- ***WORK:*** Detector hit-patterns are presented to the look up tables (*ADDRESS*) and its output-values (*DATA*) are sent to the *NN-CARDs* (via *TTL Bus Drivers*) and to the *DU*. This mode is selected during normal operation of the *M-CARD*. The input-registers (*/V_REG_OE*), the *SRAMs* (*/V_RAM_OE*) and the *TTL Bus Drivers* (*/DRV_OE*) are enabled.
- ***TEST_OVRALL:*** Test hit-patterns from test-registers of the *PU Logic & Communication* are applied to the look up tables (*ADDRESS*) and its output-values (*DATA*) are sent to the *NN-CARDs* (via *TTL Bus Drivers*) and to the *DU*. This mode allows an internal overall test

of the *RNA*-trigger. The input-registers (*/V_REG_OE*) is disabled the *SRAMs* (*/V_RAM_OE*) and the *TTL Bus Drivers* (*/DRV_OE*) are both enabled.

- ***TEST_NN:*** Test output-values from test-registers of the *PU Logic & Communication* are directly sent via the *TTL Bus Drivers* to the *NN-CARDs*. This mode allows testing the *NN-CARDs*. The input-registers (*/V_REG_OE*) and the *SRAMs* (*/V_RAM_OE*) are both disabled, the *TTL Bus Drivers* (*/DRV_OE*) is enabled.
- ***TEST_PU:*** *ADDRESSES* from test-registers of the *PU Logic & Communication* are applied to the look up tables and its output-values (*DATA*) are read via the *PU Logic & Communication*. This mode allows the readout of the look up tables (*SRAMs*). The input-registers (*/V_REG_OE*) and the *TTL Bus Drivers* (*/DRV_OE*) are both disabled, the *SRAMs* (*/V_RAM_OE*) is enabled.
- ***LOAD_SRAM:*** *ADDRESSES* and *DATA* are applied from test-registers of the *PU Logic & Communication* to the *SRAMs*. The *DATA* is written by driving (low/high) the *Write Enable* lines (*/VL_RAM_WE, /VR_RAM_WE*). This mode allows the loading of the look up tables. The input-registers (*/V_REG_OE*), the *SRAMs* (*/V_RAM_OE*) and the *TTL Bus Drivers* (*/DRV_OE*) are disabled, only the *Write Enable* lines are driven.

Mode	$\overline{V\_REG\_OE}$	$\overline{V\_RAM\_OE}$	$\overline{DRV\_OE}$	$\overline{VL/VR\_RAM\_WE}$
WORK	*0*	*0*	*0*	*1*
TEST_OVRALL	*1*	*0*	*0*	*1*
TEST_NN	*1*	*1*	*0*	*1*
TEST_PU	*1*	*0*	*1*	*1*
LOAD_SRAM	*1*	*1*	*1*	

Figure 7 ***Mode Truth Table for the PU:*** *For the different modes the corresponding state of the PU control-signals are shown in this table.*

3.3 C-CARDs-Unit (CU):

The *C-CARDs-Unit* (*CU*) receives the four minimum distances (*MIN_DIST1..4[0..3])* and the four number of hits (*HITS1..4[0..3]*) from the four *C-CARDs* and converts the signals from *dECL* to *TTL*. These values must not be registered because the *SciFi*-hitmaps are stored on the *FDR-CARDs* and the data sent by the four *C-CARDs* are stable until a new event is processed.

The *CU* selects (*SEL1..4*) the *C-CARD* which has send the smallest minimum distance and this card presents the two *SciFi* positions on the three-state bus on the *RNA-backplane.* If two or more *C-CARDs* send the same minimum distance, the lowest *C-CARD* is selected. A minimum distance of zero indicates a single hit on the corresponding *C-CARD*; a single hit is only preferred if the other *C-CARDs* send a minimum distance of 15. This selection task is implemented by a fast 64k x 4bit *SRAM* working as look up table (*MIND-LUT*) and a multiplexer. The multiplexer makes sure that, under all conditions, only one *C-CARD* can be selected and therefore no bus conflict can occur. The select signals are active high *dECL* levels. If all minimum distances are 15 the signal *MIN_DIST15* gets activated; if one or more minimum distance(s) are zero and the remainder are 15, the signal *looks like a single hit* (*LL_SINGLE_HIT*) is activated. These two flags are processed by the *Decision-Unit.*

Further the *CU* evaluates the four number of hits (*HITS1..4[0..3]*), found in each *C-CARD*, using a fast 64k x 4bit *SRAM* as look up table (*HITS-LUT*). If the sum of all the hits is zero, the signal *SciFi_EMPTY* gets activated, if it is exactly one the signal *SINGLE_HIT* is activated and if it is more than 5 the signal *SciFi_OVR* is set. These three flags are also evaluated by the *Decision-Unit.*

Before the *CU* is able to work, the look up tables (*MIND-LUT, HITS-LUT*) have to be loaded with the precalculated values via the *VMEbus*. To speed-up the *HITS-LUT* loading process, first the *LUT* can be completely filled with the *OVERFLOW*-bit set and afterwards only *LUT*-addresses with a different value than *OVERFLOW* can be written.

Figure 8 shows the block diagram of the *CU.* The high-speed part of the *CU* is realized fast *SRAMs* and *FAST TTL* (74F family) logic. The *CU Logic & Communication* is implemented in a *CPLD* (Complex Programmable Logic Device). For further details see the *CPLD* documentation *CU-CHIP*.

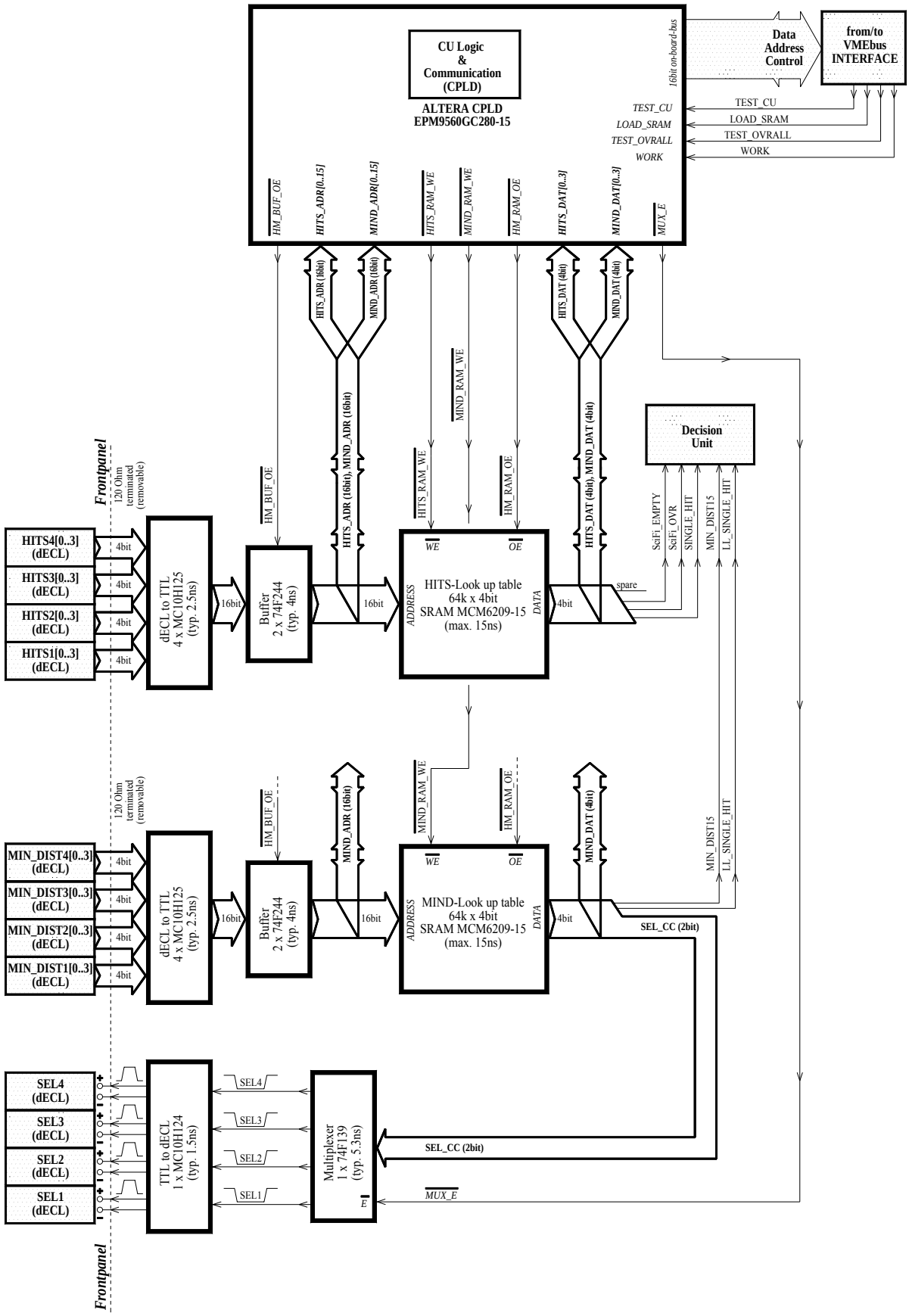


Figure 8 ***C-CARDs-Unit (CU) block diagram:*** *The information from the C-CARDs are processed with fast SRAMs used as look up tables. The multiplexer makes sure that only one C-CARD can be selected at one time and therefore no bus conflict can occur.*

The *CU* can be operated in different modes, which are selected via the *M-mode* register (see also the part *VMEbus INTERFACE*):

- ***WORK:*** The values from the *C-CARDs* are presented to the look up tables (*ADDRESS*) and its output-values (*DATA*) are used to control the multiplexer and the *Decision-Unit.* This mode is selected during normal operation of the *M-CARD*. The input-buffer (*/HM_BUF_OE*), the *SRAMs* (*/HM_RAM_OE*) and the *Multiplexer* (*/MUX_E*) are enabled.
- ***TEST_OVRALL:*** Test hit-patterns from test-registers of the *CU Logic & Communication* are applied to the look up tables (*ADDRESS*) and its output-values (*DATA*) are sent to the multiplexer and the *Decision-Unit*. This mode allows an overall test of the *RNA-trigger*. The input-buffer (*/HM_BUF_OE*) is disabled and the *SRAMs* (*/HM_RAM_OE*) and the *Multiplexer* (*/MUX_E*) are both enabled.
- ***TEST_CU:*** *ADDRESSES* from test-registers of the *CU Logic & Communication* are applied to the look up tables and its output-values (*DATA*) are read via the *CU Logic & Communication*. This mode allows the readout of the look up tables (*SRAMs*). The input-buffer (*/HM_BUF_OE*) and the *Multiplexer* (*/MUX_E*) are both disabled and the *SRAMs* (*/HM_RAM_OE*) is enabled.
- ***LOAD_SRAM:*** *ADDRESSES* and *DATA* are applied from test-registers of the *CU Logic & Communication* to the *SRAMs*. The *DATA* is written by driving (low/high) the *Write Enable* lines (*/HITS_RAM_WE, /MIND_RAM_WE*). This mode allows the loading of the look up tables. The input-buffer (*/HM_BUF_OE*), the *SRAMs* (*/HM_RAM_OE*) and the *Multiplexer* (*/MUX_E*) are disabled, only the *Write Enable* lines are driven.

Mode	$\overline{HM\_BUF\_OE}$	$\overline{HM\_RAM\_OE}$	$\overline{MUX\_E}$	$\overline{H/M\_RAM\_WE}$
WORK	*0*	*0*	*0*	*1*
TEST_OVRALL	*1*	*0*	*0*	*1*
TEST_CU	*1*	*0*	*1*	*1*
LOAD_SRAM	*1*	*1*	*1*	⎍

Figure 9 Mode Truth Table for the CU: *For the different modes the corresponding state of the CU control-signals are shown in this table.*

3.4 Decision-Unit (DU):

The *Decision-Unit* (*DU*) received the four *NN-DECISIONs* from the four *NN-CARDs* and converts the signals from *dECL* to *TTL*. These signals are directly fed to the *DU Logic & Communication*. The *NN-DECISIONs* are quasi-static signals (*NN-Pattern* is stable until a next event is processed) and therefore no register is needed. *Figure 10* shows the block diagram of the *DU.*

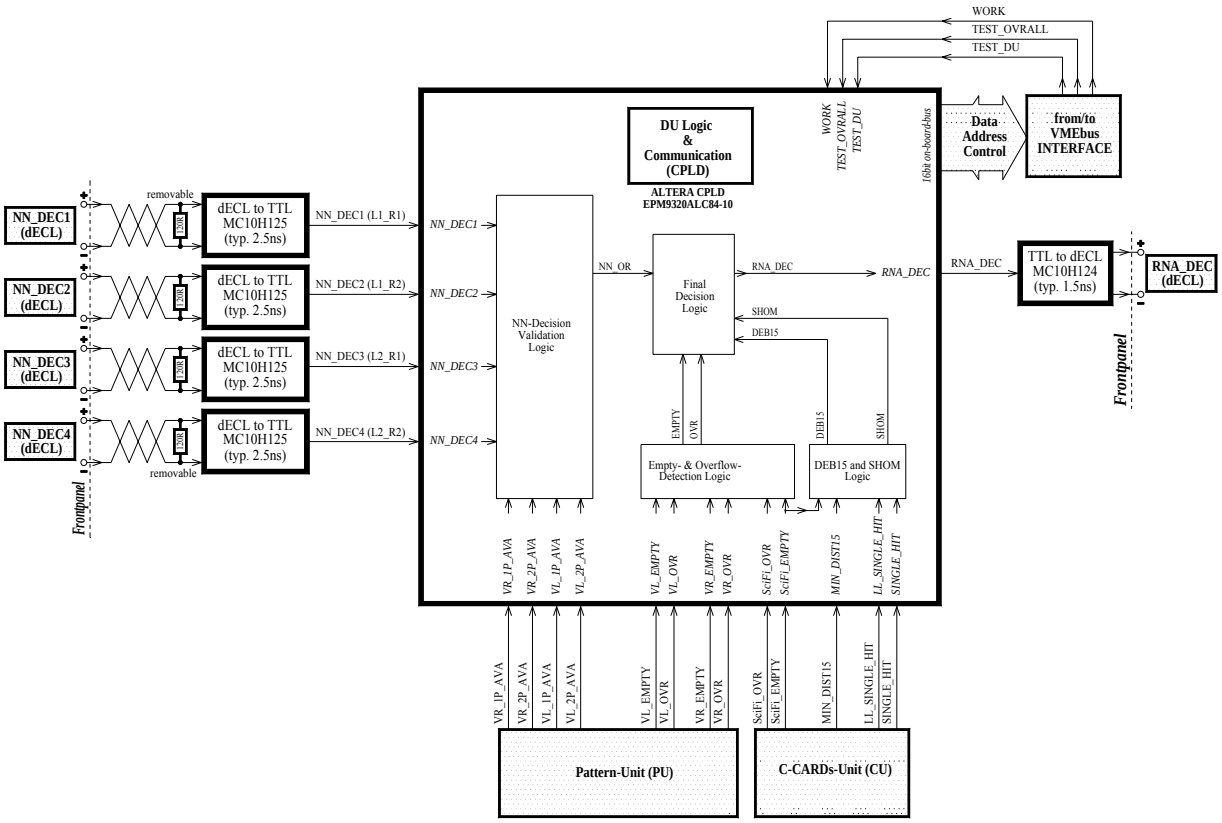


Figure 10 Decision-Unit (DU) block diagram: *In the DU the NN-DECISIONs and the flags of the Pattern-Unit and of the C-CARDs-Unit are combined to the final RNA-DECISON.*

The *DU* is realized with *ECL logic*, *FAST TTL* logic and a *CPLD* (Complex Programmable Logic Device). For further details see the *CPLD* documentation *DU-CHIP*.

The *DU* can be operated in different modes, which are selected via the *M-mode register* (see also the *VMEbus INTERFACE*):

- ***WORK:*** The external *NN-DECISIONs* are processed and the *RNA-DECISION* output is driven by the *DU Logic*. This mode is selected during normal operation of the *M-CARD*.
- ***TEST_OVRALL:*** Test patterns from test-registers of the *DU Logic & Communication* are applied to the *NN-DECISIONs* inputs. The *RNA-DECISION* output is driven by the *DU Logic.* This mode allows an overall test of the *RNA-trigger*.
- ***TEST_DU:*** The input and output of the *DU Logic* are controlled via test-registers of the *DU Logic & Communication* (see *Figure 11*). This mode allows complete testing the *Decision Logic* as well as the *RNA-DECISION* output driver.

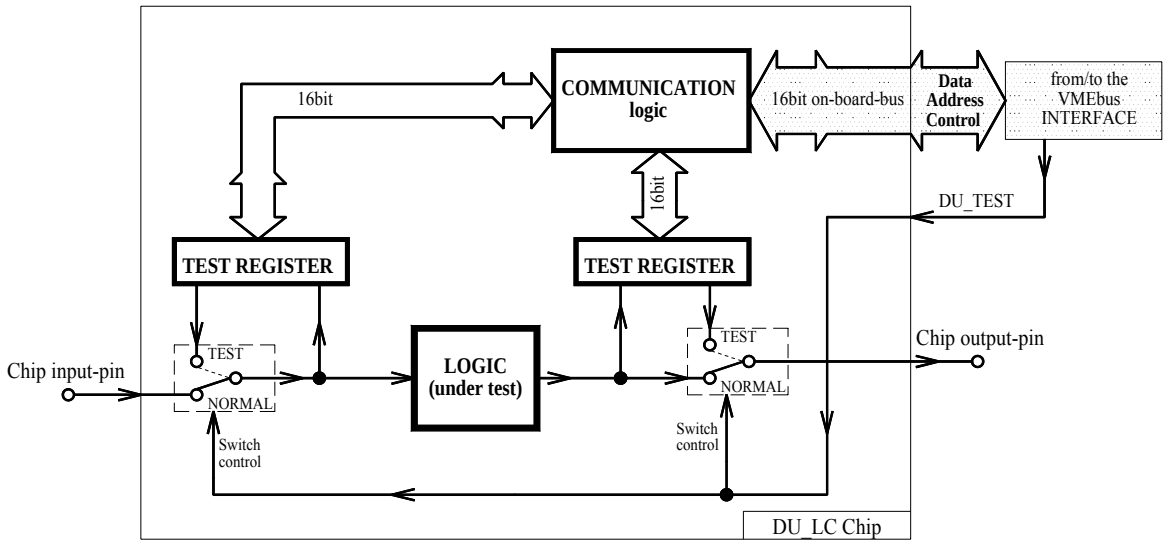


Figure 11 The DU Logic & Communication Chip in the TEST_DU mode: *In this test mode the inputs of the LOGIC can be stimulated from test-registers and the outputs of the LOGIC can be read via a test-registers. The output-pins of the chip are also controlled from test-registers.*

In the *Empty & Overflow Detection Logic* the *EMPTY* and the *OVR*-signal are generated by an or-function of the three detector *EMPTY*-signals (*VL_EMPTY* or *VR_EMPTY* or *SciFi_EMPTY*) and an or-function of the three detector *OVR*-signals (*VL_OVR* or *VR_OVR* or *SciFi_OVR*).

In the *NN-Decision Validation Logic* the four *NN_DECISIONs* (*NN_DEC1..4*) are combined with the two corresponding *AVAILABLE* flags (*VL_1P_AVA, VL_2P_AVA, VR_1P_AVA, VR_2P_AVA*) from the *Pattern-Unit*. This ensures that only *NN_DECISIONs* with the corresponding positions available are taken into the final decision. The or-function of the *validated NN-Decisions* (*NN_VAL1..4*) results in the signal *NN_OR*:

NN_VAL1 = NN_DEC1* and *VL_1P_AVA* and *VR_1P_AVA
NN_VAL2 = NN_DEC2* and *VL_1P_AVA* and *VR_2P_AVA
NN_VAL3 = NN_DEC3* and *VL_2P_AVA* and *VR_1P_AVA
NN_VAL4 = NN_DEC4* and *VL_2P_AVA* and *VR_2P_AVA

NN_OR = NN_VAL1* or *NN_VAL2* or *NN_VAL3* or *NN_VAL4

The *DEB15 and SHOM Logic* generates the following two signals: *Distance Equal or Bigger than 15* (*DEB15*), which indicates that the two closest hits found on all the four *C-CARDs* has a distance of 15 or more. The signal *Single Hit On Multiple C-CARDs* (*SHOM*) identify the case of a single hit on two or more different *C-CARDs*. These two signals are generated by the following equations:

DEB15 = MIN_DIST15* and not *SciFi_EMPTY
SHOM = LL_SINGLE_HIT* and not *SINGLE_HIT

The *Final Decision Logic* generates the *RNA-DECISION* out of the following signals: *EMPTY*, *OVR*, *NN_OR*, *DEB15* and *SHOM*. The *OVERFLOW*-condition can be enabled or disabled via a bit in the control register of the *DU Logic & Communication.*

If the *OVERFLOW*-condition is enabled the following logic is applied:
***RNA_DEC* = *NN_OR* and not (*EMPTY* or *DEB15* or *SHOM* or *OVR*)**

If the *OVERFLOW*-condition is disabled the following logic is applied:
***RNA_DEC* = *OVR* or [*NN_OR* and not (*EMPTY* or *DEB15* or *SHOM*)]**

An activated *RNA_DECISION* indicates that the *RNA-trigger* has detected a good pionic atom event.

3.5 VMEbus INTERFACE:

The *VMEbus INTERFACE* is responsible for the bi-directional communication between the *M-CARD* and a *VMEbus*-based computer. The *VMEbus INTERFACE* is located between the *VMEbus* and the *16bit on-board-bus* of the *M-CARD*.

The *M-CARD* and the *NN-CARDs* are so called *A16/D16 slave VME-CARDs* (see the book *THE VMEbus SPECIFICATION*; *ANSI/IEEE 1014-198 ; IEC821 & IEC297*). The *A16/D16* means that the *VME-CARD* decodes only 16 address bit and uses only 16 data bit. The *slave* means that the *VME-CARD* cannot act as a bus master. The *VME-CARD* is designed for a *short 16bit access*, as proposed in the book *THE VMEbus SPECIFICATION* for I/O-cards. The access mode is coded in the *Address Modifier* (*AM*; 5bit). The *VME-CARD* listens only to *short 16bit accesses*, which have the *AM*-codes *2Dh* or *29h*. The data-width of the access is determined by the control lines *DS0*, *DS1* and *LWORD*. The *VME-CARD* responds with a *Data Transfer Acknowledge* (*DTACK*-signal) only if a *double-byte* (16bit data) access is carried out. If a *triple-byte*, a *quad-byte* or a *unaligned double-byte* access is detected, the *VME-CARD* responds with a *Bus Error* (*BERR*-signal). The *DATCK*- and *BERR*-signals are indicated with a green and a red LED on the front panel.

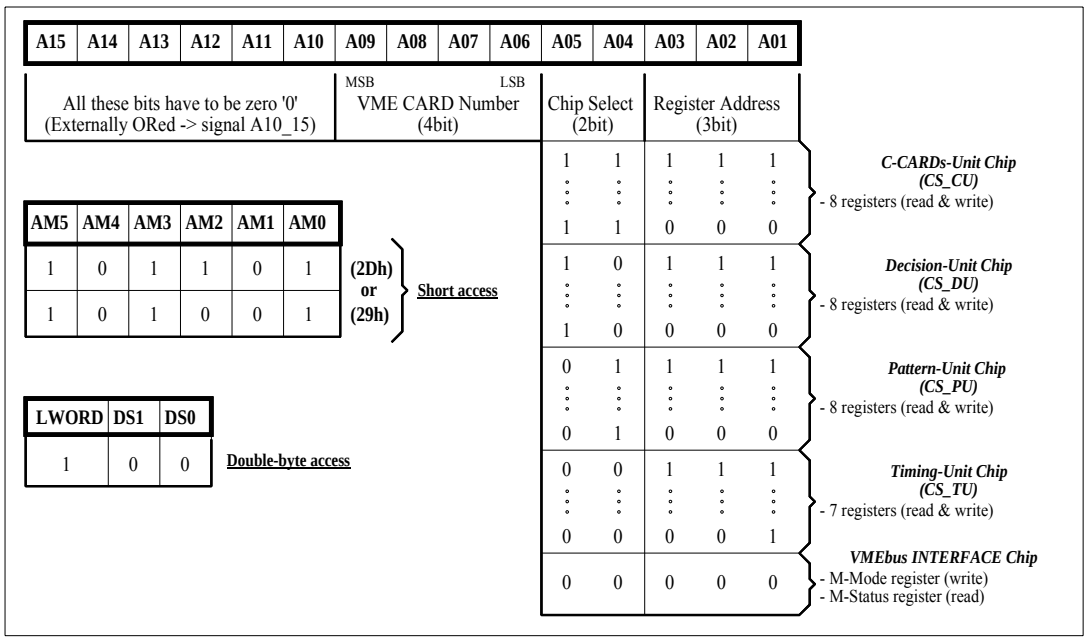


Figure 12 The VME-address decoding scheme of the M-CARD: *The M-Mode (W) and M-Status (R) register are located at address zero.*

Figure 12 shows the *VME*-address decoding performed in the *VMEbus Decoder & Control Logic*. Because the *VME-CARD* uses the *double-byte* (16bit data) access the *VME*-address-lines start from *A1*. The *VME Card Number* is set by the *Hex Switch* on the front panel of the *M-CARD*. The *VME Card Number* can be set from *0h* (*0dec*) to *Fh* (*15dec*), so sixteen different *VME-CARDs* can be addressed. Only if the *VME Card Number* matches the addresses *A6...A9*, and the addresses *A10...A15* are zero, the *M-CARD* is selected (*CARD_SELECTED*). At the address zero of the *M-CARD*, the *M-Mode* and *M-Status* registers are located. The addresses *A4* and *A5* determines which of the four *Communication Chips* (*TU, PU, DU, CU*) is selected. The lowest three addresses (*A1...A3*) are used to access the different 16bit-registers of the selected *Communication Chip.*

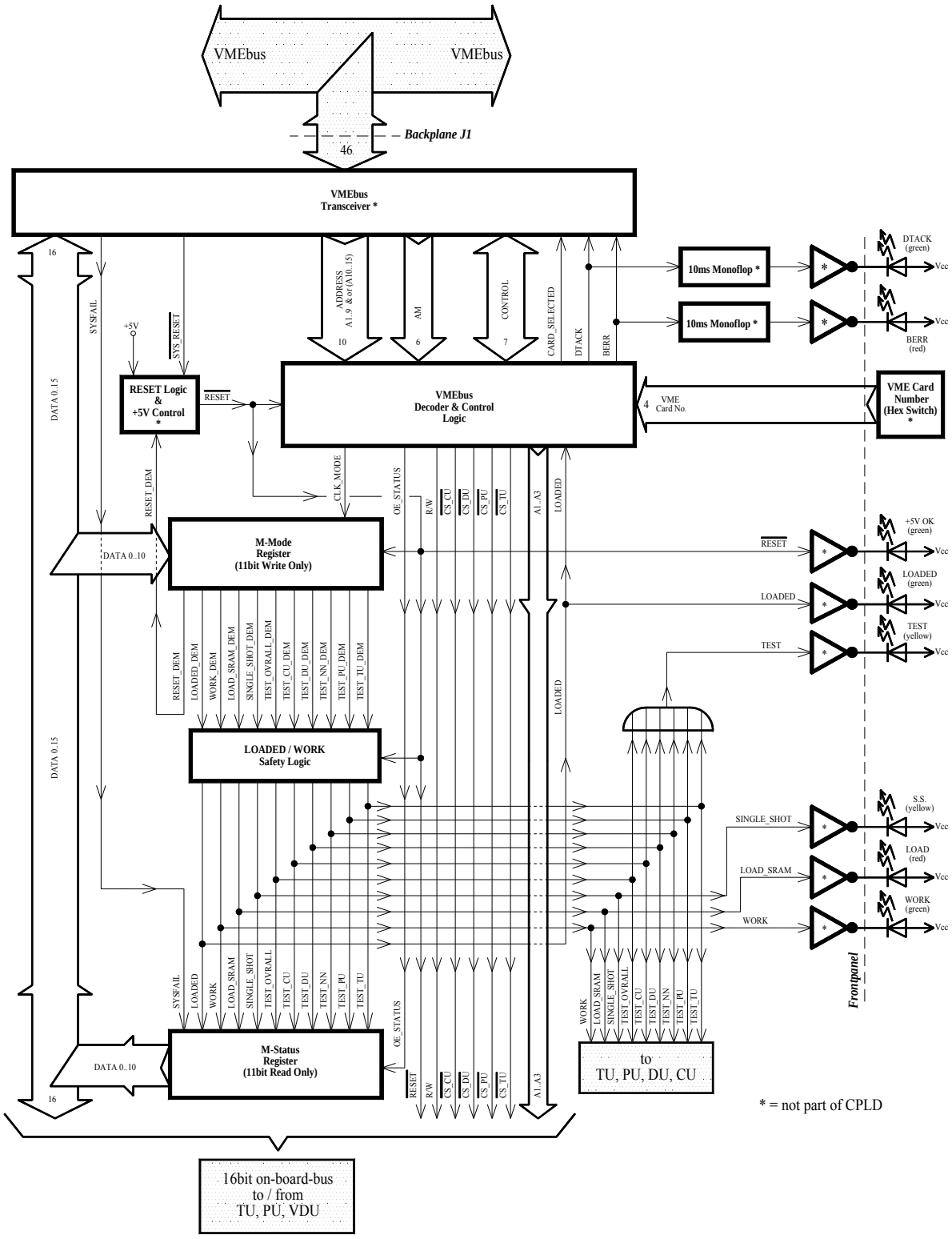


Figure 13 VMEbus INTERFACE block diagram: *The blocks marked with * are not part of the CPLD. The VMEbus INTERFACE performs the communication between the M-CARD and a VMEbus-based computer.*

The block diagram of the *VMEbus INTERFACE* is shown in *Figure 13*. In *the VMEbus TRANCEIVER* the *VMEbus TTL*-signals are buffered via special transmitter- and receiver-chips, as specified in the book *THE VMEbus SPECIFICATION*. To reduce the number of pins needed for the *VME-CHIP* the or-function of the address lines A10..15 is external implemented.

The *M-Mode Register* (write only) is used to select the different modes of *the M-CARD*:

- ***LOADED* mode:** The look up tables and the registers of the *M-CARD* are loaded and the *M-CARD* is ready to switch to the *WORK* mode. For safety reasons, writing to any register (except the *NEXT/RESET* in the *TU*) is suppressed in this mode. To switch to any *TEST* mode or to the *LOAD* mode is inhibited until the *LOADED* mode is cleared. The *LOADED* mode cannot be reached if any *TEST* mode or to the *LOAD* mode is active. These restrictions are implemented in the *LOADED*/*WORK Safety Logic*. The *LOADED* mode is displayed with a green *LED* on the frontpanel.
- ***WORK* mode:** To reach the *WORK* mode the *LOADED* mode has to be set previously. In this mode the *M-CARD* is ready to process events on the rising edge of the *START*-signal. The *WORK*-signal is wired to all of the four *TU-, PU-, DU and CU-Chips*. The *WORK* mode is displayed with a green *LED* on the frontpanel.
- ***SINGLE_SHOT* mode:** In this mode single events under real-time conditions can be analyzed via the *VMEbus*. The *SINGLE_SHOT*-signal is wired to the *TU-Chip* only. The *SINGLE_SHOT* mode is displayed with a yellow *LED* on the frontpanel.
- ***LOAD_SRAM* mode:** This mode allows the loading of the look up tables. The *LOAD_SRAM*-signal is wired to the *PU-* and *CU-Chips*. The *LOAD_SRAM* mode is displayed with a red *LED* on the frontpanel.
- ***TEST_OVRALL* mode:** This mode allows the overall testing of the *RNA trigger.* The *TEST_OVERALL*-signal is wired to the *PU-*, *DU* and *CU-Chips*.
- ***TEST_TU* mode:** This mode enables the testing of the *Timing-Unit.* The *TEST_TU*-signal is wired to the *TU-Chip* only.
- ***TEST_PU* mode:** This mode allows the readout of the look up tables in the *Pattern-Unit*. The *TEST_PU*-signal is wired to the *PU-Chip* only.
- ***TEST_CU* mode:** This mode allows the readout of the look up tables in the *C-CARDs-Unit*. The *TEST_CU*-signal is wired to the *CU-Chip* only.
- ***TEST_NN* mode:** This mode allows the testing of the *NN-CARDs* via the *Pattern-Unit*. The *TEST_NN*-signal is wired to the *PU-Chip* only.
- ***TEST_DU* mode:** This mode allows the testing of the *Decision Logic* as well as the output driver. The *TEST_DU*-signal is wired to the *DU-Chip* only.

If one of the *TEST* modes is selected the yellow *LED TEST* on the frontpanel is activated. With the restrictions mentioned above, the *LOADED* mode can be activated or deactivated via the *LOADED_DEM* bit in the *M-Mode Register*. A *RESET*-signal (active low) deactivates the *LOADED* mode immediately and a *SYSFAIL*-signal is generated on the *VMEbus*.

The *RESET Logic & +5V Control* is responsible for the correct timing of the *RESET*-signal, for supervising the +5V supply-voltage and for the power-on *RESET*. The *RESET*-signal is distributed all over the *M-CARD* and it sets the registers in a well defined state. There are three different sources, which can activate the *RESET*-signal:

- If the +5V supply-voltage (Vcc) drops below a certain voltage (typical +4V).
- If a system-reset (*/SYS_RESET*) is received via the *VMEbus*.
- If the *RESET_DEM* bit of the *M-Mode Register* is set.

The *M-Status Register* (read only) allows to read the status of the *M-CARD* and the status of the *SYSFAIL*-signal on the *VMEbus*. The *SYSFAIL*-signal is active (low), if the *M-CARD* or one of the four *NN-CARDs* is no longer in the *LOADED* mode. The *SYSFAIL*-signal can easily be checked via the *VMEbus* for supervising the *RNA*-trigger.

The *VMEbus INTERFACE* is realized with *TTL* and *HCT* logic and a *CPLD* (Complex Programmable Logic Device). For further details see the *CPLD* documentation *VME-CHIP*.

4. NN-Patterns:

The *NN-CARDs* have a 55bit wide *TTL* pattern-input. The *RNA*-trigger application needs only a 26bit *NN-PATTERN* and the unused inputs are pulled to GND. The 26bit *NN-PATTERN* consists of the two *SciFi*-positions *SciFi_POS1* (8bit) and *SciFi_POS2* (8bit), one *VL*-position *VL_1P* or *VL_2P* (5bit) and one *VR*-position *VR_1P* or *VR_2P* (5bit). The *NN-PATTERN* bits are terminated on the *NN-CARDs* with 180Ω to +5V and 330Ω to GND. The *SciFi_POS1/2* signals (16bit, *NN_PAT[0..15]*) are fed in parallel to all of the four *NN-CARDs*; therefore only the last *NN-CARD* (number 4, most right) is terminated at these input bits (*NN_PAT[0..15]*). The *VL/VR_1P/2P* are driven for each *NN-CARD* separately by the *M-CARD* and therefore on all four *NN-CARDs* these input bits are terminated.

The bit allocation in the *NN-PATTERN* is with the MSB at the lowest position and the LSB at the highest position (e.g. *NN_PAT[0]* -> MSB of *SciFi_POS1* / *NN_PAT[7]* -> LSB of *SciFi_POS1*).

The following different *NN-PATTERNs* are applied to the four *NN-CARDs* via the *RNA Backplane* (SP 827A):

NN-CARD #1: (Most left; no terminations on *NN_PAT[0..15]*)

NN_PAT[7...0]	->	*SciFi_POS1 (8bit)*
NN_PAT[15...8]	->	*SciFi_POS2 (8bit)*
NN_PAT[20...16]	->	*VL_1P (5bit)*
NN_PAT[25...21]	->	*VR_1P (5bit)*

NN-CARD #2: (No terminations on *NN_PAT[0..15]*)

NN_PAT[7...0]	->	*SciFi_POS1 (8bit)*
NN_PAT[15...8]	->	*SciFi_POS2 (8bit)*
NN_PAT[20...16]	->	*VL_1P (5bit)*
NN_PAT[25...21]	->	*VR_2P (5bit)*

NN-CARD #3: (No terminations on *NN_PAT[0..15]*)

NN_PAT[7...0]	->	*SciFi_POS1 (8bit)*
NN_PAT[15...8]	->	*SciFi_POS2 (8bit)*
NN_PAT[20...16]	->	*VL_2P (5bit)*
NN_PAT[25...21]	->	*VR_1P (5bit)*

NN-CARD #4: (Most right; **terminations** on *NN_PAT[0..15]*)

NN_PAT[7...0]	->	*SciFi_POS1 (8bit)*
NN_PAT[15...8]	->	*SciFi_POS2 (8bit)*
NN_PAT[20...16]	->	*VL_2P (5bit)*
NN_PAT[25...21]	->	*VR_2P (5bit)*

Fanout/Delay/Register
description

The Fanout/Delay/Register Card receives 64 data signals and a gate in differential ECL level (dECL) and is part of the hardware to be used on the Revised Neural Atomic trigger of the DIRAC experiment at CERN.

Description

The main blocks of the FDR are the Fanout block and the Delay and Register block. Since the data signals are present prior to the trigger , a delay on the data is mandatory and in the end of the trigger the delayed pattern is registered until the next trigger.

FANOUT and DELAY Registers.

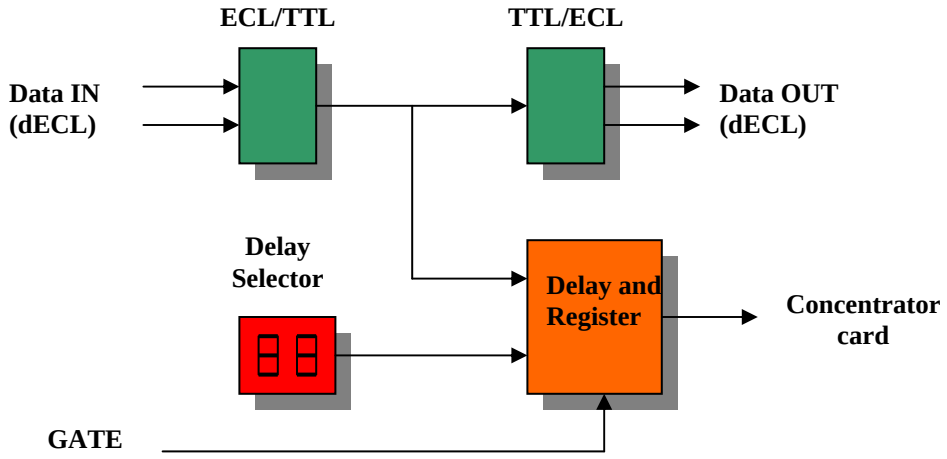
To receive all the 64 differential inputs from flat cables of 1,27mm spacing and still use a single 9U front panel a double connector was chosen from the KEL series. Each connector receives 16 dECL inputs and drives 16 dECL outputs, the 17th pair is connected to ground.

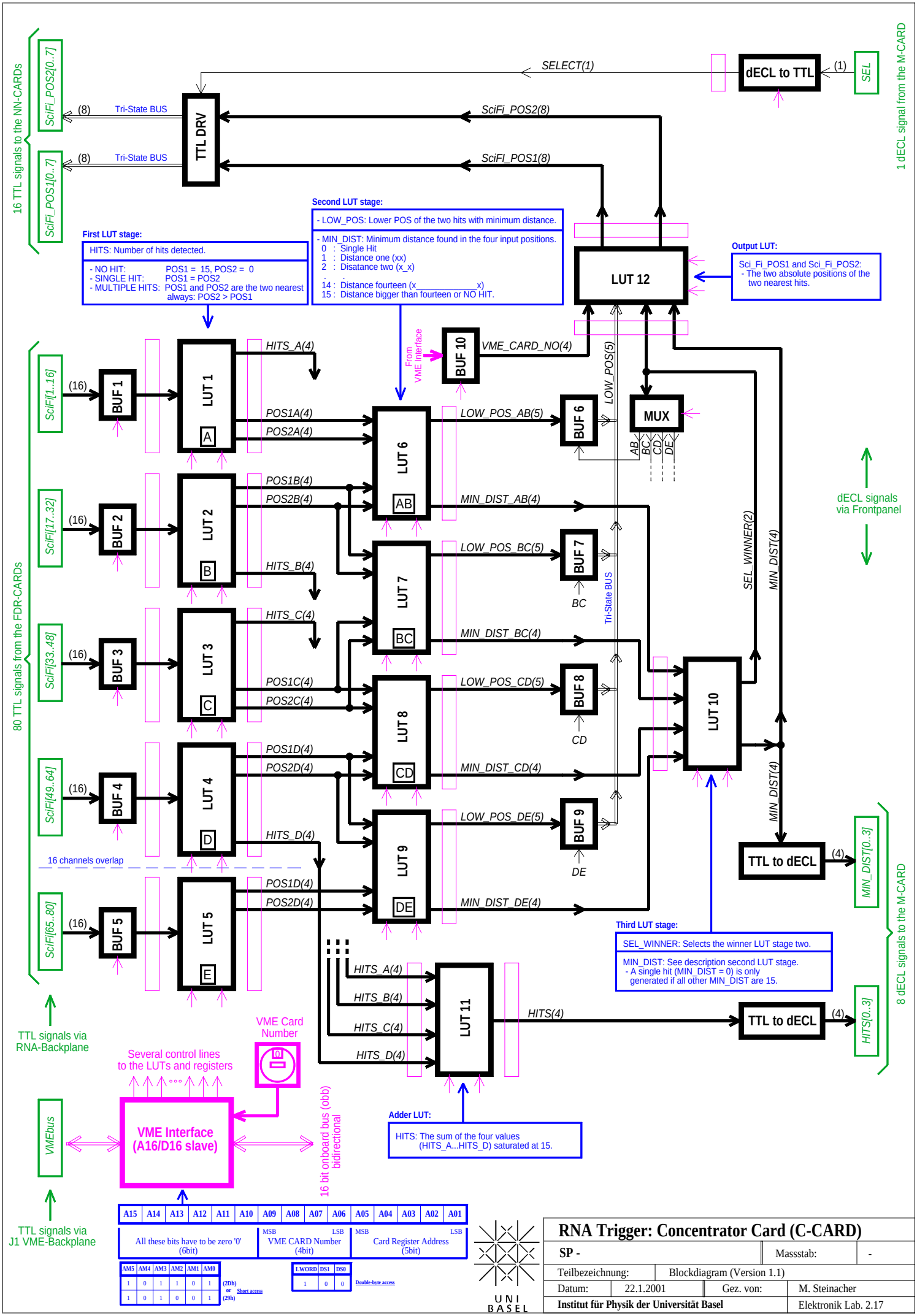
The signals arriving to the module are first converted to TTL prior to be latched on the Altera and fanout again to dECL levels for the next step of the electronics.

In the Altera the signals are delayed via a pipeline register with a programmable number of steps of 5ns and latched on the end of the trigger signal to be used by the Concentrator card. The programmable delay is selected via two BCD selectors placed on the front panel, one for the dozens and the second one for the units.

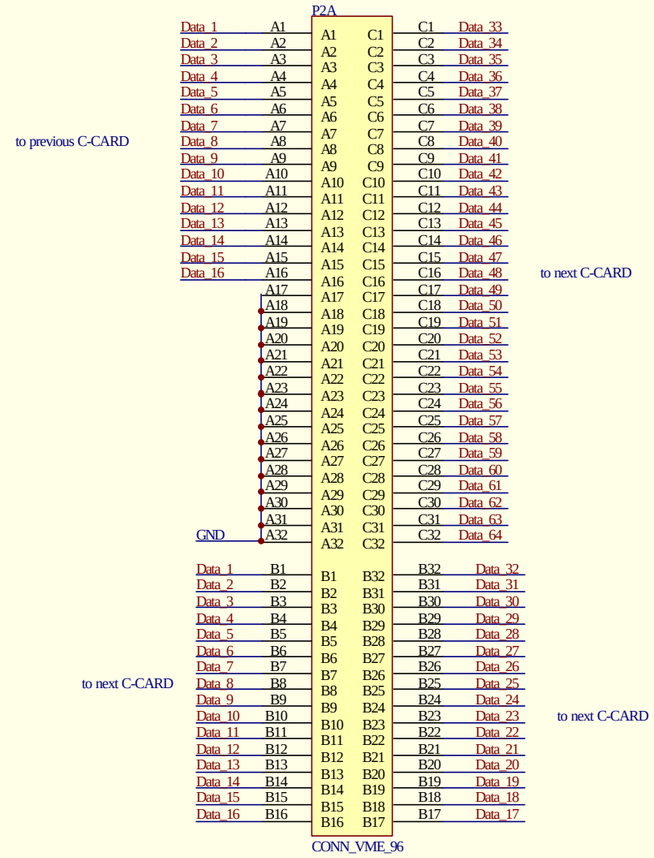
The registered signals are connected to the concentrator card via P2. Row B holds the first 32 signals and C the higher 32 data delayed and registered. On the a Row A a copy of the first 16 signals is buffered to independently. The remaining pins are connected to ground. Figure 1 shows a schematic description of the FDR.

Figure 1:



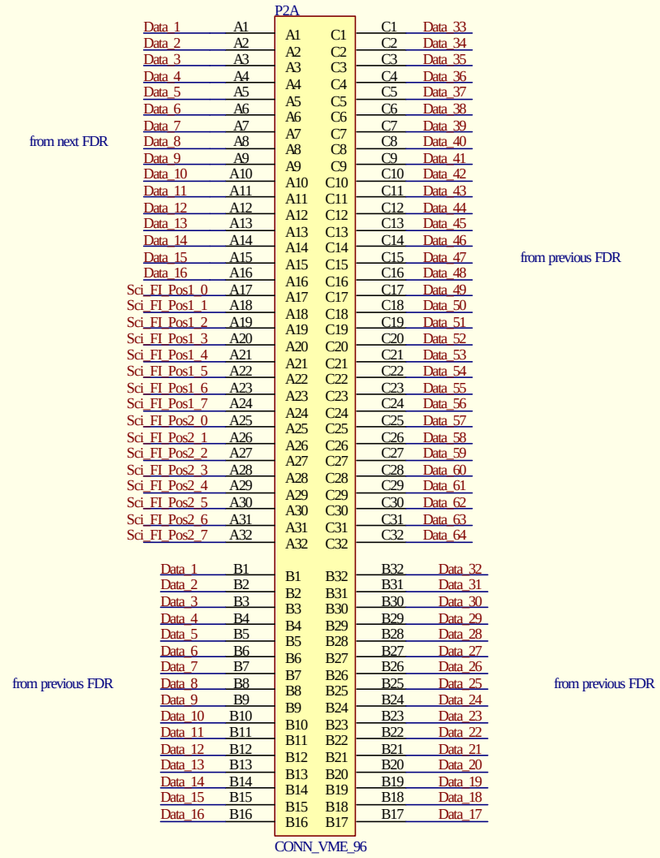

16 TTL signals to the NN-CARDs
SciFi_POS2[0..7]
SciFi_POS1[0..7]
(8)
Tri-State BUS
TTL DRV
SELECT(1)
dECL to TTL
(1)
SEL
1 dECL signal from the M-CARD
SciFi_POS2(8)
SciFI_POS1(8)
First LUT stage:
HITS: Number of hits detected.
- NO HIT: POS1 = 15, POS2 = 0
- SINGLE HIT: POS1 = POS2
- MULTIPLE HITS: POS1 and POS2 are the two nearest always: POS2 > POS1
Second LUT stage:
- LOW_POS: Lower POS of the two hits with minimum distance.
- MIN_DIST: Minimum distance found in the four input positions.
0 : Single Hit
1 : Distance one (xx)
2 : Disatance two (x_x)
14 : Distance fourteen (x_____x)
15 : Distance bigger than fourteen or NO HIT.
LUT 12
Output LUT:
Sci_Fi_POS1 and Sci_Fi_POS2:
- The two absolute positions of the two nearest hits.
From VME Interface
BUF 10
VME_CARD_NO(4)
LOW_POS(5)
80 TTL signals from the FDR-CARDs
SciFI[1..16]
SciFI[17..32]
SciFI[33..48]
SciFI[49..64]
SciFI[65..80]
(16)
BUF 1
BUF 2
BUF 3
BUF 4
BUF 5
LUT 1
LUT 2
LUT 3
LUT 4
LUT 5
A
B
C
D
E
HITS_A(4)
HITS_B(4)
HITS_C(4)
HITS_D(4)
POS1A(4)
POS2A(4)
POS1B(4)
POS2B(4)
POS1C(4)
POS2C(4)
POS1D(4)
POS2D(4)
16 channels overlap
LUT 6
LUT 7
LUT 8
LUT 9
AB
BC
CD
DE
LOW_POS_AB(5)
LOW_POS_BC(5)
LOW_POS_CD(5)
LOW_POS_DE(5)
BUF 6
BUF 7
BUF 8
BUF 9
MUX
AB
BC
CD
DE
Tri-State BUS
MIN_DIST_AB(4)
MIN_DIST_BC(4)
MIN_DIST_CD(4)
MIN_DIST_DE(4)
SEL_WINNER(2)
MIN_DIST(4)
LUT 10
TTL to dECL
(4)
MIN_DIST[0..3]
dECL signals via Frontpanel
Third LUT stage:
SEL_WINNER: Selects the winner LUT stage two.
MIN_DIST: See description second LUT stage.
- A single hit (MIN_DIST = 0) is only generated if all other MIN_DIST are 15.
8 dECL signals to the M-CARD
LUT 11
HITS(4)
TTL to dECL
(4)
HITS[0..3]
Adder LUT:
HITS: The sum of the four values (HITS_A...HITS_D) saturated at 15.
TTL signals via RNA-Backplane
VME Card Number
Several control lines to the LUTs and registers
VMEbus
VME Interface (A16/D16 slave)
16 bit onboard bus (obb) bidirectional
TTL signals via J1 VME-Backplane
A15 A14 A13 A12 A11 A10 A09 A08 A07 A06 A05 A04 A03 A02 A01
All these bits have to be zero '0' (6bit)
MSB VME CARD Number (4bit) LSB
MSB Card Register Address (5bit) LSB
AM5 AM4 AM3 AM2 AM1 AM0
1 0 1 1 0 1 (2Dh) or 1 0 1 0 0 1 (29h)
Short access
LWORD DS1 DS0
1 0 0
Double-byte access
UNI BASEL
RNA Trigger: Concentrator Card (C-CARD)
SP -
Massstab: -
Teilbezeichnung: Blockdiagram (Version 1.1)
Datum: 22.1.2001
Gez. von: M. Steinacher
Institut für Physik der Universität Basel
Elektronik Lab. 2.17

FDR P2 Connections



Text

C-CARD P2 Connections



Title	Connector definitions for FDR and C-Card		
Size: B	Number:	Revision:	
Date: 24-Jan-2001		Sheet 1 of 1	
File: F:\fdr.ddb		Drawn By: Jose DA SILVA	