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Third level trigger for DIRAC. Versions of implementation

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1 Introduction. Simulation results

The task of the 3-d level trigger is to suppress detection of pairs with a high value of the relative momentum Q_L. It has to provide further suppression after selection of pairs with the 1-st and 2-d level trigger criteria.

The input data for Trigger 3 are the numbers of hit elements in the vertical hodoscopes $V1, V2$ and the number of the ionization detector I element which detected the double ionization.

According to simulation a limitation to the Q_L value results in correlation between the numbers of $V1$ and $V2$ elements: for any I_i hit scintillator there exists a table of possible combinations of $V1$ and $V2$ elements (here and further when speaking about the hit in I, we mean the double ionization event). In other words, each hit $V1$ scintillator may be accompanied by any one of some group of $V2$ scintillators. The width and position (within the hodoscope) of this strip of $V2$ counters depend on Q_L cut and on the number of the hit I element. The picture of an event is shown in Fig.1. If the width of a scintillator in $V1$ and $V2$ is 70 mm and the condition $Q_L \leq 30$ Mev/c has to be fulfilled, then these groups are from 1–2 to 11 counters.

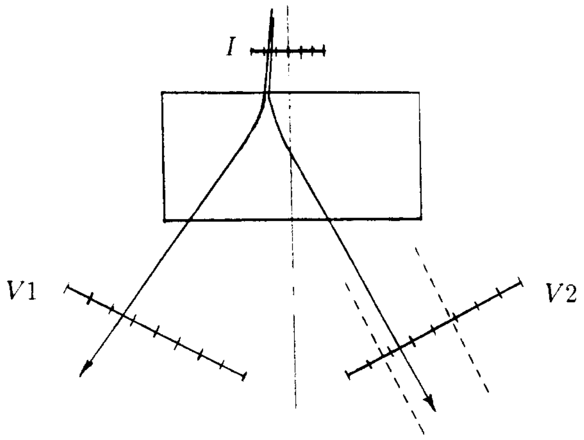

Fig.1. The picture of an event analysed by Trigger 3 scheme.

In Fig.2 there are shown the areas of permitted combinations of $V1$ and $V2$ hit counters at the condition $Q_L \leq 30$ MeV/c for different hit I scintillators.

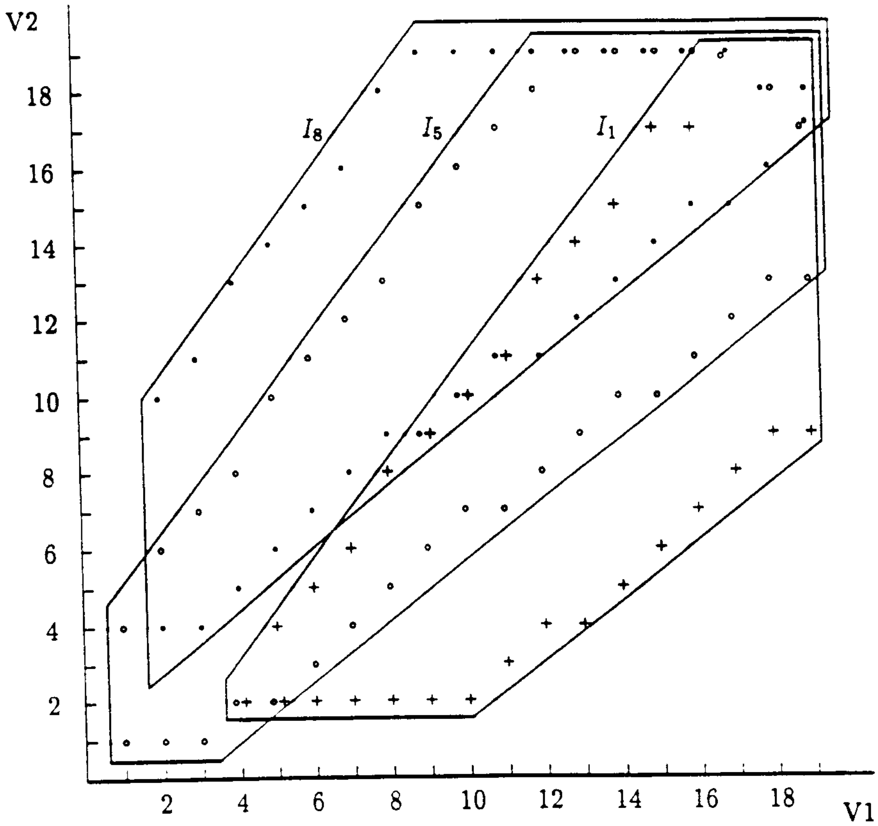

Fig.2. Permitted combinations of $V1$ and $V2$ counters for the 1-st, the 5-th and the 8-th hit elements in I (at 8-fold sampling of I). The crosses, circles and filled circles denote the extreme numbers of $V2$ counters corresponding to hits in I_1, I_5 and I_8, respectively.

The simulations have been done for different beam conditions. The rejection power and particle multiplicities in the detectors presented below are for 263 μ Ti target and $1.5 \cdot 10^{11}$ 1/spill beam intensity. Both real and accidental, within 20 ns resolution time, events from interactions in the target were taken into account. Background from the channel walls or radiation shield was not included in simulations.

The rejection coefficient of Trigger 3 has been calculated as 1.48 for the cut $Q_L \leq 30$ MeV/c, 19 $V1$ and $V2$ hodoscope scintillators of 70 mm width and 16 elements of 6.5 mm width in the ionization detector I. The probability for single particles to produce the double ionization was taken 5% except protons for which it was 10%. If not to use the information on the hit element number in I, then comparison of only $V1$ and $V2$ hit scintillator numbers provides a low reduction, around 1.15. So this simplified Trigger 3 would have no sense.

There was obtained the dependence of the rejection coefficient on ionization detector structure. While increasing the partition of I from N=1 to N=9 scintillator strips (of the same I total width), the rejection coefficient increases from 1.15 to 1.39. For N=12 it grows to 1.46, but more fine sampling of I (up to 16) almost does not add to a background suppression factor.

Another conclusion concerns the number of hits in the detectors. For the events selected by Trigger 1, a mean particle multiplicity in the ionization detector is 2.28, multiplicity of 2 corresponds to 78% events. When the Trigger 2 signal is produced, it may happen that more than one I element manifests on double ionization detected. The number of double (or less probable triple) positive decisions of I depends in a large extent on its performance in respect to separation of single and double ionization events. If there are 3 particles in I and two of them are close in space and produce a "true" double ionization signal, then the third particle may produce an additional double ionization signal due to Landau fluctuations.

Another reason of multiple positive decisions depends on the ionization detector logic. For example, if the I logic includes only a threshold for double ionization in two adjacent strips and assigns the decision to one of them (e.g. to the lower one), then the double ionization produced in a single strip #i results in two positive decisions from the outputs #i and #(i-1). This type of "false" double decisions can be removed by additional test for ionization in single strips. Nevertheless, 3 single ionization particles in 3 adjacent strips always produce two positive decisions as well as some of those events where a double ionization hit in a single strip is accompanied by a single ionization hit in an adjacent strip.

The multiplicity of positive decisions of I influences the rejection power. The rejection coefficient 1.48 given above has been obtained in conditions when the probability of more than 1 positive decision in I was calculated to be 11%. If there were only 2 particles in the ionization detector then this probability would be 3% and the rejection coefficient increases to 1.63. So we should try to avoid at least "false" double decisions in Trigger 2 scheme for better rejection on the Trigger 3 step.

The multiplicity greater than 1 in the vertical hodoscopes occurs in 8% events in $V1$ and in 5% in $V2$. The patterns of $V1$ and $V2$ entered the rejection calculations with their real multiplicities.

The Trigger 3 scheme is activated by the Trigger 2 signal. The logic of Trigger 2 involving the scintillating fibre and ionization detectors is not fixed at the moment. One of possibilities under consideration is that the 2-d level trigger is worked out as OR of decisions of the scintillating fibre and ionization detectors. In this case if there is the signal of the SciFi detector but there is no that of the ionization one, then the Trigger 3 scheme could confuse because of the lack of input I data. To avoid this the Trigger 3 stage has to be skipped if there is no signal of the ionization detector. Amount of this type events is low, so this will not result in a large increase of data to be processed in the Trigger 4 scheme. It is assumed below that the signal of I is always present at the input of the Trigger 3 scheme.

The optimum way of hardware implementation of Trigger 3 would be development of a dedicated electronic scheme. Nevertheless, it seems feasible to realize it with commercially available modules. Two versions of such implementation are considered in this note.

2 Universal logic module version

This version is based on LeCroy 2366 Universal Logic Module (ULM). ULM is a CAMAC module using completely programmable logic array technology. There are 59 front panel ECL signals which can be independently selected to be either inputs or outputs. The desired logical operations are programmed in a Xilinx 4005 gate array chip. There is a lot of hard and soft macros (like adders, counters, registers etc.) available in the library for Xilinx programming which helps to create a complicated schematics.

A powerful hardware of the 2366 module and the supporting software make possible to realize the Trigger 3 scheme in different ways. Here we describe one of possibilities.

At first let us consider a simplified case, when only one element of the ionization detector is involved in triggering. Then there is only one table of correspondence: each $V1$ element has to be matched with a group of relevant $V2$ elements. A trigger scheme for this case is shown in Fig.3.

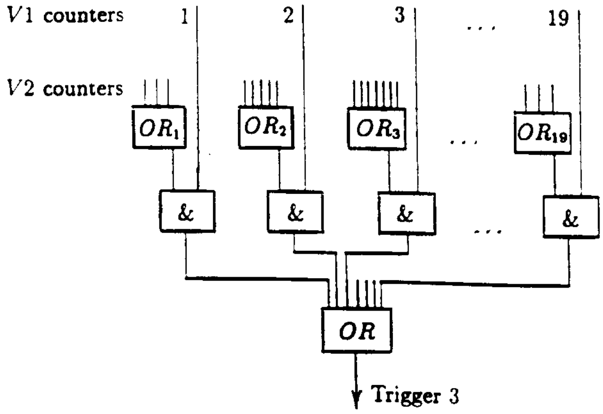

Fig.3. Trigger scheme for only one ionization detector element included.

If there are many ionization detector elements, say N, then the number of combinations increases but not as much as N times. From Fig.2 it is seen that the shape of "good combination" area is similar for different I_i, this area only shifts along the $V1$ axis with changing of I_i. This could essentially decrease a total number of $V2$ counter groups. From Fig.2 one can see that, for example, the same group of #5–#15 counters in $V2$ corresponds simultaneously to $V1_{14}$ and I_1 or $V1_9$ and I_5 or $V1_5$ and I_8. This peculiarity, in principle, may be used for development of a dedicated resource-saving scheme.

Nevertheless, we prefer to use less resource-saving but clear and uniformly structured scheme as far as the chip resources are sufficient for its realization. It consists of blocks like shown in Fig.3 repeated N times, where N is the number of I elements. The scheme is shown in Fig.4 for the case N=9. The tables of correspondence between $V1$ and $V2$ element numbers are included for all I channels, thus the inputs of OR_i^k receiving $V2$ signals are specified for every $V1_i$ and I_k element. The & schemes make coincidences of

$V1_i$ and I_k counters with a corresponding OR_i^k group of $V2$, the number of & schemes equals the product of total numbers of $V2$ and I channels. Their final OR is a Trigger 3 signal.

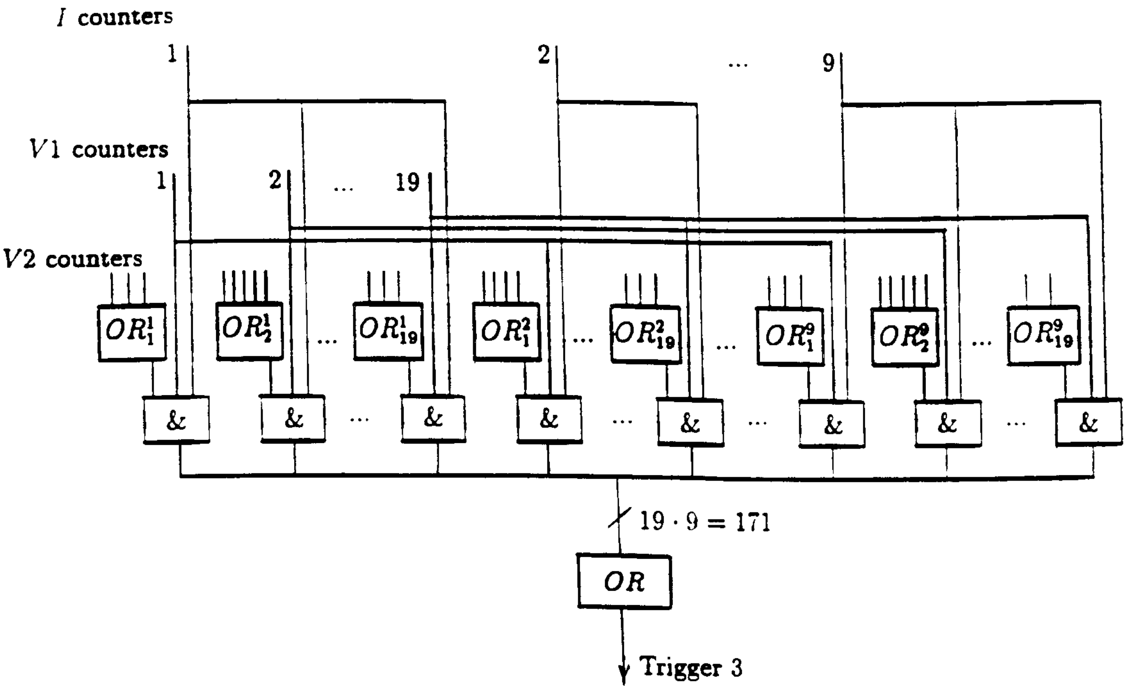

Fig.4. Trigger scheme on the base of Universal Logic Module.

All OR functions may be realized with the chip programmable interconnections. The coincidences are made with configurable logic blocks (CLB). For 19 channels in each of $V1$ and $V2$ and 9 channels in I there will be used around 1700 gates, 90 CLBs and 50 input/output blocks out of, respectively, 5000, 196 and 112 available in the Xilinx 4005 chip. Thus even 16 channel sampling of the ionization detector seems feasible to be implemented.

The delay of the scheme is defined by propagation delays of different subsystems of the chip architecture. It is very short and is estimated to be less 50 ns.

3 Memory lookup version

The selection of permitted combination of hits in $V1$, $V2$ and I hodoscopes is realized in this case with the LeCroy 2373 Memory Lookup Unit (MLU) modules. The module has 16 ECL inputs and 16 ECL outputs thus providing as many as 2^{16} combinations of input signals programmed to produce the corresponding output codes.

The number of inputs in the 2373 module is insufficient to recieve the signals from the elements of all three detectors directly. To overcome this, the patterns of $V1$ and $V2$ hodoscopes may be converted to a binary form before coming to MLU. Then $V1$ and $V2$

occupy each by 5 bits and there are 6 bits available for the I signals. The number of the MLU modules depends on the number of I elements to be implemented: as one modules has 6 inputs available, there are needed 2 modules for 12-fold sampling of I or 3 modules for 16-fold one. Below we consider the 12-fold sampling case.

For conversion to a binary code the priority encoders have to be used to handle the multihit events. The priority encoder is an encoder which serially produces at its output the codes corresponding to every non-zero input bit. These devices may be realized on the base of 2366 Universal Logic Module. The number of input/output connections available with 2366, equal to 59, is sufficient for $V1$ and $V2$ detectors: there are 19+19=38 input signals and 5+5=10 bits of the output binary codes. Taking into account that the pins of ULM connectors may be programmed as outputs or inputs in groups of 4, a total number of pins occupied by $V1$ and $V2$ is 52.

The total scheme operates as follows (Fig.5). The patterns of $V1$ and $V2$ are latched in the input registers of the Universal Logic Module by the Trigger 2 signal. UML is programmed as two priority encoders with an additional control net. The output codes of UML are fan-outed to be sent to two Memory Lookup Units. The pattern of I is divided into two parts, one is going to the first MLU, the another part to the second one. The first codes of $V1, V2$ priority encoders and the I pattern come to 2373 MLUs which are programmed to select the permitted combinations of $V1, V2$ and I signals. If the result of the check is positive then one of MLU (or sometimes both) gives the Trigger 3 signal and further processing of the event within this scheme is blocked. In opposite case the next code (if exists) of $V1$ priority encoder appears to be compared in MLUs with unchanged codes of $V2$ and I. If again there was no Trigger 3 signal, the process is repeated with the second (if exists) code of $V2$ priority encoder and every of $V1$ codes (latching of the input patterns in registers makes it possible to repeat $V1$ encoding from the beginning). A proper timing and the sequence of codes can be ensured with a relevant control signal network in 2366 UML and an appropriate choice of the clock frequency.

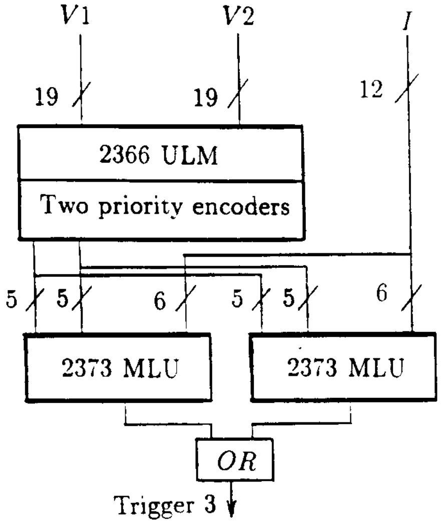

Fig.5. Trigger scheme based on Memory Lookup Unit.

The input-output delay of the scheme depends on the number of hit elements in $V1$ and $V2$. The ULM delay is estimated as 40 ns, that of MLU is 45 ns. Thus, for one particle in each hodoscope the delay between Trigger 2 and Trigger 3 is less 100 ns. For two particles in each hodoscope the maximum delay is around 250 ns (when a good combination happened to be the last one).

4 Comparison of versions

Both versions presented seem feasible for implementation but have their own specific points.

The advantages of the Universal Logic Module version are: 1) its compactness: only one 2366 module is needed; 2) there are no limitations on multiplicity in any of $V1, V2, I$ detectors as all combinations are checked simultaneously; 3) the input/output delay is very short and independent on multiplicity.

But the programming of the Xilinx chip is not a trivial job. Hence it could be not very simple to change the selection criteria if one has to reprogram the chip for this reason. Probably one can avoid reprogramming if the programmme is arranged so that the map of the chip interconnections for all OR schemes is loaded in the form of a separately prepared file.

The Memory Lookup Unit version demands more modules: two 2373 MLU (or three for 16-fold I sampling) and one 2366 ULM. The program written to a chip of 2366 UML is a fixed code with a function of the priority encoder. There is no need to vary the program in the Xilinx chip if the selection criteria are changed. This change can be done in 2373 MLU which programming raises no problems.

The choice of the version can be done on further study, especially on programming aspects.