UNIVERSIDADE FEDERAL DO RIO DE JANEIRO
INSTITUTO DE FÍSICA

Tese de Doutorado

Spontaneous R Parity Violation Measurement at DELPHI & CARIOCA - A New Front-end Electronic for the LHCb Muon Detector

Danielle Magalhães Moraes

Orientador: Leandro S. de Paula

Rio de Janeiro, 11 de Abril de 2002

Aos meus pais,

meu irmão e

ao Fernando,

pela força de sempre.

"*Deus quer. O homem sonha. A obra nasce.*"

Fernando Pessoa

Resumo

Um dos modelos alternativos ao Modelo Padrão Supersimétrico Mínimo considera a paridade R como uma simetria da lagrangiana, que é violada ao se impor um valor esperado no vácuo não nulo para neutrinos escalares. Neste cenário, o decaimento do chargino pode ocorrer através de um novo processo: $\tilde{\chi}^+ \rightarrow \tau^+ J$. Neste trabalho, os efeitos da violação espontânea da paridade R, em particular, o decaimento $\tilde{\chi}^+ \rightarrow \tau^+ J$ são estudados usando-se os dados de colisões e^+e^- coletados pelo detetor DELPHI durante os anos de 1997 à 2000. Estes dados correspondem a uma luminosidade integrada de aproximadamente $654\,\mathrm{pb}^{-1}$, na faixa de energia de centro de massa entre 183 GeV e 208 GeV. Como resultado desta análise nenhum decaimento foi encontrado, evidenciando a não violação espontânea da paridade R no decaimento de charginos produzidos com uma seção de choque maior que 0.14 pb e massa menor ou igual a 103.8 GeV/c^2.

CARIOCA é uma eletrônica de *front-end* rápida e de baixo ruído, que foi projetada para leitura de Câmaras Proporcionais Multifilares. Este circuito integrado consiste em amplificador de corrente, *shaper*, discriminador e *driver* LVDS, para leitura anódica e catódica, implemetado na tecnologia de $0.25\,\mu$m CMOS. Esta tese apresenta uma decrição detalhada do CARIOCA, bem como os resultados obtidos com os protótipos.

Abstract

Searches for spontaneous R-parity violating signals, under the assumption of R-parity breaking in the third lepton family, at centre-of-mass energies from 183 GeV up to 208 GeV have been performed using the DELPHI data collected during 1997 and 2000. The expected topology for the decay of a pair of charginos

into two acoplanar taus plus missing energy, $\tilde{\chi}^+ \rightarrow \tau^+ J$, was investigated and no evidence for a signal was found. A limit on the chargino mass of 103.8 GeV/c was found and allowed domains of the MSSM parameter space were derived.

CARIOCA is a very fast and low noise front-end chip developed for Multi Wire Proportional Chambers readout. This circuit is an amplifier, shaper, discriminator and LVDS driver chip, for both anode and cathode readout, implemented in 0.25 μm CMOS radiation tolerant technology. Its novelty lies in the current-mode amplifier circuit, which is of new conception. In this thesis I report on the CARIOCA design and prototypes test results.

Contents

Parte I

Introdução

Capítulo 1

Introdução

O trabalho na área de física de altas energias envolve diferentes etapas. Para testar os modelos que descrevem as interações das partículas elementares é necessário a construção de aceleradores, capazes de fazer colidir partículas com energia de centro de massa elevada, e de detetores que possam estudar o resultado destas interações. A análise e o processamento dos sinais dos detetores exige uma eletrônica rápida, para satisfazer os níveis de *trigger*, compacta para facilitar a integração do aparato experimental, e muitas vezes resistente a radiação resultante das interações das partículas. Por isto torna-se necessário, em muitos casos, o desenvolvimento de novas tecnologias e técnicas de deteção. Projetar e construir um detetor é uma tarefa que demora em média oito anos. Em uma tese de doutorado não há tempo hábil para acompanhar o trabalho de desenvolvimento e construção de um detetor, e ainda participar da análise dos dados deste detetor. Por este motivo, resolvi trabalhar em mais de um experimento, podendo assim acompanhar as diversas fases da construção de um detetor e desenvolver análise de dados.

Durante os últimos 20 anos, grande parte do trabalho de Física Experimental de Altas Energias consistiu em projetar, construir e operar experimentos capazes de testar a validade do Modelo Padrão[1] [1], e suas possíveis extensões [2]. Apesar do sucesso na descrição dos dados experimentais obtidos pelos aceleradores LEP [3], SLC [4], Tevatron [5] e outros, o Modelo Padrão deixa em aberto muitas questões fundamentais da física de partículas [6]. Uma destas questões é a ausência de explicação para a existência de 3 gerações de férmions. Além disto, este modelo possui parâmetros colocados "ad hoc", tais como os existentes na matriz de Cabibbo-Kobayashi-Maskawa [7], e não representa exatamente uma unificação das interações eletromagnéticas e fracas, uma vez que ele possui duas constantes de acoplamento distintas. Por estas razões, acredita-se que este modelo não seja uma teoria fundamental da natureza mas sim um modelo efetivo válido em baixa escala de energia.

A teoria supersimétrica [8] foi utilizada para construir possíveis extensões do Modelo Padrão. Esta teoria prevê a existência de partículas supersimétricas que diferem dos seus parceiros do Modelo Padrão por 1/2 unidade de spin. Dentre os diversos modelos supersimétricos existentes, o mais simples é o Modelo Supersimétrico Mínimo (MSSM) [8]. Neste modelo todos os férmions do Modelo Padrão possuem parceiros supersimétricos - sléptons, sneutrinos e squarks. Os parceiros supersimétricos dos campos de calibre neutros e dos bósons de Higgs neutros - $\tilde{\gamma}$, $\tilde{Z}^0$, $\tilde{H}_1^0$ e $\tilde{H}_2^0$ - se misturam dando origem aos gauginos neutros, cujos autoestados de massa são chamados neutralinos ($\tilde{\chi}_i^0$, $i = 1, 4$). O mesmo acontece com os parceiros supersimétricos dos bósons de calibre e dos bósons de Higgs carregados - $\tilde{W}^\pm$ e $\tilde{H}^\pm$ - que se misturam dando origem aos gauginos carregados, cujos autoestados de massa são os charginos ($\tilde{\chi}_i^\pm$, $i = 1, 2$).

O Modelo Supersimétrico Mínimo introduz um novo número quântico: a paridade R definida como $R = (-1)^{L+3B+2S}$, onde L é o número leptônico, B é o número bariônico e S é o spin da partícula. Este número quântico foi construído de maneira tal que as partículas do Modelo Padrão possuem $R = +1$ e os seu

[1] O Modelo Padrão é a teoria atualmente aceita para descrever as interações das partículas elementares.

parceiros supersimétricos $R = -1$. Sendo assim, se a paridade R for conservada as partículas supersimétricas só podem ser produzidas aos pares e a partícula supersimétrica mais leve tem que ser estável. No contexto do MSSM, não há uma previsão da conservação ou violação desta simetria. Modelos alternativos onde a paridade R é violada explicitamente tem sido bastante estudados [9].

Alguns modelos descrevem o caso em que a paridade R é uma simetria da lagrangiana e pode ser violada espontâneamente [10]. Esta simetria é violada ao se impor um valor esperado no vácuo não nulo para neutrinos escalares, o que dá origem a neutrinos massivos. Na ausência de qualquer simetria de calibre adicional, isto leva a existência de um bóson de Goldston sem massa, o Majoron (J), que seria a partícula supersimétrica mais leve. Neste caso, as partículas supersimétricas podem ser produzidas individualmente. Introduzindo a violação da paridade R somente na 3ª geração, o decaimento do chargino pode ocorrer através do processo de três corpos, como nos modelos em que há conservação da paridade R, ou através de um novo modo: $\tilde{\chi}^+ \to \tau^+ J$.

Medidas experimentais do espectro de partículas supersimétricas tem sido obtidas utilizando dados de diversos detetores. Estas medidas incluem a procura de sférmions assumindo a conservação da paridade R e um estudo do efeito da violação explicita da paridade R. Até o presente momento não existe nenhum estudo dos efeitos da violação espontânea da paridade R em dados experimentais. Nesta tese apresento a procura por sinais de violação espontânea da paridade R, em particular, a procura pelo decaimento $\tilde{\chi}^+ \to \tau^+ J$, usando os dados de colisões e^+e^- do LEP com energia de centro de massa entre 183 GeV e 208 GeV e luminosidade integrada de aproximadamente 654 pb^{-1}. Este dados foram coletados pelo detetor DELPHI [11], um dos quatro experimentos do LEP, durante os anos de 1997 e 2000.

O trabalho de desenvolvimento de uma nova tecnologia para o processamento de sinais de uma câmara proporcional multifilar foi realizado no âmbito da colaboração LHCb. O LHCb [12] é um dos detetores do colisor de prótons LHC [13], que está sendo construído no CERN, e deverá começar a funcionar a partir do ano de 2006. A proposta do LHCb é determinar os parâmetros da violação de CP, estudar os decaimentos raros do méson B e, como consequência, investigar a possibilidade da existência de uma nova física além do Modelo Padrão. Este detetor é dividido em diversos subdetetores. A tecnologia a ser empregada em cada subdetetor do LHCb está em fase de desenvolvimento e aprovação; em alguns casos a fase de construção já começou. O sistema de múons do LHCb será equipado com câmaras proporcionais multifilares (MWPC) e detetores de placas resistivas (RPC). Estas câmaras precisam ter uma boa eficiência e um tempo de resposta rápido para poder satisfazer o nível zero do *trigger* de múons ($\sim 3.2\,\mu$s).

Durante o estágio de desenvolvimento das MWPCs, diversas propostas para a eletrônica de *front-end* foram testadas, mas nenhum chip existente apresentou desempenho aceitável, por não atender aos requerimentos do sistema de múons e satisfazer a condição de ser resistente a elevadas doses de radiação. Por isto, tornou-se necessário o desenvolvimento de um chip específico. Este circuito integrado, que recebeu o nome de CARIOCA (*CERN and RIO Current Amplifier*) foi desenvolvido por mim no âmbito do projeto RD49 [14], responsável pelo estudo de circuitos integrados resistentes a radiação para o acelerador LHC. CARIOCA é um amplificador de corrente de alta velocidade e baixo ruído, projetado na tecnologia de $0.25\,\mu$m CMOS com a possibilidade de um ganho variável, o que permite a sua utilização tanto em detetores de silício quanto gasosos. A tecnologia de $0.25\,\mu$m CMOS foi escolhida para este desenvolvimento, pois mostrou-se resistente a elevadas doses de radiação e capaz da integração de circuitos em uma pequena área de silício, o que diminui o custo de produção. Além disto, esta tecnologia é relativamente nova e deverá ser adotada pela maioria dos experimentos de física de altas energias. A combinação desta tecnologia com a técnica de amplificação de corrente via espelhos de corrente, resultou num ótimo desempenho do circuito.

Na primeira parte da tese discuto a procura por sinais de violação espontânea da paridade R, bem como seus resultados. Na segunda parte, descrevo o desenvolvimento e a caracterização do CARIOCA, uma eletrônica de *front-end* rápida e resistente a radiação, que será utilizado pelo sistema de múons do LHCb.

Esta será uma das primeiras teses de doutorado da colaboração LHCb, apresentando de forma detalhada o desenvolvimento do chip CARIOCA. Neste trabalho também é descrita a procura inédita por efeitos da violação espontânea da paridade R em dados de colisões e^+e^-. Ambos os trabalhos foram desenvolvidos no âmbito de colaborações internacionais e por isto solicitei uma autorização para escrever a tese na lingua inglesa. Isto facilitará a utilização da tese por membros das colaborações, bem como por estudantes, fazendo com que a mesma seja utilizada como referência por um maior número de pessoas.

Parte II

Medida da Violação Espôntanea da Paridade R no DELPHI

Chapter 2

Supersymmetry and Spontaneous R-Parity Violation

2.1 Introduction

Standard Model (SM) [1] is the theory accepted to describe the elementary particles and their interactions. It is a Yang-Mills theory, based on the symmetry group $\mathrm{SU}_c(3) \otimes \mathrm{SU}_L(2) \otimes \mathrm{U}_Y(1)$. In the last years powerful tests of the SM have been performed at LEP, SLC and Tevatron. The experiments at the Z resonance have enormously improved the accuracy of measurements in the electroweak neutral current sector. The top quark has been found and the errors on m_Z and $\sin^2\theta_{eff}$ [15] went down by two and one order of magnitude, respectively, since the start of LEP in 1989. It has been checked that the coupling of quarks and leptons to the weak gauge bosons $\mathrm{W}^{\pm}$ and Z is indeed as precisely as prescribed by the gauge symmetry. The high accuracy (few 0.1 %) for these tests implies that, not only tree level, but also the structure of quantum corrections has been verified.

In the SM one single scalar Higgs isospin is introduced and its vacuum expectation value breaks the symmetry, generating the mass of quarks and leptons [1].

The Higgs mechanism is still largely untested and no Higgs particle has been found. The limit on the Higgs mass is $114.1\,\mathrm{GeV/c^2}$ at the $95\,\%$ confidence level [16]. If the Higgs coupling are removed from the SM Lagrangian, the resulting theory is non renormalizable and a cutoff must be introduced.

Although the SM has been very success in describing the experimental data, this theory leaves lots of open questions [6]. It can neither explain why there are three lepton families, nor the relative smallness of the weak scale mass at $\mu \sim 1/\sqrt{G_F} \sim 250\,\mathrm{GeV}$, with $G_F = g^2/(8M_W^2)$ being the Fermi coupling constant. As well as the proliferation of parameters, such as the fermions mass and the CKM matrix [7]. At present it is highly implausible that the origin of the electro-weak symmetry breaking can be explained by the standard Higgs mechanism, without accompanying new phenomena. This conclusion follows from the extrapolation of the SM at very high energies (TeV domain).

Extensions of the SM, such as evaluation of the couplings as a function of energy, points toward the unification of the electro-weak and strong forces (Grand Unified Theories: GUT) at energy scales $M_{GUT} \sim 10^{14} - 10^{16}\,\mathrm{GeV}$, which are close to the scale of quantum gravity ($M_{Pl} \sim 10^{19}\,\mathrm{GeV}$) [17]. A unified theory of all interactions including gravity (Superstrings) can also be considered [18]. One of the most attractive extensions of the SM is Supersymmetry (SUSY). There are alternative models for SUSY, as for example Technicolor theories [19], that are inspired by the break of chiral symmetry in massless QCD induced quark condensate.

2.2 Supersymmetry

Supersymmetry (SUSY) is one of the most attractive possible extensions of the SM and its signature could be investigated at LEP2 through different channels. One of the virtues of extending Standard Model using supersymmetry is that a new spectrum of particles and the mechanism of electroweak symmetry breaking occurs at the level of perturbation theory, without the need of any new strong interaction. It legitimizes the introduction of Higgs scalar fields and naturally gives rise to the mechanism of electroweak symmetry breaking [8].

In supersymmetry the cutoff is replaced by the splitting between the normal particles and their supersymmetric partners. This splitting times the size of the weak gauge couplings is of the order of the weak scale mass. In this case the mass of most supersymmetric particles would fall, partially, in the discovery reach of the LHC. There are some consistent formulated theories on the basis of this idea. The simplest one is the Minimal Supersymmetric Standard Model (MSSM) [8].

2.2.1 Minimal Supersymmetric Standard Model

The Minimal Supersymmetric Standard Model (MSSM) adds a minimal set of supersymmetric partner fields to the SM. In this model, each of the known fundamental particles must be in either a chiral or a gauge supermultiplet and have a partner with spin differing by 1/2 unit. The spin-0 partners of the quarks and leptons are called squarks and sleptons and the symbols are the same as for the corresponding fermion, but with a tilde used to denote the superpartner of a SM particle, as shown in Table 2.1. The gauge interactions of the squarks and sleptons field are the same as for the corresponding SM fermion. The left- and right-handed chiral states of each SM fermion, f_L and f_R, have as SUSY partners two scalars, $\tilde{f}_L$ and $\tilde{f}_R$. The fermionic partners of the SM Higgs scalars are called higgsinos.

The electroweak gauge symmetry $\mathrm{SU}_L(2), \otimes \mathrm{U}_Y(1)$ has associated with it spin-1 gauge boson (W^+, W^0, W^- and B^0) with spin-1/2 superpartners ($\tilde{W}^+$, $\tilde{W}^0$, $\tilde{W}^-$ and $\tilde{B}^0$), called winos and bino respectively. After electroweak symmetry breaking, the W^0, B^0 gauge eigenstates mix to give mass eigenstates Z^0 and γ. The corresponding gaugino mixtures of $\tilde{W}^0$ and $\tilde{B}^0$ are called zino ($\tilde{Z}^0$) and photino ($\tilde{\gamma}$). If supersymmetry were unbroken, these eigenstates would be mass

Names		spin 0	spin 1/2	$SU_C(3)$, $SU_L(2)$, $U_Y(1)$
squarks, quarks	Q	$(\tilde{u}_L\ \tilde{d}_L)$	$(u_L\ d_L)$	$(3,\ 2,\ \frac{1}{6})$
(x 3 families)	$\bar{u}$	$\tilde{u}^*_R$	$u^\dagger_R$	$(\bar{3},\ 1,\ -\frac{2}{3})$
	$\bar{d}$	$\tilde{d}^*_R$	$d^\dagger_R$	$(\bar{3},\ 1,\ \frac{1}{3})$
sleptons, leptons	L	$(\tilde{\nu}\ \tilde{e}_L)$	$(\nu_L\ e_L)$	$(1,\ 2,\ \text{-}\frac{1}{2})$
(x 3 families)	$\bar{e}$	$\tilde{e}^*_R$	$e^\dagger_R$	$(1,\ 1,\ 1)$

Table 2.1: Chiral supermultiplets in the Minimal Supersymmetric Standard Model.

eigenstates with masses m_Z and 0. The gauge supermultiplets are summarized in Table 2.2.

In the MSSM there are four neutralinos, $\tilde{\chi}^0_i$, $i = 1, 4$, and two charginos $\tilde{\chi}^\pm_i$, $i = 1, 2$, which are linear combinations of the SUSY partners of neutral and charged gauge and Higgs boson (gauginos and higgsinos). Charginos could be pair produced at LEP via s-channel Z/γ exchange or via t-channel exchange of a sneutrino. The neutralino could be pair production via e^+e^- annihilation into Z or through t-channel selectron exchange. The t-channel contribution is important if the slepton is light. Signatures of chargino and neutralino production in e^+e^- annihilation are discussed in References [20, 21].

When supersymmetry is broken in the TeV range, $SU_L(2) \otimes U_Y(1)$ remains intact and only the s-partners take mass while all normal particles remain massless. Only at the lower weak scale the masses of ordinary particles are generated.

The MSSM Lagrangian conserve R-parity

$$R_P = (-1)^{3B+L+2S} \tag{2.1}$$

where B is the baryon number, L is the lepton number and S is the particle spin. The R-parity is a discrete symmetry constructed so that $R_P = +1$ for the conventional gauge boson, quark, lepton and Higgs state while $R_P = -1$ for their supersymmetric partners. If R_P is exactly conserved, supersymmetric

Names	spin 1	spin 1/2	SU(3)$_C$, SU$_L$(2), U$_Y$(1)
gluon, gluino	g	$\tilde{g}$	(8, 1, 0)
W bosons, winos	$W^{\pm}$ W^0	$\tilde{W}^{\pm}$ $\tilde{W}^0$	(1, 3, 0)
B bosons, bino	B^0	$\tilde{B}^0$	(1, 1, 0)
	spin 0	spin 1/2	
Higgs, higgsinos	$(H_u^+ \; H_u^0)$	$(\tilde{H}_u^+ \; \tilde{H}_u^0)$	(1, 2, $+\frac{1}{2}$)
	$(\tilde{H}_d^+ \; \tilde{H}_d^0)$	$(\tilde{H}_d^+ \; \tilde{H}_d^0)$	(1, 2, -$\frac{1}{2}$)

Table 2.2: Gauge and Higgs supermultiplets in the Minimal Supersymmetric Standard Model.

particles can only be produced in pairs, and the lightest SUSY particle must be absolutely stable. These features underly most of the experimental searches for supersymmetric states.

2.3 Spontaneous R-Parity Violation

One alternative supersymmetric scenario is to consider the R-parity as an exact Lagrangian symmetry, broken spontaneously through the Higgs mechanism [22]. This may take place via non-zero vacuum expectation values (VEVs) for scalar neutrinos, such as for the scalar tau-neutrinos

$$v_R = \langle \tilde{\nu}_{R\tau} \rangle \; ; \quad v_L = \langle \tilde{\nu}_{L\tau} \rangle \; . \tag{2.2}$$

In this case there are two main scenarios depending on whether the lepton number is a gauge symmetry or not [23–26]. In the absence of an additional gauge symmetry, it leads to the existence of a physical massless Nambu-Goldstone boson, called the Majoron (J) [10]. In this context the Majoron remains massless and therefore stable provided that there are no explicit R-parity violating terms.

In the present work we consider the simplest model for spontaneous R-parity violation proposed in References [10,24]. In this model the Lagrangian is specified by the superpotential

$$W = W_1 + h_\nu \nu^c L\mathrm{H}_u + h\Phi\nu^c \mathrm{S} + h.c. \tag{2.3}$$

that conserves the total lepton number and R-parity. The first part of this equation contains the basic MSSM superpotential terms, including an isosinglet scalar Φ with a linear superpotential coupling, written as:

$$W_1 = h_u Q u^c \mathrm{H}_u + h_d Q d^c \mathrm{H}_d + h_e e^c L\mathrm{H}_d + (h_0 \mathrm{H}_u H_d - \mu'^2)\Phi \ . \tag{2.4}$$

The couplings h_u, h_d, h_e, h_ν, h_0, h are described by arbitrary matrices in the generation space and explicitly break flavor conservation. The additional chiral superfields ν^c, S [27] and Φ [28] are singlets under $\mathrm{SU}_L(2) \otimes \mathrm{U}_Y(1)$ and carry a conserved lepton number assigned as -1, 1 and 0, respectively. These superfields may induce the spontaneous violation of R-parity, given by the imaginary part of:

$$\frac{v_L^2}{V v^2}(v_u \mathrm{H}_u - v_d \mathrm{H}_d) + \frac{v_L}{V}\tilde{\nu}_\tau - \frac{v_R}{V}\tilde{\nu}^c_\tau + \frac{v_S}{V}\tilde{\mathrm{S}}_\tau \ , \tag{2.5}$$

leading to an R-odd Majoron. The isosinglet VEVs $v_R = \langle \tilde{\nu}_{R\tau} \rangle$ and $v_S = \langle \tilde{S}_\tau \rangle$, with $V = \sqrt{v_R^2 + v_S^2}$, characterize the R-parity breaking. The isodoublet VEVs $v_u = \langle H_u \rangle$ and $v_d = \langle H_d \rangle$ induce the electroweak breaking and generate the fermion masses with the combination $v^2 = v_u^2 + v_d^2$ being fixed by the W and Z masses. There is a small seed of R-parity breaking in the double sector $v_L = \langle \tilde{\nu}_{L\tau} \rangle$, whose magnitude is related to the Yukawa coupling h_ν.

The form of the chargino mass matrix

$$\begin{array}{c|ccc} & e_j^+ & \tilde{H}_u^+ & -i\tilde{W}^+ \\ \hline e_i & h_{eij} v_d & -h_{\nu ij} v_{Rj} & \sqrt{2} g_2 v_{Li} \\ \tilde{H}_d^- & -h_{eij} v_{Li} & \mu & \sqrt{2} g_2 v_d \\ -i\tilde{W}^- & 0 & \sqrt{2} g_2 v_u & M_2 \end{array} \tag{2.6}$$

is common to a wide class of $\mathrm{SU}_L(2) \otimes \mathrm{U}_Y(1)$ SUSY models with spontaneous broken of R-parity. In this matrix, M_2 denote the supersymmetry breaking gaugino mass parameter, g_2 is the $\mathrm{SU}_L(2) \otimes \mathrm{U}_Y(1)$ gauge coupling divided by $\sqrt{2}$ and μ is the effective higgsino mixing parameter. The canonical relation $M_1/M_2 = \frac{5}{3}\tan^2\theta_W$ is assumed. To diagonalize the 5×5 non-symmetric chargino mass matrix, two matrix U and V are needed

$$\chi_i^+ = V_{ij}\psi_j^+ \tag{2.7}$$

$$\chi_i^- = U_{ij}\psi_j^- \tag{2.8}$$

where the index i and j run from 1 to 5 and $\psi_j^{\pm} = (e_1^{\pm},\, e_2^{\pm},\, e_3^{\pm},\, \tilde{H}_u^{\pm},\, -i\tilde{W}^{\pm})$. The neutralino mass matrix can be approximated to a 7×7 matrix, shown in Reference [24].

In this model the R-parity breaking was introduced only in the third family, since the largest Yukawa couplings are those of the third generation. In that case the R-parity breaking is effectively parameterized by a bilinear superpotential term given by:

$$\epsilon_i \equiv h_{\nu_{i3}} v_{R3} \ . \tag{2.9}$$

This effective parameter leads to the R-parity violating gauge couplings and contributes to the mixing between the charged (neutral) leptons and the charginos (neutralinos), as can be seen from the fermion mass matrices in Reference [29].

By construction, neutrinos are massless at the Lagrangian level but get mass from the mixing with neutralinos [25, 29]. As a result, all R-parity violating observables are directly correlated to the τ neutrino mass:

$$m_{\nu_\tau} \sim \frac{\xi\epsilon^2}{m_{\tilde{\chi}}} \ , \tag{2.10}$$

where $m_{\tilde{\chi}}$ is the neutralino mass, ϵ is the R-parity violation parameter and ξ is an effective parameter [30] given as a function of M_2, μ and $\tan\beta$.

There are many restrictions on the model parameters, which follow from experiments related to neutrino physics [31]. Taking into account all the constrains, the parameters expectation values lie in the ranges

$$\begin{gathered}10^{-10} \leq h_{\nu 13},\, h_{\nu 23} \leq 10^{-1}\,,\ 10^{-5} \leq h_{\nu 33} \leq 10^{-1} \\ v_{L1} = v_{L2} = 0\,,\ v_L = v_{L3} = 100\,\mathrm{MeV} \\ v_{R1} = v_{R2} = 0\,,\ 50\,\mathrm{GeV} \leq v_R = v_{R3} \leq 1000\,\mathrm{GeV} \\ v_S = v_{S3} = v_R\end{gathered} \tag{2.11}$$

2.3.1 Chargino and Neutralino Decay Modes

In the present model the chargino decays are modified by the existence of new channels. The lightest chargino ($\tilde{\chi}^{\pm}$) exhibits a two-body decay mode with a Majoron (J) in the final state

$$\tilde{\chi}^{\pm} \rightarrow \tau^{\pm} J \tag{2.12}$$

in addition to the three-body decays

$$\tilde{\chi}^{\pm} \rightarrow \nu_\tau \mathrm{W}^{\pm} \rightarrow \nu_\tau \mathrm{q}\bar{\mathrm{q}}',\ \nu_\tau \mathrm{l}_\mathrm{i}^{\pm} \nu_\mathrm{i} \tag{2.13}$$

and

$$\tilde{\chi}^{\pm} \rightarrow \tilde{\chi}^0 \mathrm{W}^{\pm} \rightarrow \tilde{\chi}^0 \mathrm{q}\bar{\mathrm{q}}',\ \tilde{\chi}^0 \mathrm{l}_\mathrm{i}^{\pm} \nu_\mathrm{i} \tag{2.14}$$

assuming that all sfermions are sufficiently heavy ($\mathrm{M}_{\tilde{\nu}} \geq 300\,\mathrm{GeV/c^2}$) not to influence the chargino production or decay. Figure 2.1 illustrates the Feynman diagrams for $\tilde{\chi}^+$ decay. In the framework of MSSM only the last decay channel is present, with the $\tilde{\chi}^0$ being stable. Both the two-body decay (2.12) and the decay with a neutralino in the final state (2.14) are R-parity conserving, while in equation (2.13) the chargino decays through an R-parity violating vertex. The decay branching ratios depend strongly on the effective R-parity violation parameter ($\epsilon \equiv h_{\nu_{i3}} v_{R3}$), as can be observed in Figure 2.2. In a large range of ϵ the new two-body decay mode is the dominant channel and, since it is R-parity conserving, it can be large.

The spontaneous R-parity violation not only opens new decay channels for the chargino but also allows the neutralino to decay, creating new signatures for

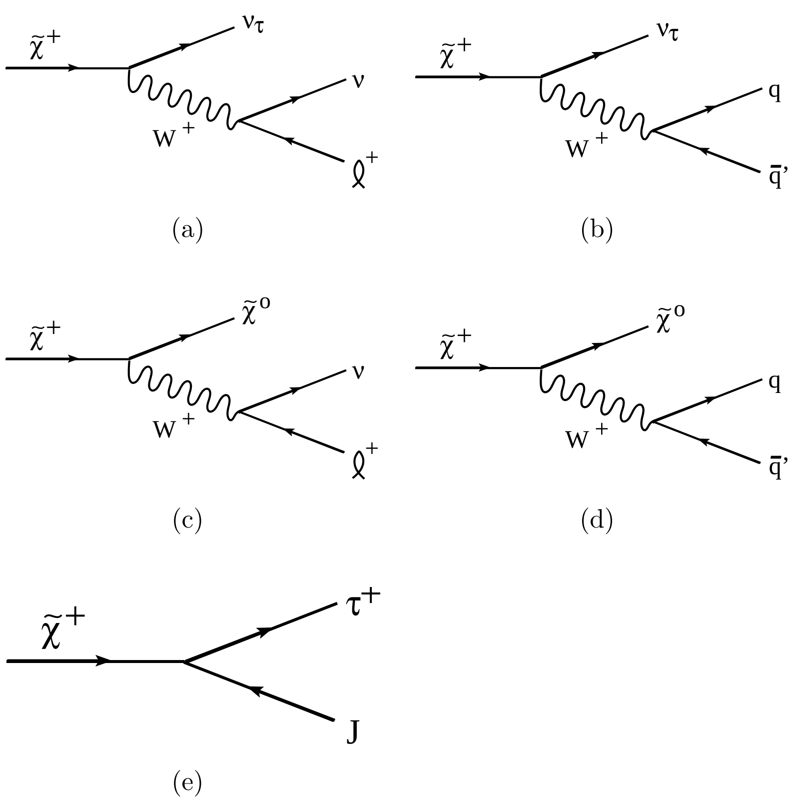


Figure 2.1: Feynman diagrams for $\tilde{\chi}^+$ decay. (a) $\tilde{\chi}^+ \to \nu_\tau l_i^+ \nu_i$, (b) $\tilde{\chi}^+ \to \nu_\tau q \bar{q}'$, (c) $\tilde{\chi}^+ \to \tilde{\chi}^0 \ell_i^+ \nu_i$, (d) $\tilde{\chi}^+ \to \tilde{\chi}^0 q \bar{q}'$ and (e) $\tilde{\chi}^+ \to \tau J$.

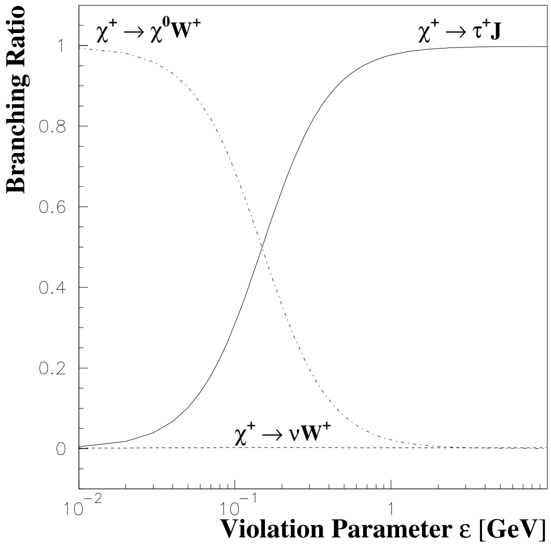


Figure 2.2: Chargino decay branching ratios as a function of the effective R-parity violation parameter ϵ for $\tan\beta = 2$, $\mu = 100\,\mathrm{GeV/c^2}$ and $\mathrm{M_2} = 400\,\mathrm{GeV/c^2}$.

SUSY. In this model the neutralino can decay invisibly into $\tilde{\chi}^0 \to \tau^\pm J$, as well as into

$$\begin{aligned} &\tilde{\chi}^0 \to \nu_\tau \mathrm{Z}^* \to \nu_\tau \nu\nu\,,\ \nu_\tau \ell_i^\pm \nu_i\,,\ \nu_\tau q\bar{q}\ \ ; \\ &\tilde{\chi}^0 \to \tau^\pm W^\pm \to \tau \nu_i \ell_i\,,\ \tau q\bar{q}'\ \ . \end{aligned} \tag{2.15}$$

In this thesis, I perform the search for chargino production at LEP2, considering only the two-body decay mode, as reported in the next chapter.

Chapter 3

R-Parity Violation Search

In this Chapter I present the analysis of the search for spontaneous R-parity violation using the DELPHI detector data. In this search the model described in Section 2.3 is assumed, where the chargino can decay via the two-body decay mode $\tilde{\chi}^{\pm} \to \tau^{\pm} J$.

DELPHI is one of the four experiments of the accelerator LEP (Large Electron Positron Collider), that worked from 1989 to 2000. From the beginning of the data taking up to 1995, LEP delivered events at the Z^0 resonance ($\sqrt{s} \approx 92\,\mathrm{GeV}$) allowing precise measurements of the Standard Model. On its second phase of functionality (LEP2) the machine was upgraded and it started to deliver centre-of-mass energy above $136\,\mathrm{GeV}$, going up to $\sqrt{s} = 208\,\mathrm{GeV}$. This increased the possibility to look for the Higgs and to search for models beyond the Standard Model.

3.1 DELPHI Detector - A Brief Description

The DELPHI detector was previously described in my Master thesis [15]. A brief description can be found in [32]. In this section, I summarize the properties of the DELPHI detector relevant to my analysis. Charged particle tracks were reconstructed in the 1.2 T solenoidal magnetic field by a system of cylindrical tracking detectors. These were the microVertex Detector (VD), the Inner Detector (ID), the Time Projection Chamber (TPC), and the Outer Detector (OD). In addition, two planes of drift chambers aligned perpendicular to the beam axis (Forward Chambers A and B) tracked particles in the forward and backward directions, covering polar angles $11^\circ < \theta < 33^\circ$ and $147^\circ < \theta < 169^\circ$ with respect to the beam (z) direction.

The VD consisted of three cylindrical layers of silicon detectors, at radii 6.3 cm, 9.0 cm and 11.0 cm. All three layers measured coordinates in the plane transverse to the beam. The closest (6.3 cm) and the outer (11.0 cm) layers contained double-sided detectors to measure z coordinates also. The polar angle coverage of the VD was from 25° to 155°. Mini-strips and pixel detectors making up the Very Forward Tracker (VFT) have been added to the end caps of the VD increasing the angular acceptance to include the regions from 10° to 25° and from 155° to 170° [33]. The ID, covering polar angles between 15° and 165°, was composed of a cylindrical drift chamber (inner radius of 12 cm and outer radius of 22 cm) surrounded by 5 layers of straw drift tubes with inner radius of 23 cm and outer radius of 28 cm. The TPC, the main tracking device of DELPHI, was a cylinder of 30 cm inner radius, 122 cm outer radius and length 2.7 m. Each end-plate was divided into 6 sectors, with 192 sense wires and 16 circular pad rows used for 3 dimensional space-point reconstruction. The OD consisted of 5 layers of drift cells at radii between 198 cm and 206 cm, covering polar angles between 43° and 137°.

The average momentum resolution for the charged particles in hadronic final states was in the range of $\Delta p/p^2 \simeq 0.001$ to 0.01 (GeV/c)$^{-1}$, depending on which detectors were used in the track fit [32].

The electromagnetic calorimeters were the High density Projection Chamber (HPC) covering the barrel region of $40^\circ < \theta < 140^\circ$, the Forward ElectroMagnetic Calorimeter (FEMC) covering $11^\circ < \theta < 36^\circ$ and $144^\circ < \theta < 169^\circ$, and the

STIC, a Scintillator TIle Calorimeter which extended coverage down to 1.66° from the beam axis in either direction. The 40° taggers were a series of single layer scintillator-lead counters used to veto electromagnetic particles that would otherwise have been missed in the region between the HPC and FEMC. A similar set of taggers was arranged at 90° to cover the gap between the two halves of the HPC. The efficiency to register a photon with energy above 5 GeV, measured with the LEP1 data, was above 99 %. The hadron calorimeter (HCAL) covered 98 % of the solid angle. Muons with momenta above 2 GeV/c penetrated the HCAL and were recorded in a set of muon drift chambers.

3.2 DELPHI Data Samples

The data collected by the DELPHI detector during 1997 at $\sqrt{s} = 183\,\mathrm{GeV}$ and 1998 at $\sqrt{s} = 189\,\mathrm{GeV}$ corresponds to an integrated luminosity of $211\,\mathrm{pb}^{-1}$. In the year 1999, a total integrated luminosity of $219\,\mathrm{pb}^{-1}$ was collected at the centre-of-mass energies 192 GeV, 196 GeV, 200 GeV and 202 GeV. In 2000, the detector collected a total of $224.6\,\mathrm{pb}^{-1}$ at $\sqrt{s}$ between 202 GeV and 208 GeV. In this last year the largest amount of data was collected at centre-of-mass energy around 206 GeV and the energies were not distinguished in the analysis. The integrated luminosity corresponding to each centre-of-mass energy is showed in Table 3.1.

In order to measure R-parity spontaneous violation signal, it was assumed that the R-parity breaking occurs in the third generation, being parametrized by $\epsilon \equiv h_{\nu_{i3}} v_{R3}$, as discussed in Section 2.3. In that case the lightest chargino ($\tilde{\chi}^{\pm}$) can undergo the two-body decay mode $\tilde{\chi}^{\pm} \rightarrow \tau^{\pm} J$ [10]. The chargino production and decay were simulated by an specific program, described in the next section.

To evaluate background contaminations, different contributions from Standard Model (SM) processes were considered. The background events $Z/\gamma \rightarrow q\bar{q}(\gamma)$ was generated using the PYTHIA [34] generator. The processes $Z/\gamma \rightarrow \tau^+\tau^-(\gamma)$,

Year	$\sqrt{s}$	Luminosity
1997	183 GeV	$53\,\mathrm{pb}^{-1}$
1998	189 GeV	$158\,\mathrm{pb}^{-1}$
1999	192 GeV	$25\,\mathrm{pb}^{-1}$
1999	196 GeV	$76\,\mathrm{pb}^{-1}$
1999	200 GeV	$78\,\mathrm{pb}^{-1}$
1999	202 GeV	$40\,\mathrm{pb}^{-1}$
2000	202 GeV-208 GeV	$224.6\,\mathrm{pb}^{-1}$
1997-2000	183 GeV-208 GeV	$654.6\mathrm{pb}^{-1}$

Table 3.1: Integrated luminosity collected by the DELPHI detector from 1997 to 2000.

$\mu^+\mu^-(\gamma)$ were produced with KORALZ [35] and DYMU3 [37], respectively.

Four-fermion final states were generated with the programs EXCALIBUR [38] and GRC4F [36]. The generator BABAMC [39] was used for the Bhabha scattering. Two-photon interactions leading to leptonic and hadronic final states were produced by the BDK [40] and TWOGAM [41] programs, respectively. Both signal and background events were passed through a detailed detector response simulation and reconstructed as the real data [32].

3.3 Signal Simulation

The program RP-generator II, described in reference [24], was used to calculate charginos masses, production cross-sections and decay branching ratios. It was assumed that all sfermions are sufficiently heavy ($\mathrm{M}_{\tilde{\nu}} \geq 300\,\mathrm{GeV/c^2}$) not to influence the chargino production or decay. Therefore, only the γ and Z s-channels contribute to the chargino cross-section.

Chargino pair production was considered for one value of the R-parity violation parameter, $\epsilon = 3$, for which the decay mode $\tilde{\chi}^{\pm} \rightarrow \tau^{\pm} J$ is dominant. The model parameters were assumed to lie in the ranges described in Equation 2.11. Typical ranges of values for the SUSY parameters $\mu \equiv h_0\langle\Phi\rangle$ and M_2 were assumed for the simulation:

$$\begin{aligned} -200\,\mathrm{GeV/c^2} \leq \mu \leq 200\,\mathrm{GeV/c^2} \\ 40\,\mathrm{GeV/c^2} \leq \mathrm{M}_2 \leq 400\,\mathrm{GeV/c^2} \end{aligned} \tag{3.1}$$

which can be covered by the chargino production at LEP. Also assumed are the GUT relation $\mathrm{M}_1/\mathrm{M}_2 = 5/3\tan^2\theta_W$ and that $\tan\beta$ $(= v_u/v_d)$ lies in the range

$$2 \leq \tan\beta \leq 40\ . \tag{3.2}$$

In order to have a better grid in this parameter space, a faster simulation program *Simulation a Grande Vitesse* [42] (SGV) was used for the signal simulation. The SGV was used to check the points that were not generated by the full DELPHI simulation program (DELSIM). Since this program does not have the same detector description as the DELSIM and do not simulate the DELPHI taggers, a correction has to be done in the simulated data.

3.3.1 DELSIM and SGV Comparison

A comparison between SGV and DELSIM was performed and the selection efficiencies[1] were corrected accordingly. To perform this comparison, up to ten chargino mass points, with 1000 events each, where simulated by DELSIM and SGV at $\sqrt{s} = 183\,\mathrm{GeV}$, $196\,\mathrm{GeV}$, $200\,\mathrm{GeV}$ and $206\,\mathrm{GeV}$. The selection efficiencies of both generators were compared and a correction factor was applied in the selection efficiency. Figure 3.1 shows the comparison between the SGV and DELSIM efficiencies, if the DELPHI taggers are not considered. The correction factor result in about 1.00 at $\sqrt{s} = 183\,\mathrm{GeV}$, 0.92 at $\sqrt{s} = 196\,\mathrm{GeV}$ and $200\,\mathrm{GeV}$. Since

[1]The efficiency of the chargino selection is defined as the number of events satisfying the applied cuts divided by the total number of generated chargino events.

there was no modification from 1999 detector configuration to 2000, a correction factor of 0.92 was also assumed to $\sqrt{s} = 206\,\mathrm{GeV}$.

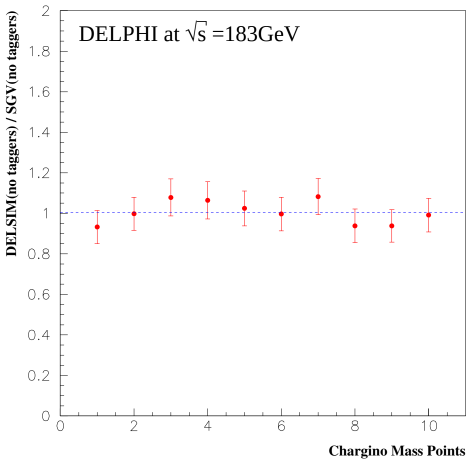
A study performed using DELSIM shows that if the taggers are used in the signal selection, 97% of the events pass this criteria, as can be observed in Figure 3.2. This percentage has to be taken into account for the efficiency correction. As a result, a total correction factor of 0.97 was used in the 1997 and 1998 data selection. The selection efficiency of the data collected in the year 1999 and 2000 was corrected by 0.89.

3.4 Searches for $\tilde{\chi}^{\pm} \to \tau^{\pm} + J$

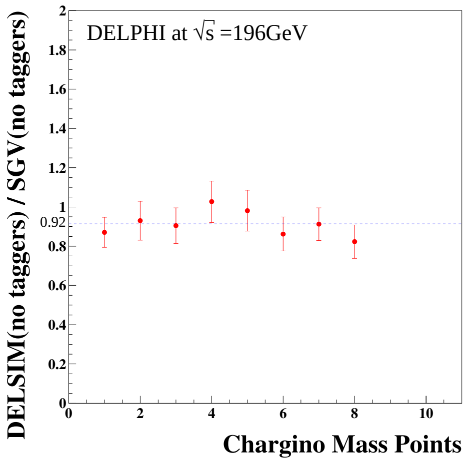
With the R-parity spontaneous breaking, the chargino can decay through an R-parity conserving vertex into $\tau^{\pm} J$ events. Due to the undetectable Majoron, such events have the topology of two taus acoplanar with the beam axis plus missing energy. To select events with this signature it was required that the charged and neutral particles were well reconstructed and that the total momentum transverse to the beam was greater than $4\,\mathrm{GeV/c}$. Charged particles were considered if they had a momentum between $1\,\mathrm{GeV/c}$ and the beam momentum and a polar angle between 30° and 150°. Events passing these cuts were considered as an initial sample events.

The charged particles in the event were then divided in two clusters. The clusters were constructed by considering all combinations of assigning the charged particles in the event into two groups. Neutral particles were then added to the groups such that the mass remains below $5.5\,\mathrm{GeV}$ and those which could not be added to either of the two groups were considered as isolated. Events containing two clusters of charged and neutral particles, each cluster with invariant mass below $5.5\,\mathrm{GeV/c^2}$ and with an acoplanarity[2] above 5° were selected. The events

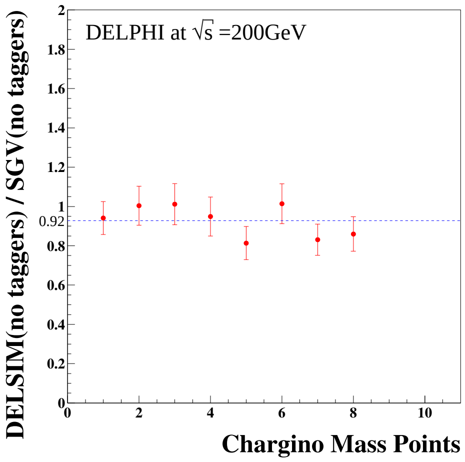
[2]The acoplanarity is defined as the complemental of the angle between the clusters when projected onto the plane perpendicular to the beam.



(a)

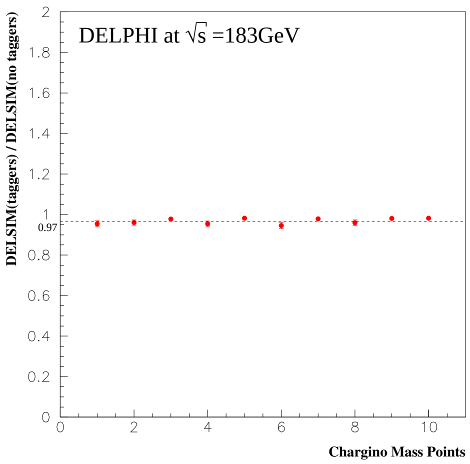


(b)

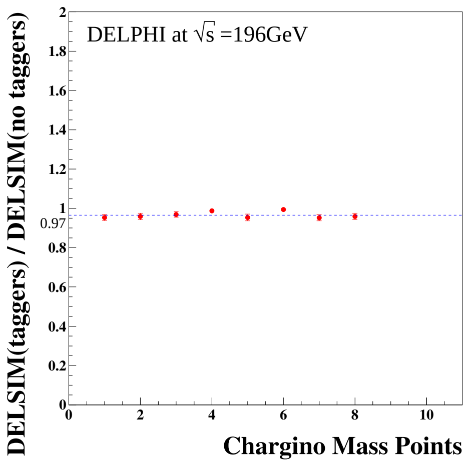


(c)

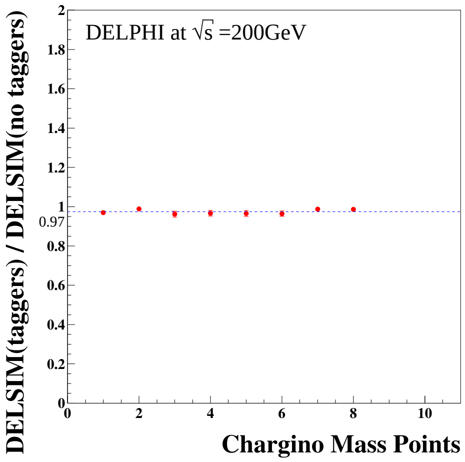
Figure 3.1: Selection efficiency ratio between signal events simulated by DELSIM and SGV, without the cut using the 40° and 90° taggers. The dashed line shows the average value for the efficiency correction factor.



(a)



(b)



(c)

Figure 3.2: Ratio between the selection efficiencies for the DELSIM simulated events before and after require no signal in the 40° and 90° taggers. The average correction factor obtained is 0.97.

were also required to have less than 7 charged particles and not a signal in the 40° or 90° taggers. This preliminary selection was common for all centre-of-mass energies.

3.4.1 Event Selection at 183 GeV

Events passing the preliminary selection were required to have acoplanarity below 176°. Events with forward going secondaries were avoided by rejecting any with energy measured in a 30° cone around the beam axis. Some of the energy in the forward cone resulted from noise and other backgrounds which were not included in the simulation of the signal. It was estimated that $\sim 20\%$ of any signal would be rejected by this selection and the efficiency was appropriately corrected.

To reject the radiative return to the Z background, no events with isolated photons with more than 5 GeV were accepted. The $\gamma\gamma$ and $\mu^+\mu^-(\gamma)$ backgrounds were reduced by requiring that the events had at least one charged particle with momentum between 5 GeV/c and 60 GeV/c. To reduce the $\tau^+\tau^-(\gamma)$ background the square of transverse momentum with respect to the thrust axis divided by the thrust[3] had to be above 0.75 (GeV/c)^2.

To reduce the $\gamma\gamma$ background further, events with momentum of their most energetic charged particle (P_{max}) below 10 GeV/c had to have total momentum

[3] The thrust is defined as

$$thrust \equiv max \frac{\sum \vec{p_i} \cdot \vec{n_i}}{\sum |\vec{p_i}|} \ . \tag{3.3}$$

For two tracks, the thrust is

$$thrust = \left| \frac{p_1 \cos\alpha + p_2 \cos\beta}{p_1 + p_2} \right|_{max} \tag{3.4}$$

where α and β are the angle between the track direction and the thrust axis. In this case, the transverse momentum with respect to the thrust axis divided by the thrust is given by

$$\frac{p_T}{thrust} = \frac{2p_1p_2 \sin(\alpha+\beta)(p_1+p_2)}{|\vec{p_1} - \vec{p_2}|^2} \ . \tag{3.5}$$

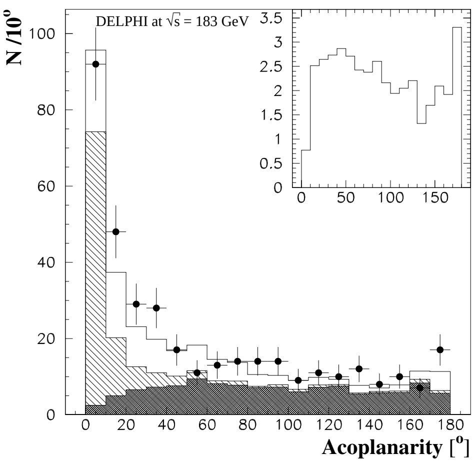
transverse to the beam above 10.5 GeV/c. For events with $P_{max} > 10$ GeV/c, the main remaining contamination comes from $Z/\gamma \to \tau^+\tau^-$ and WW. For those, if the acoplanarity was below 15°, the angle between the missing momentum and the beam had to be greater than 30°. On the other hand, if the acoplanarity was above 15°, it was required that the momentum of the most energetic particle was below 23.5 GeV/c and the angle between the missing momentum and the beam was greater than 34.5°.

The agreement between data and simulated background events are shown in Figure 3.3. The inserts for each plot shows an example of the two body decay mode behavior for $\tan\beta = 2$, $\mu = 100\,\mathrm{GeV/c^2}$ and $M_2 = 400\,\mathrm{GeV/c^2}$. In this Figure the events were selected by requiring two clusters of well reconstructed neutral and charged particles, less than 7 charged particles and a total transverse momentum above 4 GeV/c. For the acoplanarity distribution, it was also required that the square of the transverse momentum with respect to the thrust axis divided by the thrust was above 0.75 (GeV/c)^2. A detailed agreement between data and background after each selection criteria is reported in References [43–45].

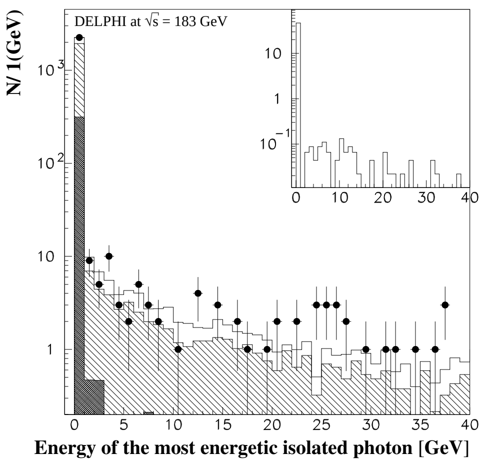
This selection resulted in 6 candidates of $\tilde{\chi}^\pm \to \tau^\pm + J$ with a background estimation of 6.3 ± 0.4 and a signal detection efficiency of about 18 %. Figure 3.4 shows the dependence of the signal detection efficiency on the chargino mass. Table 3.2 summarizes the number of accepted events in the data, together with the predicted number of events from background sources.

3.4.2 Event Selection at 189 GeV

Since LEP delivered a higher luminosity for this energy and the WW background increased, tighter cuts were applied. The required acoplanarity had to be between 10° and 176° and no events with an isolated photon were accepted. The momentum of each of the two particle clusters had to be above 5 GeV/c and below 55 GeV/c and the square of transverse momentum with respect to the thrust



(a)



(b)

Figure 3.3: Distribution of (a) acoplanarity and (b) energy of the most energetic isolated photon. The points with error bars show the real data, while the white histograms show the total simulated background. The distributions corresponding to the $\gamma\gamma$ background and the Bhabha scattering are shown as dark and hatched histograms, respectively. An example of the two body decay mode $\tilde{\chi}^{\pm} \to \tau^{\pm} + J$ behavior is shown in the inserts for each plot.

Observed events	**6**
Total background	**6.3 ± 0.4**
Bhabha scattering and Z/$\gamma \to ee, \mu\mu, \tau\tau, q\bar{q}$	1.0 ± 0.3
4-fermion events except WW	0.6 ± 0.1
$\gamma\gamma \to ee, \mu\mu, \tau\tau$	0.3 ± 0.1
W^+W^-	4.4 ± 0.3

Table 3.2: Summary of the observed events and expected backgrounds for the data collected by DELPHI at $\sqrt{s} = 183\,\mathrm{GeV}$.

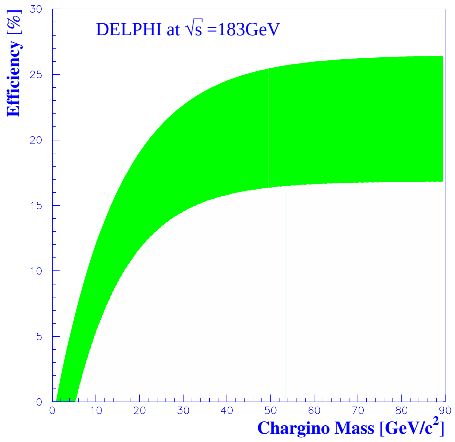


Figure 3.4: Chargino detection efficiency as a function of the chargino mass for $\sqrt{s} = 183\,\mathrm{GeV}$, considering only the two body decay mode $\tilde{\chi}^{\pm} \rightarrow \tau^{\pm} + J$. The bands correspond to the statistical uncertainties combined with the effect of generating events with different MSSM parameters M_2 and μ, which have been varied in the ranges $40\,\mathrm{GeV/c^2} \leq \mathrm{M}_2 \leq 400\,\mathrm{GeV/c^2}$ and $-200\,\mathrm{GeV/c^2} \leq \mu \leq 200\,\mathrm{GeV/c^2}$, for $\tan\beta = 2$.

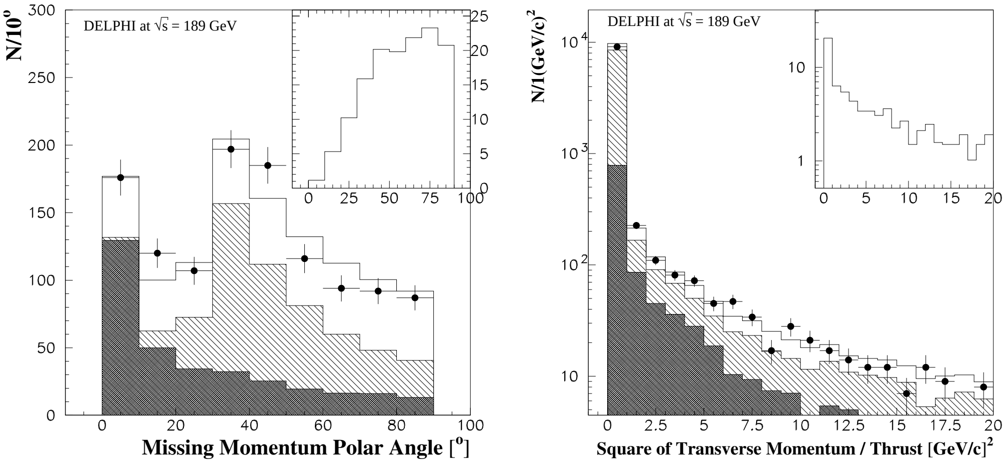
axis divided by the thrust had to be above 1.0 (GeV/c)^2. All the events had to have the angle between the missing momentum and the beam greater than 35°.

The $\gamma\gamma$ background was mainly reduced by requiring a total momentum transverse to the beam greater than 9 GeV/c. Events from WW processes were reduced by requiring that the momentum of the most energetic particle was below 23 GeV/c.

If one cluster had a momentum above 10 GeV/c and the acoplanarity was less than 15° it was also required that the value of the effective centre-of-mass energy after any initial state radiation ($\sqrt{s'}$) [46] did not fall in the region between 90 GeV and 94 GeV. For an acoplanarity above 15°, the angle between the missing momentum and the beam was required to be greater than 40° and the visible mass lower than 70 GeV/c^2.

Figure 3.5 shows the agreement between data and simulated background events, together with an example of the two body decay mode for $\tan\beta = 2$, $\mu = 100\,\mathrm{GeV/c^2}$ and $\mathrm{M}_2 = 400\,\mathrm{GeV/c^2}$. The events shown in this Figure were selected by requiring two clusters of well reconstructed neutral and charged particles, less than 7 charged particles and a total transverse momentum above 4 GeV/c. For the missing momentum polar angle distribution, it was also required that the square of the transverse momentum with respect to the thrust axis divided by the thrust was above 1. (GeV/c)^2. References [45, 47, 48] gives a detailed agreement between data and background after each selection criteria.

As a result, 9 candidates of $\tilde{\chi}^{\pm} \to \tau^{\pm} + J$ were selected, with a background estimation of 9.6±0.4 and a signal detection efficiency of about 14 %. The number of accepted events in the data, together with the predicted number of events from background sources are summarized in Table 3.3. The signal detection efficiency dependence on the chargino mass is shown in Figure 3.6. The bands correspond to the statistical uncertainties combined with the effect of generating events with different MSSM parameters M_2 and μ, which have been varied in the ranges described in Equation 3.1, for $\tan\beta = 2$.



(a) (b)

Figure 3.5: Distribution of (a) angle between the missing momentum and the beam-axis and (b) square of transverse momentum with respect to the thrust axis divided by the thrust. The points with error bars show the real data, while the white histograms show the total simulated background. The distributions corresponding to the $\gamma\gamma$ background and the Bhabha scattering are shown as dark and hatched histograms, respectively. An example of the decay mode $\tilde{\chi}^{\pm} \rightarrow \tau^{\pm} + J$ is shown in the inserts for each plot.

Observed events	**9**
Total background	**9.6 ± 0.4**
Bhabha scattering and $Z/\gamma \rightarrow ee, \mu\mu, \tau\tau, q\bar{q}$	0.6 ± 0.1
4-fermion events except WW	1.2 ± 0.2
$\gamma\gamma \rightarrow ee, \mu\mu, \tau\tau$	0.2 ± 0.2
W^+W^-	7.6 ± 0.3

Table 3.3: Summary of the observed events and expected backgrounds for the data collected by DELPHI at $\sqrt{s} = 189\,\text{GeV}$.

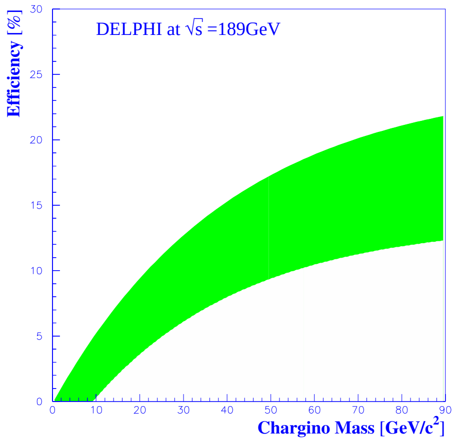


Figure 3.6: Chargino detection efficiency as a function of the chargino mass for $\sqrt{s} = 189\,\mathrm{GeV}$, considering only the two body decay mode $\tilde{\chi}^{\pm} \rightarrow \tau^{\pm} + J$.

3.4.3 Event Selection from 192 GeV to 208 GeV

For this selection the accumulated luminosity was much higher than the previous years and the background increased, due to the higher centre-of-mass energy. Because of that the requirements on the measured energy in a 30° cone around the beam axis and the square of transverse momentum with respect to the thrust axis divided by the thrust were not used. Events with forward going secondaries and $\tau^+\tau^-(\gamma)$ background were reduced by a cut on the event missing energy.

The events passing the preliminary selection were required to have missing energy greater than 50 % of the centre-of-mass energy. The radiative return to the Z background was reduced by demanding no isolated photons in the event. To reduce the $\gamma\gamma$ background the momentum of each of the two particle clusters had to be above 5 GeV/c and the total momentum transverse to the beam axis had to be greater than 11 GeV/c. The $\mu^+\mu^-(\gamma)$ background was reduced by requiring a cluster momentum below 55 GeV/c. Events from WW processes were avoided by requiring that the momentum of the most energetic particle was below 23 GeV/c. It was further required that all events had an acoplanarity between 10° and 176°, the angle between the missing momentum and the beam axis greater than 35° and no signal in the 40° or 90° taggers.

If one cluster had a momentum above 10 GeV/c and the acoplanarity was less than 15° it was also required that the value of the effective centre-of-mass energy after an initial state radiation ($\sqrt{s'}$) [46] did not fall in the region between 90 GeV and 94 GeV. For an acoplanarity above 15°, the angle between the missing momentum and the beam axis was required to be greater than 40°. These cuts reject mainly WW and $\tau^+\tau^-(\gamma)$ events.

An example of the agreement between data and simulated background events is shown on Figures 3.7 and 3.8. An example of the decay mode $\tilde{\chi}^\pm \to \tau^\pm + J$ for $\tan\beta = 2$, $\mu = 100\,\mathrm{GeV/c^2}$ and $\mathrm{M_2} = 400\,\mathrm{GeV/c^2}$ is shown in the inserts of each plot. These events were selected by requiring at least two clusters of well reconstructed charged and neutral particles and an acoplanarity above 5°.

A total of 57 candidates of $\tilde{\chi}^\pm \to \tau^\pm + J$ were selected at $\sqrt{s}$ between 192 GeV and 208 GeV, with a total background estimation of 56.4 ± 2.4 and a selection efficiency of about 20 %. Table 3.4 shows the number of accepted events in the data, together with the predicted number of events from background sources. The systematic and statistical errors on the simulated background calculation are negligible compared to the experimental statistical accuracy. The number of candidates, expected backgrounds and the signal detection efficiency after each selection criteria are reported elsewhere [49, 50].

The corrected selection efficiencies are shown in Figure 3.9 as a function of the chargino mass. The bands correspond to the effect of generating points with different MSSM parameters $\mathrm{M_2}$ and μ, which have been varied in the ranges $40\,\mathrm{GeV/c^2} \leq \mathrm{M_2} \leq 400\,\mathrm{GeV/c^2}$ and $-200\,\mathrm{GeV/c^2} \leq \mu \leq 200\,\mathrm{GeV/c^2}$, for $\tan\beta = 2$. Figure 3.10 shows event displays of two selected candidates at centre-of-mass energies of 196 GeV and 200 GeV.

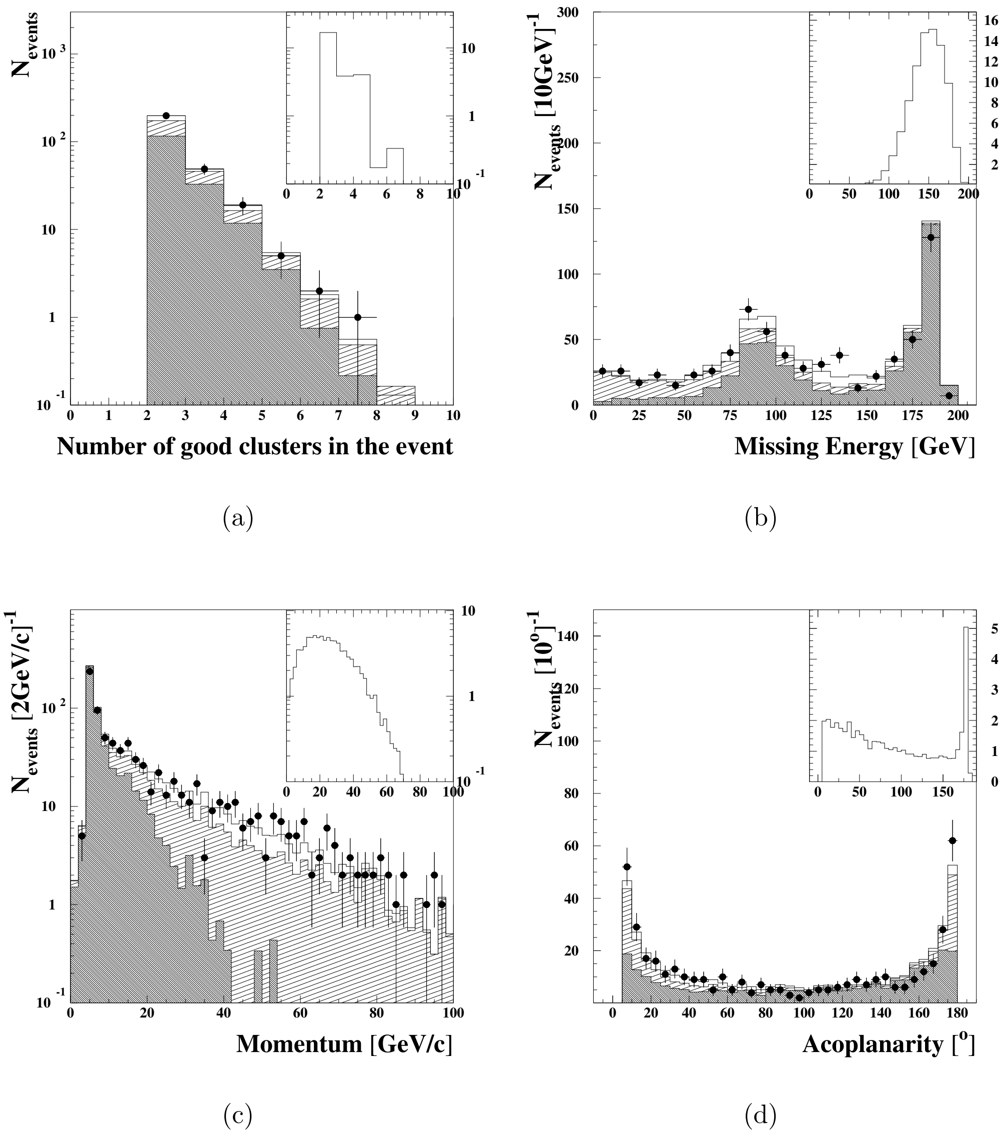
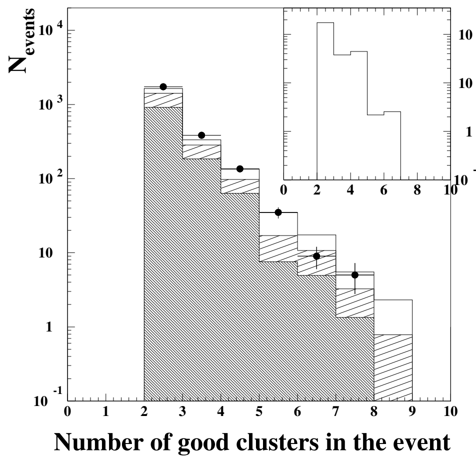
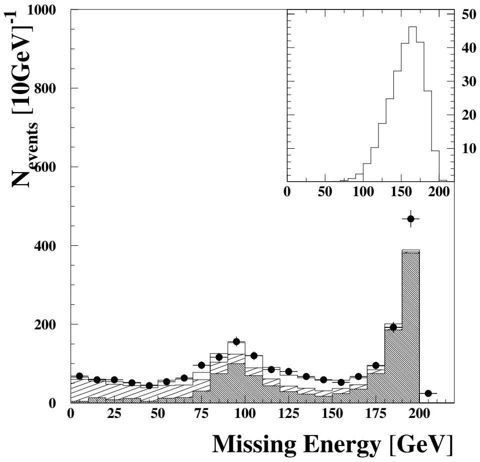


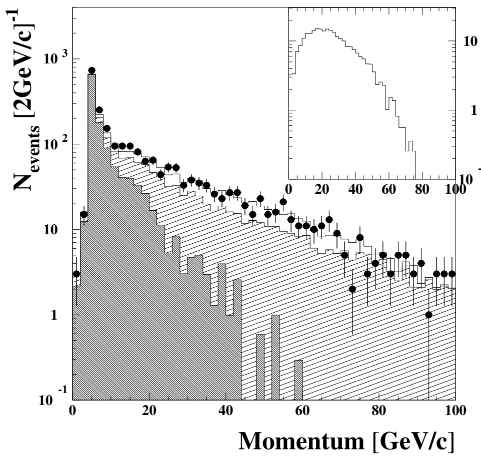
Figure 3.7: Distribution of (a) number of clusters in the event for $\sqrt{s} = 192\,\mathrm{GeV}$, (b) missing energy for $\sqrt{s} = 196\,\mathrm{GeV}$, (c) cluster momentum for $\sqrt{s} = 200\,\mathrm{GeV}$ and (d) acoplanarity for $\sqrt{s} = 202\,\mathrm{GeV}$. The points with error bars show the real data, while the white histograms show the total simulated background. The distributions corresponding to the $\gamma\gamma$ background are shown as dark histograms, while the Bhabha and Z/γ simulated events are shown as hatched histograms. The inserts for each plot show an example of the two body decay mode.



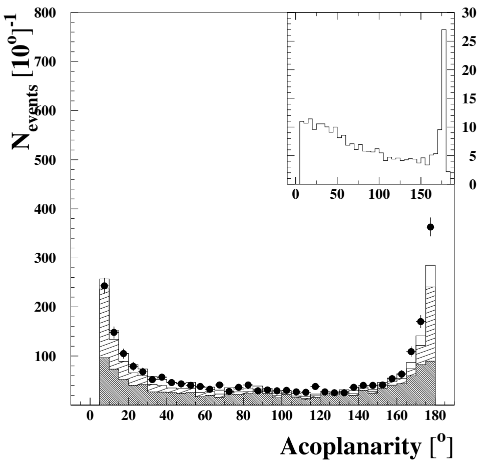
(a)



(b)

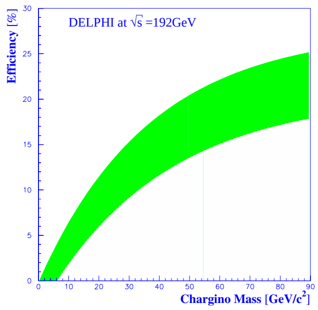


(c)

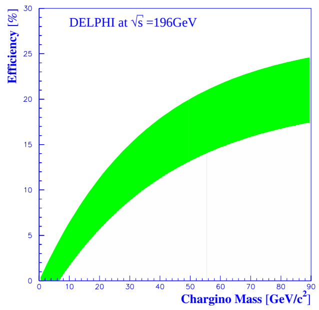


(d)

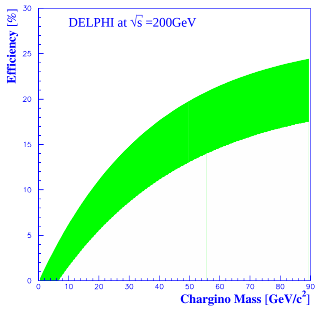
Figure 3.8: Distribution of (a) number of clusters in the event, (b) missing energy, (c) cluster momentum and (d) acoplanarity for $\sqrt{s} \sim 206\,\mathrm{GeV}$. The points with error bars show the real data, while the white histograms show the total simulated background. The distributions corresponding to the $\gamma\gamma$ background are shown as dark histograms, while the Bhabha and Z/γ simulated events are shown as hatched histograms. The inserts for each plot show an example of the two body decay mode.



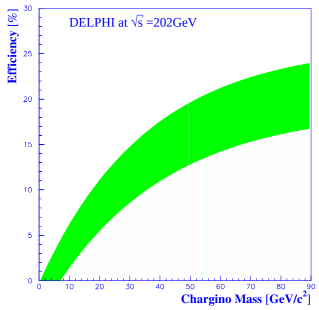
(a)



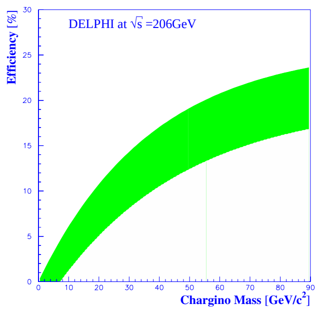
(b)



(c)

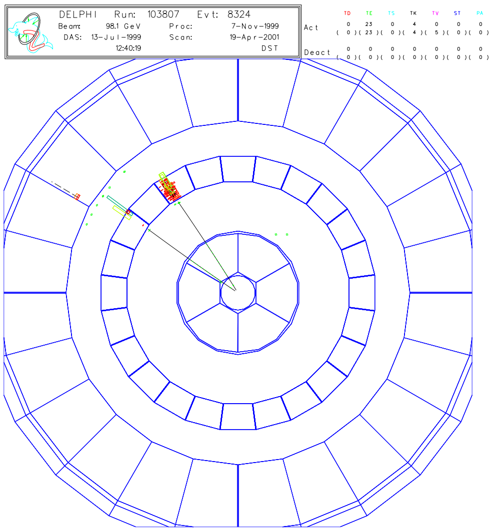


(d)

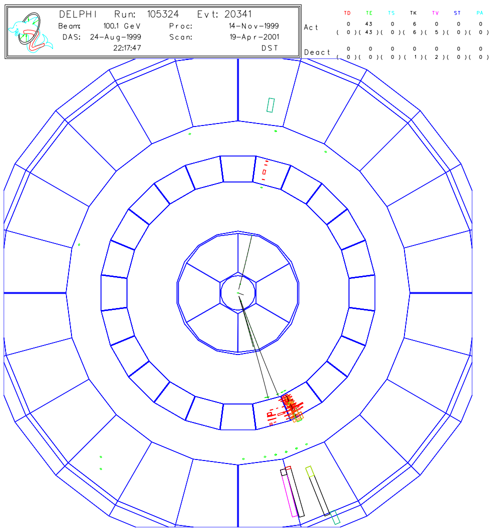


(e)

Figure 3.9: Chargino detection efficiency as a function of the chargino mass for centre-of-mass energies (a)192 GeV, (b) 196 GeV, (c) 200 GeV, (d) 202 GeV and (e) 206 GeV, considering only the two body decay mode $\tilde{\chi}^{\pm} \rightarrow \tau^{\pm} + J$.



(a)



(b)

Figure 3.10: Example of event displays of two selected candidates at $\sqrt{s} = 196\,\mathrm{GeV}$ (top) and $\sqrt{s} = 200\,\mathrm{GeV}$ (bottom).

Year	1999	2000
Centre-of-mass energy	192 GeV to 202 GeV	202 GeV to 208 GeV
Observed events	**25**	**32**
Total background	**28.8 ± 1.2**	**27.6 ± 1.8**
$\gamma\gamma$	6.4 ± 1.1	6.0 ± 1.7
WW	15.6 ± 0.4	15.3 ± 0.3
Zγ	6.0 ± 0.4	5.1 ± 0.2
ZZ	0.7 ± 0.1	1.1 ± 0.2
Bhabha	0.1 ± 0.1	0.1 ± 0.1

Table 3.4: Observed events and expected backgrounds for centre-of-mass energies from 200 GeV to 208 GeV.

3.5 Combined Results

The DELPHI detector collected a total integrated luminosity of 654.6 pb^{-1} during the years 1997, 1998, 1999 and 2000. Combining all the results obtained in the search for $\tilde{\chi}^{\pm} \to \tau^{\pm} + J$ at centre-of-mass energies between 183 GeV and 208 GeV, 72 candidates with 72.3 ± 2.5 expected from the SM processes are obtained. The number of candidates together with the expected background are summarized in Table 3.5.

3.6 Summary

In the present analysis it was assumed that the R-parity breaking occurs in the third generation and, as a consequence, the lightest chargino decays mainly through the two-body decay mode $\tilde{\chi}^{\pm} \to \tau^{\pm} + J$, assuming a sneutrino mass above 300 GeV/c^2. No evidence for spontaneous R-parity breaking has been observed and a limit on the chargino production cross-section and mass was calculated.

Year	Luminosity	Observed events	Total background
1997	$53\,\mathrm{pb}^{-1}$	6	6.3 ± 0.4
1998	$158\,\mathrm{pb}^{-1}$	9	9.6 ± 0.4
1999	$219\,\mathrm{pb}^{-1}$	25	28.8 ± 1.2
2000	$224.6\,\mathrm{pb}^{-1}$	32	27.6 ± 1.8
Total	$654.6\,\mathrm{pb}^{-1}$	72	72.3 ± 2.5

Table 3.5: Summary of the observed events and expected backgrounds found in the search for $\tilde{\chi}^{\pm} \rightarrow \tau^{\pm} + J$.

The maximum allowed production cross-section can be calculated according to the formula

$$\sigma(e^+e^- \rightarrow \tilde{\chi}^+\tilde{\chi}^-) = \frac{N_{sig}}{\mathcal{L}\ \varepsilon} \tag{3.6}$$

where N_{sig} is the number of expected signals, $\mathcal{L}$ the luminosity and ε the selection efficiency. Considering the background is perfectly known, the number of expected signals can be determined by using the Bayesian statistics [51] with a confidence level ($C.L.$) as

$$1 - C.L. = \frac{e^{-(N_{Bck}+N_{sig})} \sum_{n=0}^{N_{obs}} \frac{(N_{Bck}+N_{sig})^n}{n!}}{e^{-N_{Bck}} \sum_{n=0}^{N_{obs}} \frac{N_{Bck}^n}{n!}} \tag{3.7}$$

where N_{Bck} is the number of background events and N_{obs} number of observed events in the data.

Considering 72 candidates with 72.3 ± 2.5 expected background events at an integrated luminosity of $654.6\,\mathrm{pb}^{-1}$, 18.23 signal events are expected at 95% confidence level. This gives a maximum allowed cross-section of 0.14 pb, as shown in Figure 3.11.

At this cross-section, a chargino can be produced if its mass is greater or equal to $103.8\,\mathrm{GeV/c}^2$. With this limit it is possible to construct the excluded domains of the (μ, M_2) parameter space. Figure 3.12 shows these excluded domains for $\tan\beta = 2$ and $\tan\beta = 40$ at centre-of-mass energies up to 208 GeV. The two body decay mode $\tilde{\chi}^{\pm} \rightarrow \tau^{\pm} J$ has a low branching ratio in the region for $\tan\beta = 2$, $50 \leq \mathrm{M}_2 \leq 75$ and $-150 \leq \mu \leq -100$. Therefore no limit can be set in this region and the μ, M_2 excluded domain plot has a hole in this region.

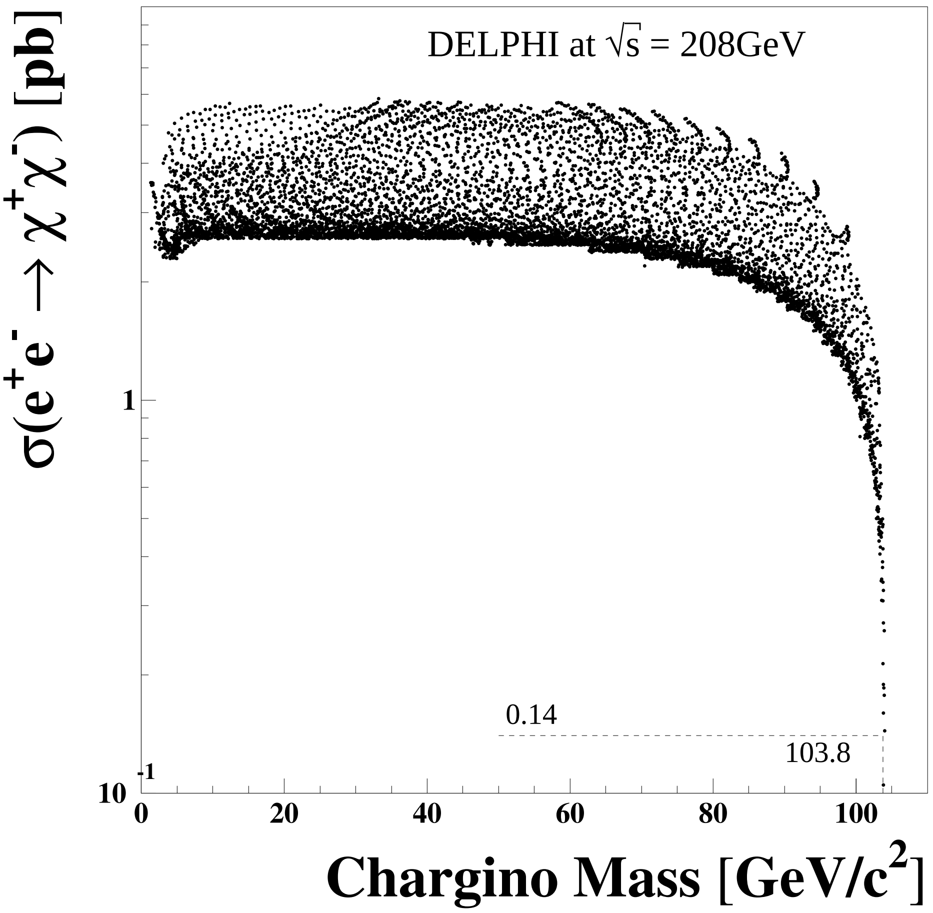
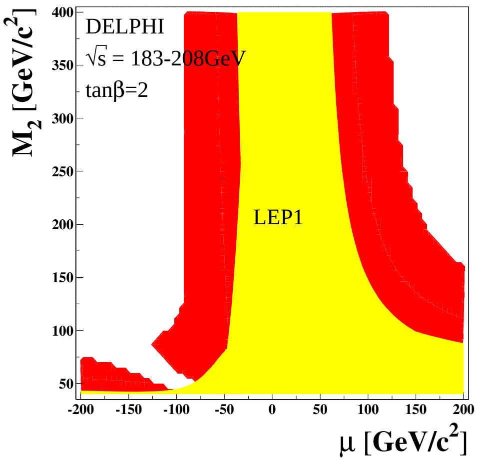
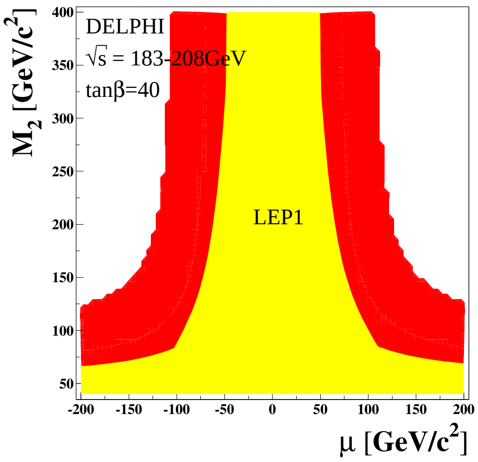


Figure 3.11: Expected $e^+e- \to \tilde{\chi}^+\tilde{\chi}^-$ cross-section at 208 GeV (dots) as a function of chargino mass, assuming a heavy sneutrino ($M_{\tilde{\nu}} \geq 300\,\mathrm{GeV/c^2}$). The dots correspond to the generating points at different chargino masses for the parameters ranges: $40\,\mathrm{GeV/c^2} \leq \mathrm{M_2} \leq 400\,\mathrm{GeV/c^2}$, $-200\,\mathrm{GeV/c^2} \leq \mu \leq 200\,\mathrm{GeV/c^2}$ and $2 \leq \tan\beta \leq 40$. The dotted line shows the maximum allowed chargino production cross-section at 95% confidence level and the corresponding mass limit.



(a)



(b)

Figure 3.12: Excluded regions in μ, M_2 parameter space at 95% confidence level for (a) $\tan\beta = 2$ and (b) $\tan\beta = 40$, assuming $M_{\tilde{\nu}} \geq 300\,\mathrm{GeV/c^2}$. The exclusion area obtained with the $\tilde{\chi}^{\pm} \rightarrow \tau^{\pm} J$ search is shown in dark grey and the corresponding area excluded by the LEP1 data [52] is shown in light grey.

Parte III

CARIOCA - Uma Nova Eletrônica de *Front-end* para o Detetor de Múons do LHCb

Chapter 4

A New Generation of Research Facilities

4.1 Introduction

Future progress concerning the physics beyond the Standard Model depends on experimental tests of the electroweak symmetry breaking mechanism. The future Large Hadron Collider (LHC) will provide the opportunity to test the validity of the one-doublet Higgs sector of the Standard Model, as well as its possible extensions, to measure the CP violation in the B meson system and to study heavy ions interactions. In this chapter I give an overview of the LHC and its high energy physics experiments that are foreseen to start operating around 2006 at CERN, Geneva.

4.2 The Large Hadron Collider

Large Hadron Collider (LHC) is a circular accelerator that is currently under construction at CERN. It consists of two adjacent 27 Km rings in which two proton beams run in opposite direction. Each ring will be filled with 2835 bunches of 10^{11} particles, resulting in a beam current of 0.53 A. The beams will be stored at high energy for about 10 to 20 hours and during this time the particles will make four hundred million revolutions around the machine. These beams will collide in four points along the circumference at a centre-of-mass energy of 14 TeV. A maximum luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and a good mean life time of about 10 hours will permit to get sensitivity to small cross-section processes. Four experiments are under construction to investigate proton-proton and heavy ions interactions: ATLAS (A Toroidal LHC ApparatuS) [53], CMS (Compact Muon Solenoid) [54], ALICE (A Large Ion Collider Experiment) [55] and LHCb (Large Hadron Collider beauty experiment) [56].

Compared to previous machines, the LHC is a challenge in terms of data acquisition and triggering. The bunch crossing period will be of 25 ns, compared to HERA with 96 ns, Fermilab $\overline{p}p$ collider with 3.5 μs and LEP with 11 μs. In addition to that, in the ATLAS and CMS colliding points, each bunch crossing will contain several proton-proton interactions with an average of 20 inelastic collisions per crossing at the nominal luminosity. Consequently, events corresponding to rare physics process will be superimposed on a huge background of particles from other interactions. At the LHCb interaction point, the beam is defocused, allowing in average one pp interaction for reduced luminosity.

To minimize the problem of pileup, in which particles form an event overlap with particles from other interactions in the same bunch crossing, high granularity detectors are proposed. This leads to a very large number of detector channels. To avoid dead time all detector data from all bunch crossings should be recorded in pipeline memories until the first trigger decision is taken. The overall trigger architectures currently under consideration for LHC contain several trigger levels. After the last trigger level a full event reconstruction can be performed, reducing the amount of data to be recorded for the physics analysis purposes.

At high luminosity the proton-proton collision will produce an extremely hostile radiation environment. The doses[1] and fluences[2] for many particles have been calculated for each LHC experiment. The total dose contribution is mainly due to the primary flux (protons, pions, kaons) coming from the interaction region.

4.3 Physics Motivations

The non conservation of Charge and Parity symmetry (CP) is one of the remaining open questions in particle physics. It was first observed in K^0 meson decays in 1964 [57] and after in B decays. CP violation can occur in any theory in which there are complex coefficients in the Lagrangian. In the SM, the origin of CP violation is the complex coupling of quarks to the Higgs field. After the electroweak symmetry breaking and after removing unphysical phases, one complex phase remains in the three-generation quark mixing matrix, the Cabibbo-Kobayashi-Maskawa (CKM) quark matrix [7]. Although a phase can be introduced in the unitary CKM matrix, the theory does not predict the magnitude of the effect.

There is already an extensive experimental program to look for CP violation in the neutral B-meson systems: Babar [58], Belle [59], CDF [60], CLEO [61], D0 [62] and HERA-B [63]. Both Babar and Belle have established a method to measure the CP violation parameters in B meson decays. The most recent results for $\sin 2\beta$ are $0.075 \pm 0.09 \pm 0.07$ [64] and $0.082 \pm 0.012 \pm 0.05$ [65]. However, the precision test of the SM will remain by far incomplete due to the limited statistics and detector capabilities in those experiments, and the LHC will still play a crucial role to reveal physics beyond the standard model [66].

Recent measurements of a non-zero CP asymmetry [64, 65, 67–70] have shown that future hadron collider experiments will play an important role in understanding of how much the CKM matrix of the Standard Model can accommodate

[1] Dose is the energy deposited for ionization in the material. The SI unit is the Gray (Gy) and it corresponds to 1 Gy=1 J/Kg=100 Rad.

[2] Fluence is the number of incident particles per area.

the observed CP violation. One of the most promising way is the study of B meson decays where the Standard Model predicts large CP violating effects and new physics could be detected from precise measurements of CP violations. Detailed description can be found elsewhere [71].

At LHC, B mesons can be produced with large cross section ($\sigma = 500\,\mathrm{pb}$) in collider mode ($\sqrt{s} = 14\,\mathrm{TeV}$). Compared to other machines that are in operation or under construction, the LHC will be the largest source of B mesons, due to the high $b\bar{b}$ cross-section and high luminosity. Both ATLAS and CMS experiments have included the measurement of CP violation in their physics program, based essentially on the study of the "golden" channel $B \rightarrow J/\psi + K_s$, but they are not optimized for b physics. The LHCb detector is designed to exploit the large number of b hadrons produced in order to make precise studies of CP asymmetries and of rare B mesons decays. The high centre-of-mass energy and luminosity combined with the efficient trigger, including on-line detection of secondary vertices, will give unprecedent statistics for many physics channels.

4.4 The LHCb Experiment

The LHCb Technical Proposal [56] was approved in the year 1998 and since that time the subdetectors are under development. Some of the detector characteristics described in the technical proposal have changed and they are being updated in the subsystems technical design report. The total amount of material in the detector is still under investigation and a reduction should be done. In this section I describe the detectors as they are reported in their technical design report.

LHCb will be ready to take data from the start of the LHC operation at its full physics potential, since it is designed to run at an average luminosity of $2 \times 10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The luminosity will be kept constant (even when ATLAS and CMS will run at high luminosity) by an appropriate defocusing of the beams at the LHCb interaction point. At this luminosity the detector occupancy remains low and the radiation damage is reduced. This will allow the experiment to collect data for many years under constant conditions.

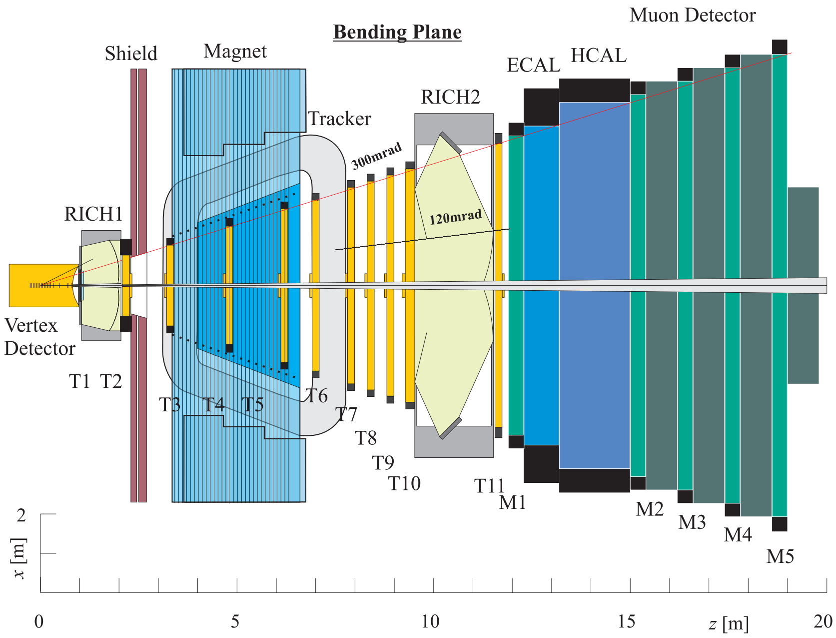
In one year of data taking[3] about 10^{12} $b\bar{b}$ pairs are expected. With the capabilities described in [56], the LHCb can determine all the angles of the two unitary triangles of the Wolfenstein's parameterisation [72] using high statistics data.

4.4.1 Detector Overview

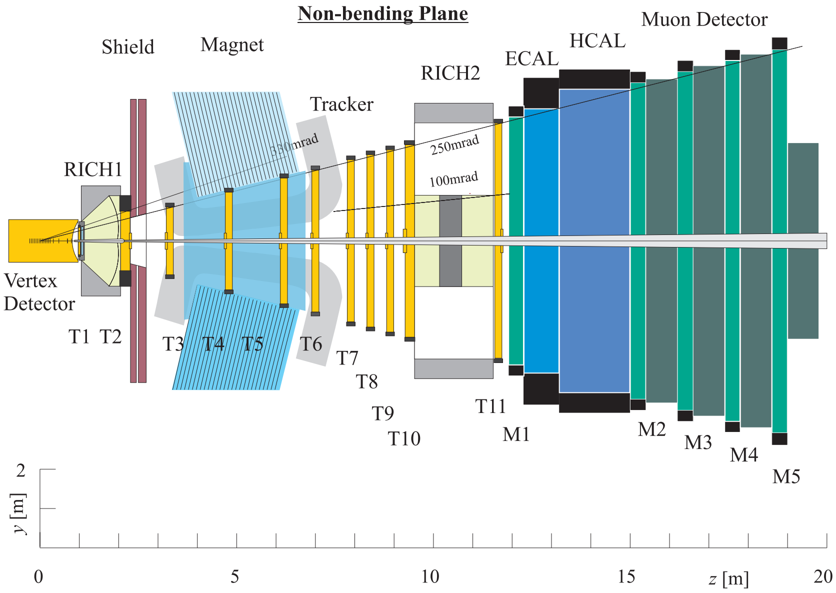
LHCb is a single-arm spectrometer with a forward coverage from about 10 mrad to 300 mrad (250 mrad) in the bending (non-bending plane). Figure 4.1 shows the detector layout as from the technical proposal. The choice of the detector geometry is motivated by the fact that at high energies both b and $\bar{b}$ hadrons are mainly produced in the same forward cone. The detector comprises a vertex detector system, a tracking system, RICH counters, an electromagnetic and hadronic calorimeter and a muon detector. All detectors subsystems, except the vertex detector, can be assembled in two halves, which can be separated horizontally for maintenance and to provide access to the beam pipe. A right-handed coordinate system is defined centered on the interaction point, with z along the beam axis and y pointing upward.

The magnets with a free aperture of ±300 mrad horizontally and ±250 mrad vertically [73] is placed close to the interaction region, covering part of the tracking system. Tracking detectors in and near the magnetic field have to provide momentum measurement for charge particles with a precision of 0.4 % for momenta up to 200 GeV/c. This demands an integrated field of 4 Tm for tracks originating near the primary interaction point. An iron shield upstreams of the magnet reduces the stray field close to the vertex and the RICH 1 detector. For the technical proposal a superconducting magnet has been assumed, but contacts

[3] One year of data taking is defined as 10^7s.



(a)



(b)

Figure 4.1: LHCb detector seen from (a) bending plane and (b) non-bending plane.

with industry and detailed study the design was moved to a warm magnet. A warm dipole permits rapid ramping-up of the field, synchronous to the ramping-up of LHC magnets, as well as regular field inversions. The polarity inversion is important to reduce systematic errors in the CP violation measurements that could result from a left-right asymmetry of the detector.

The basic tasks of the vertex detector [74] are the primary vertex position reconstruction, detection of tracks which do not originate from the primary vertex and reconstruction of b hadron decay vertices. The vertex detector comprises a total of 25 stations, using $0.32\,\mathrm{m}^2$ of silicon area, with a total of 204,800 readout channels. the stations are divided in left and right detector modules and each module has one R-measuring and one ϕ-measuring sensor. The silicon sensors have a circular shape, patterned with azimutal (R measuring) or quasi-radial (ϕ measuring) strips. Each sensor has an azimutal coverage of about 182°, giving a small overlap between right and left halves. Simulations show that for an average event, the resolution in z direction is $42\,\mu$m and $10\,\mu$m perpendicular to the beam. The error on the primary vertex is dominated by the number of tracks produced in the pp collision. A pile-up veto counter is under study, for use in the Level-0 trigger to suppress events containing multiple pp interactions in a single bunch crossing, by counting the number of primary vertices.

Charge particle tracking behind the vertex region will be performed with a system of tracking stations. The stations are located between the vertex detector and the calorimeters. Each station consist of several planes, and each plane is assembled from discrete detector modules. By the time of the LHCb technical proposal approval, the number of tracking station were eleven. This is still under study and the total number of stations is not completely defined. The inner most region of each station, where the particle flux is high, will be covered with a fine grained detector know as Inner Tracker. The Outer Tracker [75] will cover the remaining area, which corresponds to 98 % of the stations surface. The smallest station, T1, will be built with Inner Tracker technology only. The main task of the tracking system is to provide efficient reconstruction and precise momentum measurement of charged tracks, track directions for ring reconstructions in RICH and information for Level-1 and higher-level triggers. The choice of technology for the Inner and Outer Tracker is determined by the requirement of low occupancy.

The RICH system [76] has the task of identifying charged particles over the momentum range 1 to 150 GeV/c, covering the full angular acceptance of the LHCb. To cover the full range, three radiators are required, with different refractive index. The system consists of an upstream detector (RICH 1) with both silica aerogel and a C_4F_{10} gas radiator, and a downstream detector (RICH 2) with CF_4 gas radiator. RICH 1 has 25-330 mrad acceptance and is used to detect low momentum tracks. RICH 2 has a small acceptance, 120 mrad (horizontal) and 100 mrad (vertically), and it catches a large fraction of the high momentum tracks. The Cherenkov photons are focused by mirrors to detector planes positioned outside the spectrometer acceptance. A total image surface of about $2.9\,\mathrm{m}^2$ and a detector granularity of $2.5 \times 2.5\,\mathrm{mm}^2$ is required.

The calorimeter system [77] is divided into a preshower detector, an electromagnetic calorimeter (ECAL) and a hadronic calorimeter (HCAL). Its main purpose is to provide identification of electrons and hadrons for trigger and offline analysis, with measurements of position and energy. The preshower cells are made from 14 mm thick lead plates followed by square scintillators, 10 mm thick. The scintillators are read out by wavelength-shifting (WLS) tubes. The ECAL comprises 70 layers, consisting of 2 mm thick lead plates and 4 mm thick polystyrene-based scintillator plates, corresponding to a length of $25X_0$. Light is collected by 1 mm WLS fibers traversing the whole station length. An energy resolution of

$$\frac{\sigma(E)}{E} = \frac{10\%}{\sqrt{E}} \oplus 1.5\% \tag{4.1}$$

(E in GeV) is sufficient to provide hadron rejection factor of about 100, as well as for π^0 reconstruction. The HCAL module is made of scintillator tiles embedded in an iron structure. The tiles are placed parallel to the beam direction, in a staggered arrangement. The overall transverse dimensions of the sensitive volume is 9×7 m with a iron depth of 1.5 m, providing $7.3\,\lambda_I$. Approximately 50 photoelectrons/GeV are expected to be detected, resulting in an energy resolution with 80 % statistical and a 5 % constant term.

The Muon detector [78] provides Muon identification and Level-0 trigger formation. It consists of four stations M2-M5 embedded in iron filter and a special station M1 in front of the calorimeter. A more detailed description is given in Chapter 5.

4.4.2 Front-end Electronics

The subdetectors will use a common architecture for the front-end electronics, which has to follow the specific trigger requirement and be radiation hard or tolerant[4], if mounted inside the detector. All analogue and digital signals arriving at 40 MHz will be stored in Level-0 pipelined buffers and wait for Level-0 trigger decision taken after a fixed delay of 3.2 μs. Events accepted at an average rate of 1 MHz are transmitted to short de-randomizing buffers to avoid overflow due to limited output speed. The data is then multiplexed, digitized (if they were still analogue) and sent to Level-1 buffers. The average rate of events accepted by Level-1 is 40 kHz. Events accepted pass zero suppression, are multiplexed and sent to the data acquisition system, located about 60 m from the detector.

4.4.3 Trigger Scheme

The LHCb trigger system must be selective and efficient in extracting the small fraction of interesting events from the large number of $b\bar{b}$ and other pp inelastic

[4] An electronic component is said radiation hard when it is tested and survive a dose of about 100 KRad. A radiation tolerant device is an electronic device that must survive small doses of radiation.

events. The trigger strategy is based on four levels: Level-0, Level-1, Level-2 and Level-3.

Level-0 comprises three high p_T triggers, operating on muons, electrons and hadrons. High p_T means higher than particles produced in most of the inelastic pp interactions (minimum-bias events). A pile-up veto that suppresses bunch crossings with more than one pp interaction was for seen in the LHCb technical proposal, but its implementation is under study. Operating at a bunch crossing frequency of about 40 MHz the level-0 trigger is designed to achieve a total suppression factor of 40. The latency of $3.2\,\mu$s is sufficient to cover the execution time of the algorithm ($\sim 2\,\mu$s) and to collect the input and deliver the decision to the front-end electronics ($\sim 1\,\mu$s).

Level-1 algorithm is still under study. It select events containing one or more secondary vertex and search for high p_T tracks. It operates at 1 MHz (Level-0 accept rate) and has a suppression factor of 25. The latency is variable and is largely determined by the algorithm execution time. The maximum latency is set to $256\,\mu$s.

Level-2 eliminates events with fake secondary vertices, by using momentum information. It operates at a rate of 40 kHz and achieves a suppression factor of 8. The latency is also dependent of the algorithm execution time, but an average of 10 ms is required.

Level-3 uses full and partial reconstruction of final states to select events associated with specific b hadron decays modes. For that, it makes use of all detector components, including the RICH. The suppression factor is about 25, the data recording rate is $\sim$200 Hz and the latency is estimated to be about 200 ms.

4.4.4 Data Acquisition System

The role of the data acquisition system [79] (DAQ) is to read zero-suppressed data from front-end electronics, to assemble complete events and to provide sufficient CPU power execution of the Level-2 and Level-3 trigger algorithms. The input rates are determined by the average event size ($\sim$100 KB) and the Level-1 accept rate (40 kHz). This results on a total data acquisition rate of 4 GB/s. The output rate is mainly determined by the Level-3 accept rate ($\sim$ 200 Hz), leading to a data storage requirement of about 20 MB/s.

Chapter 5

LHCb Muon System Overview

5.1 General Detector Structure

The LHCb muon detector [78] has a total area of about $435\,\mathrm{m}^2$ divided in five stations M1 to M5, as shown in Figure 4.1. The first station (M1) is located in front of the calorimeters and the following ones (M2-M5) are behind the calorimeters, embedded in iron filter to attenuate hadrons, photons and electrons. This shield has a total absorber-thickness of 20 nuclear interaction lengths. A muon must have at least 5 GeV of energy to penetrate this shield and reach the station M5. An additional shield behind M5 protects the station from machine related background and back splash from nearby LHC beam elements.

The muon system has inner and outer angular acceptances equal to 20 mrad and 306 mrad in the bending plane. In the non-bending plane, the inner and outer angular acceptances equal to 16 mrad and 258 mrad, respectively. This provides a geometrical acceptance of 20 % for muons from b decays, relative to the full solid angle.

The muon stations are equipped with chambers made of different technologies, as described in Section 5.6. Each station is divided in four regions (R1-R4). The regions are subdivided in sectors and the sectors are divided in x and y logical channels. A coincidence of two logical channels form a logical pad that is the information used by the muon trigger and the off-line reconstruction. Due to the different granularity requirements and the large variation in particle flux, the logical pads dimension are different in each station. A description and physical implementation of the logical layout is given in [78].

5.2 Performance Requirements

The main function of the muon system is to identify and trigger on muons produced in B decays. In order to achieve a muon trigger efficiency of at least 95 % within 20 ns time window, the station efficiency has to be higher than 99 %. This can be achieved by having several detector layers and taking the logical OR of these layers. Since the muon system must provide unambiguous bunch crossing identification, the detector time resolution should be considered. The detector efficiency is limited by the intense flux of charged and neutral particles, making the rate capability an important requirement. Moreover, the materials for the chamber must have good ageing properties, allowing 10 years of operation.

The chamber spatial resolution must allow the determination for p_T of triggering muons with 20 % resolution. This requires a good granularity in station M1 and M2, used to measure p_T. Since there are parallel layers of detectors, inclined tracks can hit more than one logical pad affecting the geometrical cluster size and deteriorating the granularity. In order to have an optimum granularity, the cluster size should be kept at about 1.2. To avoid any additional deterioration, crosstalk between readout channels should be minimized.

5.3 Readout Electronics

The readout electronics has to prepare the information required by the Level-0 muon trigger as fast as possible and must conform to the overall LHCb readout specifications [80]. The preparation for the Level-0 muon trigger corresponds to a formation of 26,000 logical channels, starting from 120,000 physical channels. Each logical channel must be tagged with the number of bunch crossing (BX) to which it belongs. The first step should be performed on the chamber, in order to reduce the number of LVDS links exiting the detector. The second step requires a time alignment of channels, because signals from different channels take different paths before being sent to the Level-0 pipelines and tagged with their BX identifiers. In addition to that, each front-end channel has a time behaviour that depends on the readout scheme and the chamber operating conditions.

The readout consists of front-end boards (FEB), intermediate boards (IM), off-detector boards (ODE) and service boards (SB). The front-end boards are located on the chambers and they house the amplifier, shaper, discriminator (ASD) chips and the the chips responsible to form the logical channels. The IM boards are on the side of the muon station and they are used to generate logical channels for regions where the logical channels are made of physical channels belonging to different chambers. ODE boards is where the data is synchronized and send to the Level-0 muon trigger. They are also located on the side of the muon station and it comprises Level-0 pipelines, Level-1 buffers and the interface to the data acquisition (DAQ). The service boards (SB) are used to control and monitor the FEB and the ODE. The information is sent to the experiment control system (ECS). A simplified scheme of the muon architecture is shown in Figure 5.1 and a detailed description can be found in [81].

The physical channels are processed by ASD chips, located on the FEB. The formation of logical channels from physical channels is achieved using an integrated circuit for DIagnostics, time Alignment and LOGics (DIALOG). The DIALOG chip also allows programming of a delay for each single input channel and contains features useful for system setup, monitoring and debugging. Once generated, the logical channels are sent to the ODE, where the BX identifier is assigned, and the data sent to the Level-0 trigger.

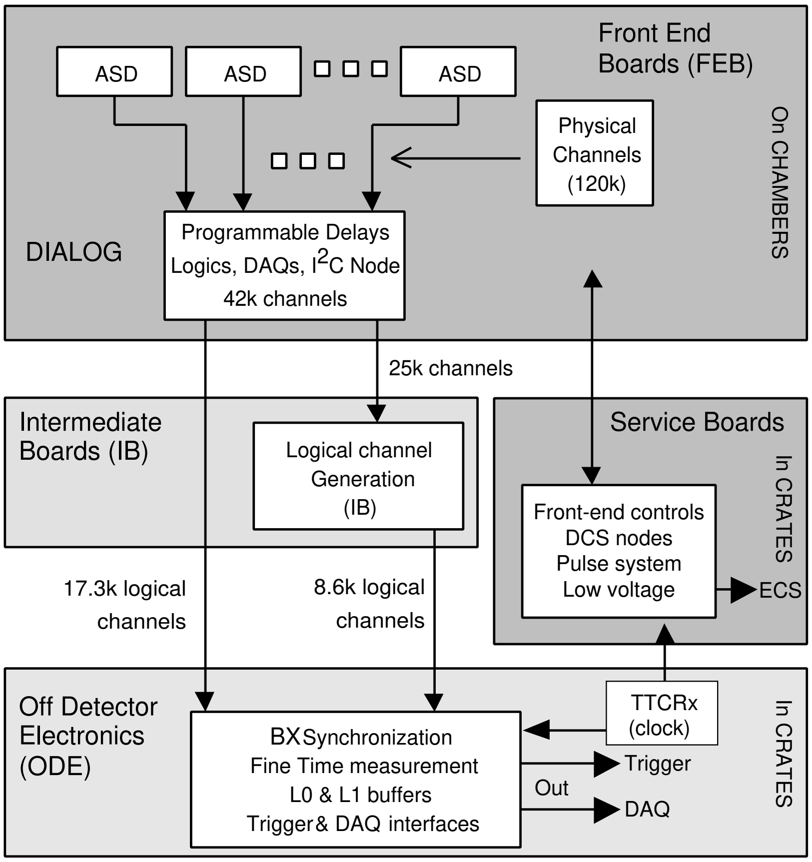


Figure 5.1: Simplified scheme of muon system readout architecture.

5.4 Level-0 Muon Trigger

The Level-0 muon trigger looks for muon tracks with a large transverse momentum (p_T). It searches for hits defining a straight line through the five muon stations and pointing toward the interaction point. The track position in the first two stations allows determination of p_T. For a correct execution of the algorithm the trigger requires projectivity at each station.

The Level-0 muon trigger is implemented with the four quadrants of the muon system treated independently. Track finding in each region of a quadrant is performed by 12 processing units. A processing unit collects data from pads and strips from five stations. A detailed description of the trigger algorithm and performance is given in [82].

5.5 Muon Identification

Efficient muon identification is important in the reconstruction of physics channels with muons in the final state. For rare decays, such as $B_s^0 \rightarrow \mu^+\mu^-$ it is essential to have high muon identification efficiency keeping the misidentification of other particles, mainly pions, as low as possible.

Well reconstructed tracks that have at least one hit in the vertex detector and are within the geometrical acceptances of stations M2 and M3 are extrapolated from the last tracking station to the muon system. This track is identified as a muon if hits are found inside a rectangular search window centered on the track extrapolation. The number of hits required depends on the track momentum. For nominal background, the muon identification efficiency in $b \rightarrow \mu X$ events is 94 % and the pion misidentification probability is 1.5 %. In 61 % of the cases the pion is misidentified because it decays in flight to a muon and in 27 % of the cases the misidentification occurs because a muon from another hadron decay is close to the pion. The remaining 12 % of pion misidentified result from some combination of background hits and ghost hits.

The performance of the muon identification algorithm has been tested using reconstructed charged tracks, simulated with nominal parameters of the muon system. Details of this study are given in [83].

5.6 Chamber Technologies

The combination of physics goals and background conditions have determined the choice of technologies. The main parameters considered were the rate capability, ageing conditions and time and spatial resolution. Cost and performance robustness were also taken into account.

The chamber technology used in the various regions of the muon system is mainly determined by the rates experienced by the detectors. The highest rates are in station M1 which is not protected by any shield. Most detector regions, about 52 % of the total area, are equiped Multi Wire Proportional Chambers [84] (MWPC) operating in low gain mode. In the outer regions (R3 and R4) of the last two stations (M4 and M5) the rate is below 1 KHz/cm^2 and Resistive Plate Chambers [85] (RPC) are used. The same chamber dimensions have been chosen for MWPCs and RPCs, making one technology backup of the other, in some regions of the muon system. Both MWPC and RPC are described in following sections.

The most challenging area are the inner regions (R1 and R2) of the first station (M1), where the rate goes up to 460 KHz/cm^2. The technology for this region must still be selected. However it represents an area of 2.9 m^2, thus less than 1 % of the total muon system area. Various technologies such as asymmetric MWPC or triple GEM detectors [86] are under investigation. In this chapter I am concentrating on the MWPC description and requirements, because this technology is directly related to my thesis project.

5.7 Resistive Plate Chambers

RPC are parallel plate chambers with a gas gap between two resistive electrodes. The readout occurs via capacitive coupling to external strip or pad electrodes, which are fully independent of the sensitive element. Ionizing particles create electron-ion clusters in the gas, where an intense constant electric field is present between two parallel plates. Multiplication in the gas, averaged over the gap, is about 10^7. The plates are made of Bakelite, a phenolic resin with high bulk resistivity between 10^9 and 10^{11} Ωcm. Due to the exponential growth of the avalanche, the output signal induced on the readout electrodes has a very fast rise time (∼1 ns). This results in excellent time resolution of ≤ 2 ns and there for

Parameter	Design Value
Gas gap	2 mm
Operating voltage	9-10 KV
Gas mixture	$C_2H_2F_4/C_4H_{10}/SF_6$ (95:4:1)
Gas gain	$\approx 10^7$
Avalanche charge	≈ 15 pC
Time resolution	≤ 2 ns
Threshold	40 fC
Bakelite bulk resistivity	$(8 \pm 2) \times 10^9\,\Omega$cm

Table 5.1: Main RPC parameters.

good adaptation for fast triggering. In order to achieve full efficiency, a threshold of 40 fC is adequate.

This chamber has limitations to high rates, because of the voltage drop on the electrodes. The main characteristics of the RPC detectors of the LHCb are summarized in Table 5.1. A better description of this chamber, together with operation conditions, simulations and test results, is reporter in [85], [87] and [88].

5.8 Multi Wire Proportional Chambers

A schematic diagram of one MWPC sensitive gap is shown in Figure 5.2. The chamber has a symmetric cell with anode-cathode distance of 2.5 mm and anode wire spacing of 1.5 mm. The gas volume of 5 mm thickness is filled with a non-flammable gas mixture of $Ar/CO_2/CF_4$ (40:50:10). Table 5.2 summarizes the main MWPC parameters. A muon crossing the gas gap of 5 mm leaves on average of 50 e^- (100 e^-/cm) that drift to the wires in the electric field with a gas gain of 10^5, this corresponds to about 0.8 pC of charge. The electrons and the ions moving in the avalanche close to the wire induce a negative signal on the wire

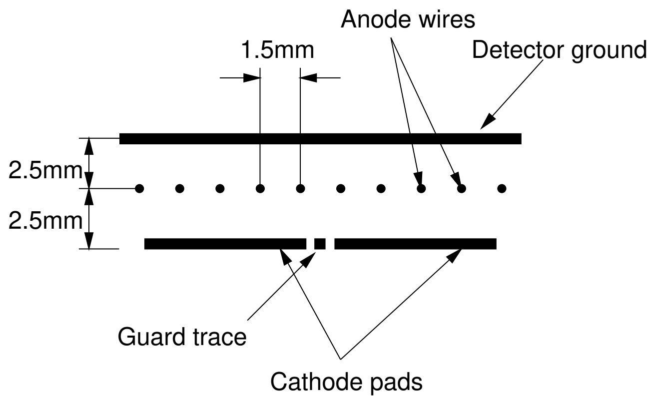


Figure 5.2: Schematic diagram of one MWPC sensitive gap.

and a positive signal with the same shape and about half the magnitude on the cathode.

Each MWPC contains four sensitive gaps which are connected as two double gaps to two front-end channels. This provides redundancy and insure a double gap efficiency of about 99 %. Depending on the position in the muon system, the chambers can have anode readout, cathode readout or both anode and cathode readout. Anode pads are made by grouping 4 to 42 wires, varying from 6 mm to 62 mm, to match the required granularity. In the muon system there are 864 four-gap chambers with about 2.5×10^6 wires and 80,000 front-end channels.

A full simulation of the MWPC performance is described in [89]. Prototype chambers have been evaluated in several test-beam studies. A double gap MWPC using a fast gas and a wire spacing of 1.5 mm has a time resolution of about 3 ns. A threshold of 10 fC is adequate to achieve full efficiency and fast time resolution. Space charge effects due to accumulation of ions are not expected for rates of up to 10 MHz/cm^2. The results are presented in [90–95].

Parameter	Design Value
Gas gap	5 mm
Wire spacing	1.5 mm
Wire diameter	30 μm
Operating voltage	3.0-3.2 KV
Gas mixture	$Ar/CO_2/CF_4$ (40:50:10)
Gas gain	$\approx 10^5$
Primary ionization	$\approx 100\,e^-/cm$
Charge/5 mm track	≈ 0.8 pC
Threshold	10 fC

Table 5.2: Main MWPC parameters.

5.8.1 Cross talk

Two sources of crosstalk can be distinguished in the MWPC [96]: directly induced crosstalk and electrical crosstalk. The directly induced crosstalk happens if a particle crosses the chamber close to the edge of a pad. In this case the amount of crosstalk between cathode pads depends on the wire pitch and the cathode-wire distance. To keep the crosstalk below 20 %, the cathode pad should be larger than 2.2 cm, assuming a threshold of six primary electrons. The directly induced crosstalk in the wire pads is negligible.

Electrical crosstalk between pads depends on several factors, including the amplifier input impedance, the pads capacitance and mutual pad to pad capacitances. Between wire pads it can only be limited by a low amplifier input impedance. Between cathode pads it can be limited by using guard traces between the pads. If a low impedance amplifier is used for the pads readout, this type of crosstalk is not significant.

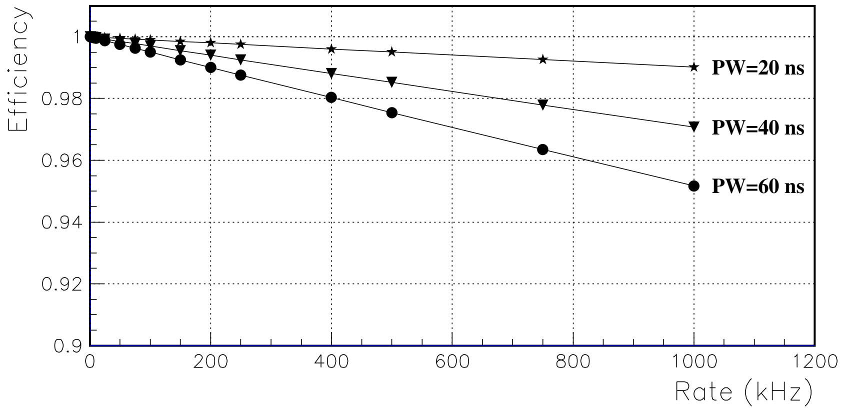


Figure 5.3: Efficiency as a function of signal rate for different pulse width (PW).

5.8.2 Front End Requirements

Several requirements must be satisfied by the front-end electronics. Since both cathode and anode pads should be read, the ASD chip must be able to handle both positive and negative polarities. The average signal charge collected in the first 10 ns is 40 fC for a double gap chamber with a gas gain of 10^5, but Landau fluctuations result in a large signal dynamic range. Since the chamber signal has an ion tail, with a constant of $t_0 \approx 1.5$ ns, a dedicated ion tail cancellation network filter is needed. In order to guarantee optimum tail cancellation for more than 95 % of the signals, the ASD chip must be able to handle 150 fC of input charge.

In the highest rate regions the maximum total dose is about 1 MRad, which requires the use of radiation tolerant chips. These high rates have a large impact on the detector efficiency due to dead time of the ASD chip output pulse width. Figure 5.3 shows how the pulse width affects the single layer efficiency. Since a pulse width below 50 ns is not feasible, a maximum signal rate of 1 MHz per physical channel has been defined. To minimize the dead time, a unipolar pulse shape is required.

The wire signals are AC coupled and the high voltage loading time is τ =

Parameter	Specification
Input Polarity	positive and negative
Detector capacitance	40-250 pF
Maximum signal rate	1 MHz
Maximum total dose	1 MRad
Input resistance	$< 50\,\Omega$
Average pulse width	< 50 ns
Peaking time	~ 10 ns
Shaping circuit	unipolar $2\times$ pole/zero
Baseline restorer	1-5 μs response time

Table 5.3: Front-end electronics requirements.

$R_L C_{det} = 100\,\mu$s. This implies large baseline fluctuations at high rates for a unipolar signal processing chain. Therefore, the unipolar signal processing requires a baseline restoration (BLR) to avoid baseline fluctuations.

In order to limit the crosstalk due to capacitive coupling, the amplifier input impedance has to be smaller than $50\,\Omega$. In addition to that, the amplifier should keep its performance for input capacitances up to 250 pF. The noise level should be as small as possible. Since the detector capacitance represents a series noise source, the noise level is completely determined by the front-end design. Finally, the power dissipation of the front-end chip should be low to keep thermal gradients on the chambers to a minimum. Table 5.3 summarizes the ASD chip requirements.

Various front-end chips have been studied in order to find the optimum solution for the muon system. The candidates were PNPI, ASDQ++, SONY++ and CARIOCA. The PNPI electronics [90] consists of an on-chamber preamplifier and an off-chamber main amplifier. ASDQ++ [91,97] is a chip developed for the COT chamber at Fermilab. The SONY++ [92, 98] is a front-end chip developed for the ATLAS TGCs. The first three electronics were tested on a MWPC, but gave unsatisfactory results. The preferred solution for the muon system, however, is the CARIOCA [99]. It consists of a new chip that was developed for the MWPCs of the muon system and is described in the following chapters.

Chapter 6

CARIOCA - A Readout Chip for the LHCb Muon System

6.1 Introduction

CARIOCA (**C**ERN **A**nd **RIO** **C**urrent-mode **A**mplifier) is an octal amplifier-shaper-discriminator circuit, with baseline restoration, dedicated to the Multi Wire Proportional Chambers (MWPC) of the LHCb Muon system. It is developed in $0.25\,\mu$m complementary metal-oxide-semiconductor (CMOS) technology, that operates at 2.5 volts. The main novelty of the CARIOCA chip lies in the amplifier, which is developed in the current-mode approach. Its amplifier is developed in the current-mode approach, that is attractive for fast circuits, and has an adjustable gain allowing different detector applications. The main task of this electronics is to amplify the chamber signal, before discrimination. For that, several stringent requirements must be satisfied, as described in the following section.

The development of the chip, the circuit was divided into various sub-circuits, allowing the realization and test of several prototypes. In this chapter I am describing the final circuit topology and design, together with the simulation results. The sub-circuits design and the prototype production, as well as the measurement results are discussed Chapter 7.

6.2 Overview and Specifications

The task of the wire chambers of the LHCb Muon System is to measure the arrival time of muons to better than 3 ns. The chamber signal is characterized by a fast rising edge and a long $1/(t + 1.5)$ tail, where t is the time in ns, going over into a DC current lasting for about $20\,\mu s$. This signal has to be shaped to a unipolar narrow pulse in order to cope with the high rates expected in the experiment and limit the dead time of the trigger.

A detector gas gain of 10^5 together with an amplifier peaking time of 10 to 15 ns is found to be the optimum working point for this detector. This results in an average pulse height of about 60 fC of charge, when referred to a delta input signal. To obtain a narrow pulse, a tail cancellation circuit has to be implemented and which should correctly work for at least 99 % of chamber signals (up to 250 fC input charge). In order to allow the desired threshold of 10 fC, the equivalent noise charge (ENC) at the input should not exceed 2 fC up to the largest detector capacitance of 250 pF. In addition, the amplifier input impedance should be lower than $50\,\Omega$ to keep crosstalk low enough for chamber operation.

High rates of up to 800 KHz per channel in some detector regions require fast pulse shaping and baseline restoration circuits to compensate for baseline shifts and fluctuations. A total accumulated dose of 1 MRad during the life of the experiment requires radiation tolerant chip technology.

6.3 Topology and Architecture

The CARIOCA integrated circuit is developed in two versions: one for cathode readout (positive input polarity version) and another for anode readout (negative

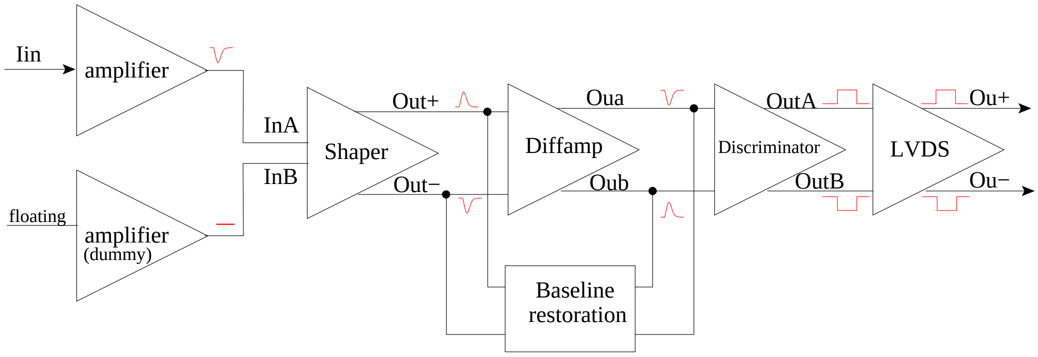


Figure 6.1: CARIOCA channel block diagram.

input polarity version). Each chip is composed of eight identical channels and a bias network, that provides the bias voltage and current to the channels. The general analog features of each CARIOCA channel are shown in Figure 6.1.

The input of the CARIOCA circuit is pseudo-differential, consisting of two identical current-mode amplifiers. One amplifier is connected to the chamber pad through a trace on the printed circuit board (PCB). The other, *dummy* amplifier, has a floating input and it is used to provide DC balance to the shaper and common mode rejection to pickup, crosstalk and noise on the power supply lines. Following the amplifier there is a shaper circuit and a differential amplifier which provide further gain while the ion and the amplifier tails are suppressed. The differential amplifier output is feed into the discriminator. The discriminator output is sent to the LVDS cell, where it is converted to external low level signals. Each CARIOCA channel draws approximately 10 mA from the 2.5 V supply, dissipating about 25 mW.

CARIOCA sub-circuits are described below. A detailed schematic of each sub-circuit and the bias network are show on the Appendix B.

6.4 Current-mode Amplifier

Fast low noise amplifiers are usually based on charge or transimpedance circuits and have limited performance at large detector capacitance. This limitation is due to the fact that the feedback network, which converts the output voltage into an input current, must have low impedance in order to keep the closed loop gain small enough to get a high speed response. As a consequence, the charge-to-voltage gain is smaller and the noise performance reduced.

Current-mode architectures are an attractive alternative to the more conventional voltage-mode ones for very fast circuits. In this approach, the signal is processed in the current domain, thus avoiding charge and discharge of parasitic capacitances and keeping the internal nodes of the circuit at low impedance values. Therefore current-mode techniques combined with deep sub-micron technology provide the opportunity of build analog circuits with high speed and low power consumption.

The CARIOCA amplifier input stage is a cascode [100] structure with a large input transistor, followed by a voltage to current converter and a current mirror. The mirror feeds the current to the output stage and back to the input stage. The input transistor ($N1$) is a n-channel with a length of $0.7\,\mu$m and width $1600\,\mu$m, corresponding to an input capacitance of 6 pF. This transistor operates in moderate inversion and has 42 mA/V transconductance (g_m) at a drain current of about 3.2 mA. The folded transistor ($N2$) is chosen to have an open loop gain of about 30. The feedback capacitor (C_{feed}) of 406 fF is used to split the first two poles of the circuit and improve the stability. The design of both positive and negative polarity amplifiers, shown in Figure 6.2, are very similar and they have the same working principle. The main difference is the output stage current mirror ($N5/N6$) that uses nmos devices on the cathode readout amplifier and pmos on the one for anode readout. This difference is due to the current input polarity, which forces the replacement of the pmos transistors by nmos transistors. Al-

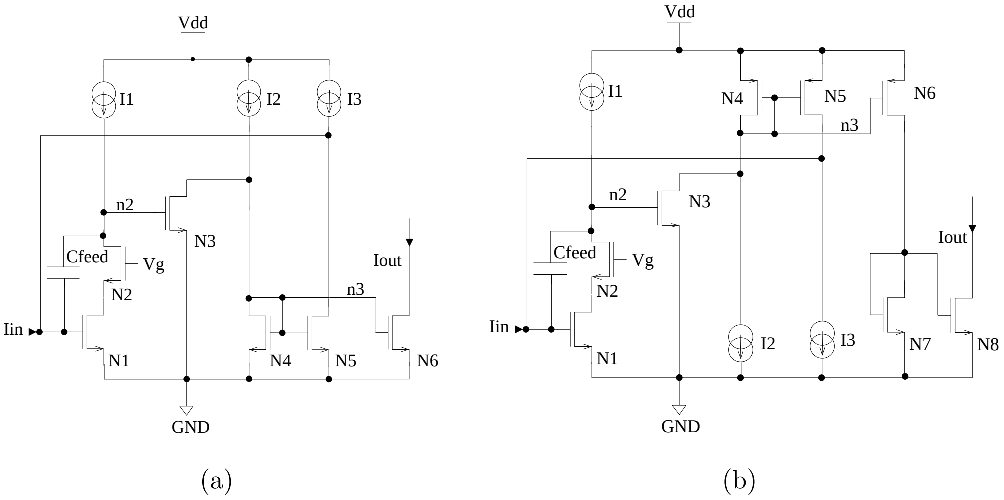


Figure 6.2: Simplified schematic of the positive (a) and negative (b) CARIOCA input polarity amplifiers.

though nmos and pmos transistors do not have the same properties, both circuits are optimized to have almost the same operating points and the differences are small.

Current sources are made with high impedance cascode transistors. A global bias circuit, shown on the Appendix B, provides the required bias voltages for the circuit, setting the correct DC voltage level.

6.4.1 Working Principle

The current coming from the detector is sensed by the input transistor $N1$ and is integrated by the feedback capacitor (C_{feed}). When this current is positive, the voltage on the input node increases and it allows the current to flow on the input transistor, reducing the voltage on the node $n2$. When the voltage on $n2$ becomes more negative, less current flows on $N2$ and the voltage on the node $n3$ becomes more positive allowing more current to flow in the output transistor $N5$. The current flowing on this transistor is mirrored to $N4$ and then to $N6$. The mirror gain of 6 is given by the transconductance ratio of $N5$ and $N6$. Folded cascode transistors with small size, on the drain of the transistor $N5$ and $N6$ (not shown) are used to provide a small output conductance and thus keep the amplifier insensitive to the input capacitance spread.

If the current on the input is negative, the inverse occurs and the output current is also negative. Since we want to have both amplifiers with the same output polarity, the current of the negative input polarity amplifier is inverted by an additional current mirror ($N7$ and $N8$). This is done to provide the same voltage polarity to the shaper input, independent of the amplifier used. This last stage slows down the circuit, adding 1 ns to the signal peaking time.

Figure 6.3 shows the simulated output voltage waveforms on the node between the amplifier and the shaper. The negative polarity amplifier has a larger tail than the positive one, as a consequence of different pole positions. In addition, the positive polarity amplifier output voltage has a small undershoot.

The transfer characteristics of both amplifiers is shown in Figure 6.4. The positive amplifier has a higher gain (3.0 mV/fC) than the negative one (2.7 mV/fC) for an input capacitance of 60 pF. This difference is due to the output stage configuration. The amplifier simulated sensitivity and peaking time dependence on the input capacitance is shown in Figure 6.5 for an input charge of 60 fC. Considering the MWPC pad capacitance range (50 pF to 250 pF) the sensitivity decays from 3.2 mV/fC (2.3 mV/fC) to 2.1 mV/fC (1.6 mV/fC) and the peaking time increases from 7 ns (7 ns) to 14 ns (15 ns) for the positive (negative) input polarity amplifier. Although these variations appear to be high, they satisfy the requirements.

6.4.2 Saturation Behaviour

The CARIOCA amplifier is designed to work up to an input charge of 400 fC. In order to achieve this requirement, the positive polarity amplifier current source

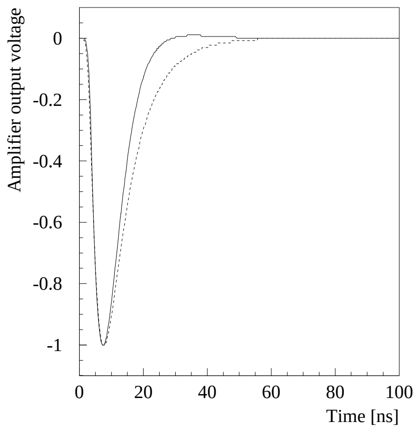


Figure 6.3: Normalized output voltage of the positive (full line) and negative (dashed line) input polarity amplifiers for a delta input charge of 60 fC at 60 pF input capacitance.

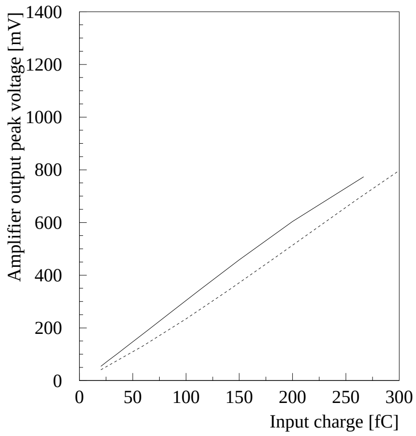


Figure 6.4: Simulated transfer characteristics (output peak voltage versus input charge) of the positive (full line) and negative (dashed line) input polarity amplifiers at an input capacitance of 60 pF. Both amplifiers show a good linearity up to 270 fC. The gain is about 3.0 mV/fC and 2.7 mV/fC for the positive and negative amplifiers, respectively.

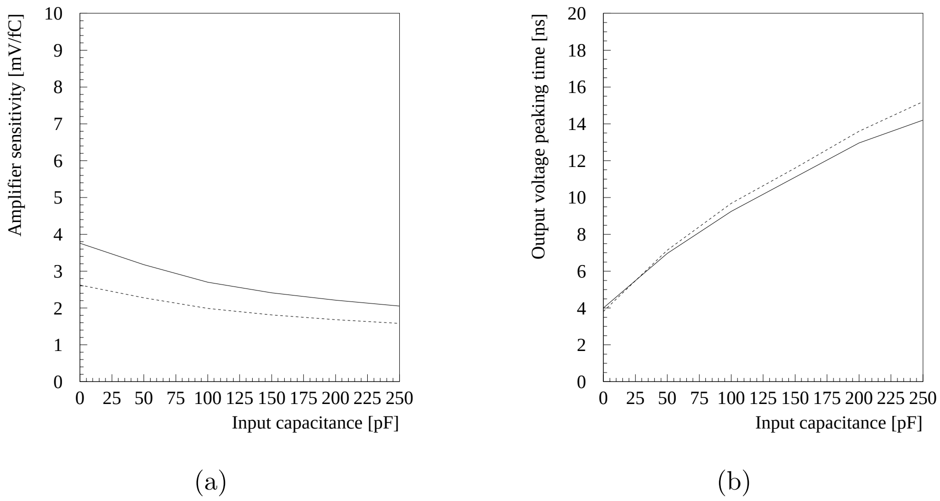


Figure 6.5: Sensitivity (a) and peaking time (b) of the positive (full line) and negative (dashed line) input polarity amplifiers as a function of the input capacitance.

I_2 drives more current compared to the negative one. For the negative input polarity amplifier the current flows in one transistor (N_3), forcing the voltage on the node n_2 to increase and letting the voltage on n_3 swing. On the positive polarity amplifier the saturation occurs because the current is divided between the transistors and the voltage on n_3 is limited, restricting the gate voltage of the output transistors. When this voltage goes to a maximum, the transistors are off and can not drive more current. The voltage on the node n_3 can be increased adding more current to N_3, allowing a higher voltage swing on n_2 and $n3$. This extra current is obtained introducing an additional current, that is described in Section 7.7.2.

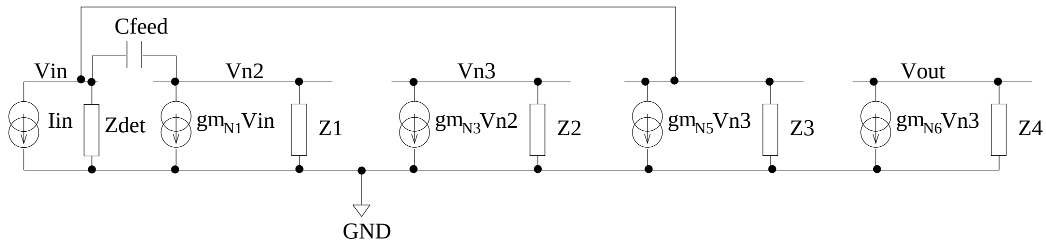


Figure 6.6: Small signal equivalent circuit of the CARIOCA amplifier.

6.4.3 Small Signal Model

Figure 6.6 shows the small-signal equivalent circuit of the CARIOCA amplifier connected to a detector. The detector is considered as a voltage source with very high resistance, as a consequence $Z_{det} \approx 1/(sC_{in})$. The amplifier input stage is a common-source stage and can be represented as a current source controlled by a voltage source with transconductance gm_{N1}. The consecutive stages follow the same rule. The impedances Z_1, Z_2 and Z_3 represent the total impedance at the current source node of I_1, I_2 and I_3, respectively, including transistors input and output impedances.

The equations that describe the system can be written as:

$$I_{in} + \frac{V_{in}}{Z} + gm_{N5}V_{n3} - (V_{in} - V_{n2})C_{feed}s = 0 \tag{6.1}$$

$$gm_{N1}V_{in} + \frac{V_{n2}}{Z_1} - (V_{n2} - V_{in})C_{feed}s = 0 \tag{6.2}$$

$$gm_{N3}V_{n2} + \frac{V_{n3}}{Z_2} = 0 \tag{6.3}$$

$$gm_{N6}V_{n3} + \frac{V_{out}}{Z_{out}} = 0 \tag{6.4}$$

where $s = iw$, gm is the transistor transconductance, V_x is the voltage on the nodes x and Z represents the equivalent impedance of Z_{det} in parallel to Z_3. This impedance can be approximated to $Z \approx Z_{det} = 1/(sC_{in})$, considering that an ideal current mode amplifier has zero input impedance and infinite output impedance.

Solving these equations we find that the circuit has a transfer function with one zero and three poles. The feedback and output currents are given by:

$$\frac{I_{feed}}{I_{in}} = -\frac{(gm_{N1} + C_{feed}s)G}{gm_{N1}G + (-C_{feed}(1 + gm_{N1}Z1 - G) + C_{in})s - C_{feed}C_{in}Z1s^2} \quad (6.5)$$

$$\frac{I_{out}}{I_{in}} = \frac{gm_{N6}/gm_{N3}(gm_{N1} + C_{feed}s)G}{gm_{N1}G - (C_{feed}(1 + gm_{N1}Z1 - G) - C_{in})s - C_{feed}C_{in}Z1s^2} \quad (6.6)$$

where

$$G = gm_{N3}gm_{N5}Z_1Z_2 \quad (6.7)$$

and

$$Z_i = \frac{1 + R_iC_is}{sC_i} \ . \quad (6.8)$$

The input impedance is given by:

$$Z_{in} = \frac{1 - C_{feed}Z_1s}{gm_{N1}G + (C_{feed}(1 + gm_{N1}Z1 - G) - C_{in})s + C_{feed}C_{in}Z1s^2} \ . \quad (6.9)$$

At low frequency these equations can be written as :

$$\frac{I_{feed}}{I_{in}} = -1 \ , \quad \frac{I_{out}}{I_{in}} = \frac{gm_{N6}}{gm_{N5}} \ , \quad Z_{in} = \frac{1}{gm_{N1}G} \ . \quad (6.10)$$

6.4.4 AC Analysis

The small signal frequency response of the CARIOCA amplifier, from HSPICE simulation [101], is shown in Figure 6.7. The bandwidth[1] is 22 MHz and 15 MHz for the positive and negative polarity amplifiers, respectively. Both amplifiers show a small signal gain around -30 dB. The input impedance stays smaller than 50 Ω for both amplifiers, as shown in Figure 6.8.

[1] The bandwidth is defined as -3 dB crossing frequency of the closed loop gain curve.

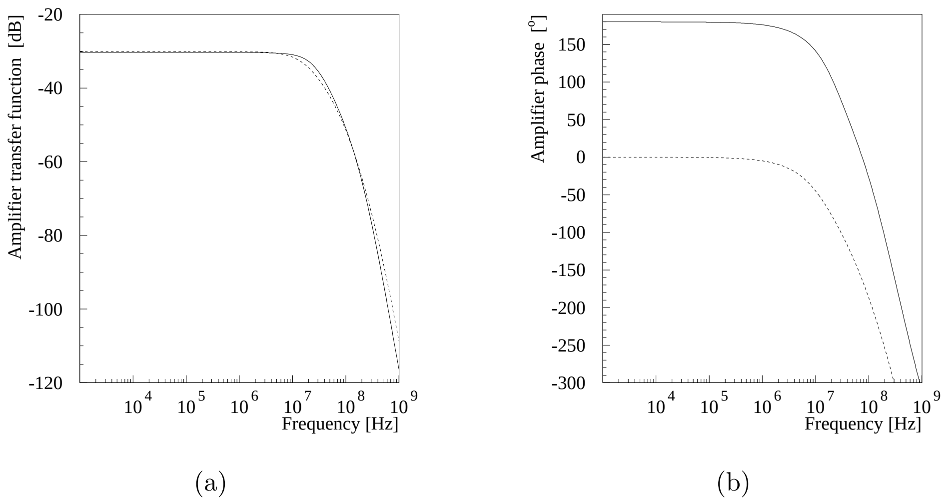


Figure 6.7: Closed loop gain (a) and phase (b) versus frequency for the positive (full line) and negative (dashed line) polarity amplifiers. The -3dB point is at 22 MHz and 15 MHz for the positive and negative polarity amplifiers, respectively.

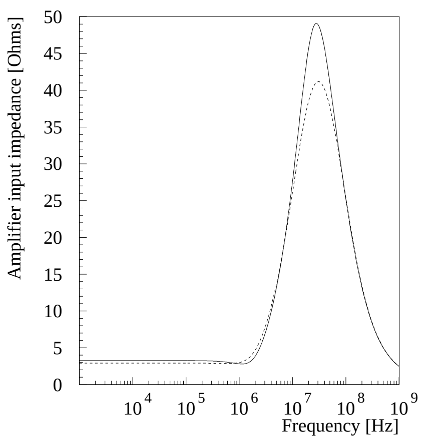


Figure 6.8: Input impedance of the negative (dashed line) and positive (full line) input polarity amplifiers.

6.5 Shaper

The CARIOCA shaper is a one stage pole/zero filter with 2-poles and 2-zeros. This piece of the CARIOCA circuit was not designed by me, but by somebody else [102]. The input stage is a current-to-voltage converter shown in Figure 6.9. The output current from the amplifiers (I_{amp} and I_{dummy}) are converted into voltage (V_{inA} and V_{inB}) by a $5\,\mathrm{K}\Omega$ resistor and these voltages are sent to the shaper inputs. A simplified schematic of the shaper circuit is shown in Figure 6.10. It consists of a differential amplifier in a folded cascode configuration with common-mode feedback. The DC output voltage is set by the common-mode voltage (V_{CM}) via $5\,\mathrm{K}\Omega$ resistors. The common-mode voltage is chosen to be 1.27 V to explore the maximum dynamic range of the signals.

The tail cancellation is performed by a double pole-zero compensation network [103, 104] composed by R_1, R_2, R_3, C_1 and C_2. At high frequency there is no feedback and the circuit is an open loop. For lower frequencies it provides feedback and reduces the gain at these frequencies. Thus the pole/zero network transfer function is given by the ratio of the closed loop gain at high frequency divided by that at low frequency and it can be written as:

$$H(s) = \frac{1 + ((R_1 + R_2 + R_3)C_1 + R_2C_2)s + (R_1 + R_3)R_2C_1C_2s^2}{(1 + R_1C_1s)(1 + \frac{C_2s}{1/R_2+1/R_3})} \tag{6.11}$$

where $\mathrm{R}_1 = 20\,\mathrm{K}\Omega$, $\mathrm{R}_2 = 2.7\,\mathrm{K}\Omega$, $\mathrm{R}_3 = 14\,\mathrm{K}\Omega$, $\mathrm{C}_1 = 2\,\mathrm{pF}$ and $\mathrm{C}_2 = 1.1\,\mathrm{pF}$. This equation can be simplified and written as

$$H(s) = \frac{s + 1/\tau_1}{s + 1/\tau_2} \cdot \frac{s + 1/\tau_3}{s + 1/\tau_4} \tag{6.12}$$

where τ_1=9 ns, τ_2=2.6 ns, τ_3=80 ns and τ_4=40 ns.

Figure 6.11 shows the shaper output for positive and negative input polarity amplifiers with delta input charge of 60 fC. These waveforms have an undershoot, due to the tail cancellation optimization. The shaper differential output peak voltage, is shown in Figure 6.12 as a function of the input charge. It shows a

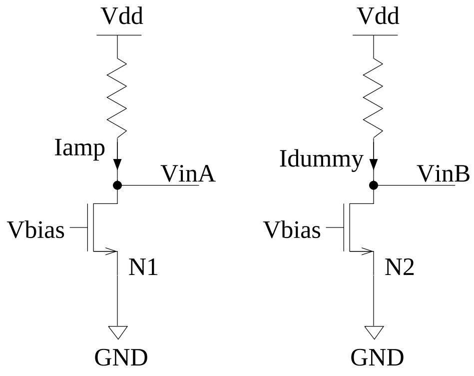


Figure 6.9: Current to voltage converter at the input of the shaper circuit. I_{amp} and I_{dummy} are the currents that come from the amplifiers and V_{inA} and V_{inB} are the voltages sense by the shaper input transistors $N3$ and $N4$, respectively.

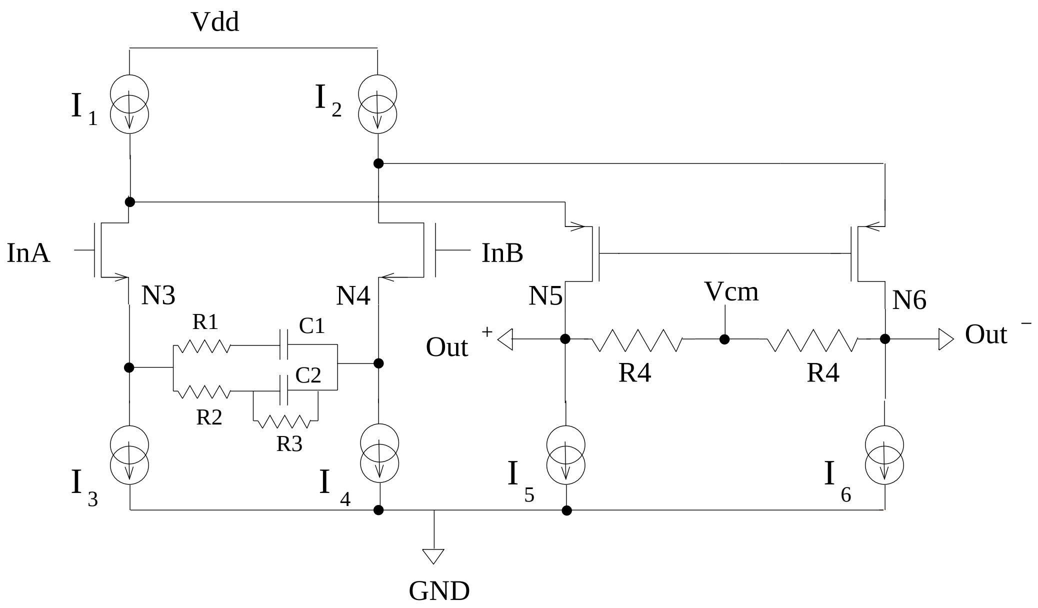


Figure 6.10: Simplified schematic of the shaper circuit.

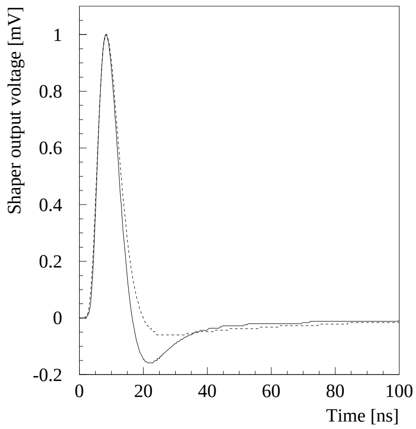


Figure 6.11: Normalized positive (full line) and negative (dashed line) amplifiers and shaper differential output voltage, for a delta input charge of 60 fC and 60 pF input capacitance.

good linearity up to about 200 pF input capacitance. The gain is about 4.0 mV/fC and 3.6 mV/fC for the positive and negative polarity amplifiers, respectively. The sensitivity and the peaking time dependence on the input capacitance is shown in Figure 6.13.

6.5.1 AC Analysis

The shaper circuit is designed with a speed such that the amplifier peaking time is not significantly degraded. The contribution to the peaking time is about 1 ns. Therefore the dominant high frequency pole is located at about 140 MHz. Figure 6.14 shows the frequency response - gain and phase Bode plots - for the positive and negative polarity amplifiers followed by the shaper circuit, obtained using the HSPICE simulator. The voltage gain peaks at about -37 dB in the range of 6 to 23 MHz.

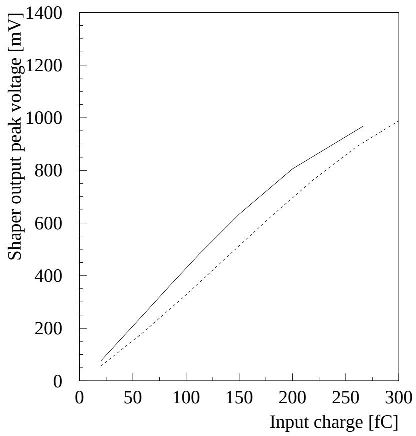


Figure 6.12: Positive (full line) and negative (dashed line) input polarity amplifiers and shaper simulated output peak voltage versus input charge, at 60 pF input capacitance. The gain is about 4.0 mV/fC and 3.6 mV/fC for the positive and negative amplifiers, respectively.

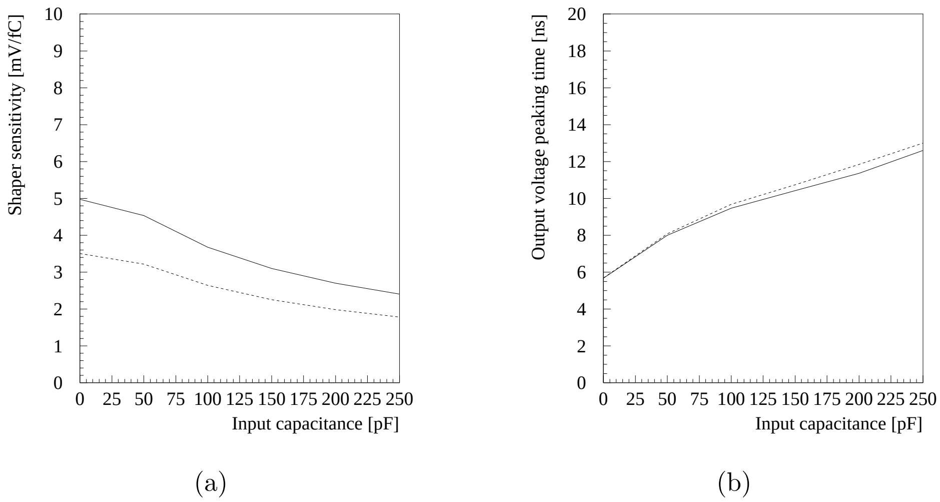
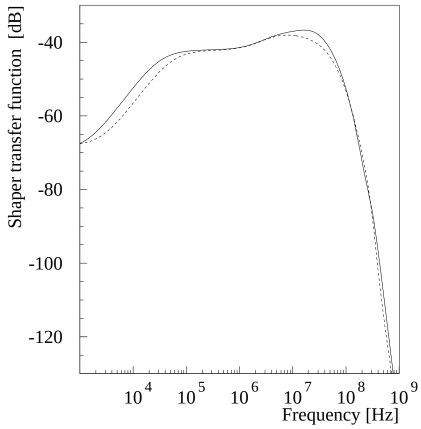
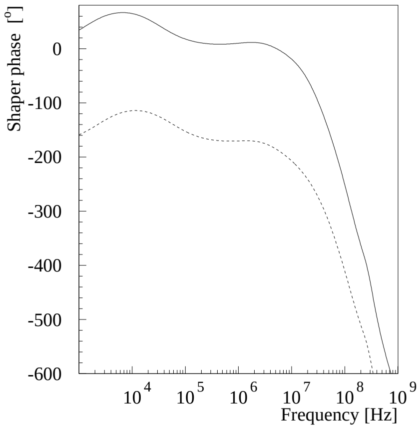


Figure 6.13: Sensitivity (a) and peaking time (b) of the positive (full line) and negative (dashed line) input polarity amplifiers and shaper as a function of the input capacitance.



(a)



(b)

Figure 6.14: Positive (full line) and negative (dashed line) input polarity amplifiers and shaper frequency response - gain (a) and phase (b) Bode plots. Both amplifiers shows a gain of about -37 dB in the range of 6 to 23 MHz with the -3dB point at 140 MHz (dotted line).

6.6 Differential Amplifier

The differential amplifier follows the basic design shown in Figure 6.15. It serves as gain and shaping amplifier. The gain is set by the load impedance Z and the source impedance Y. The source impedance is a combination of resistors and capacitances, making a pole/zero structure to cancel the time constant of the amplifier output. Since the positive and negative input polarity amplifiers have a different tail, two different pole/zero structures are chosen, i. e., the value of Y differs from positive to negative input polarity version.

The DC output voltage of the differential amplifier is established by common mode feedback. The output nodes are connected to the gates of N_5/N_6 and N_9/N_{10}, that operate in their linear region as resistors, with 100 mV across N_5/N_6 and 62 mV across N_9/N_{10}. Common mode gain is achieved by modulating the

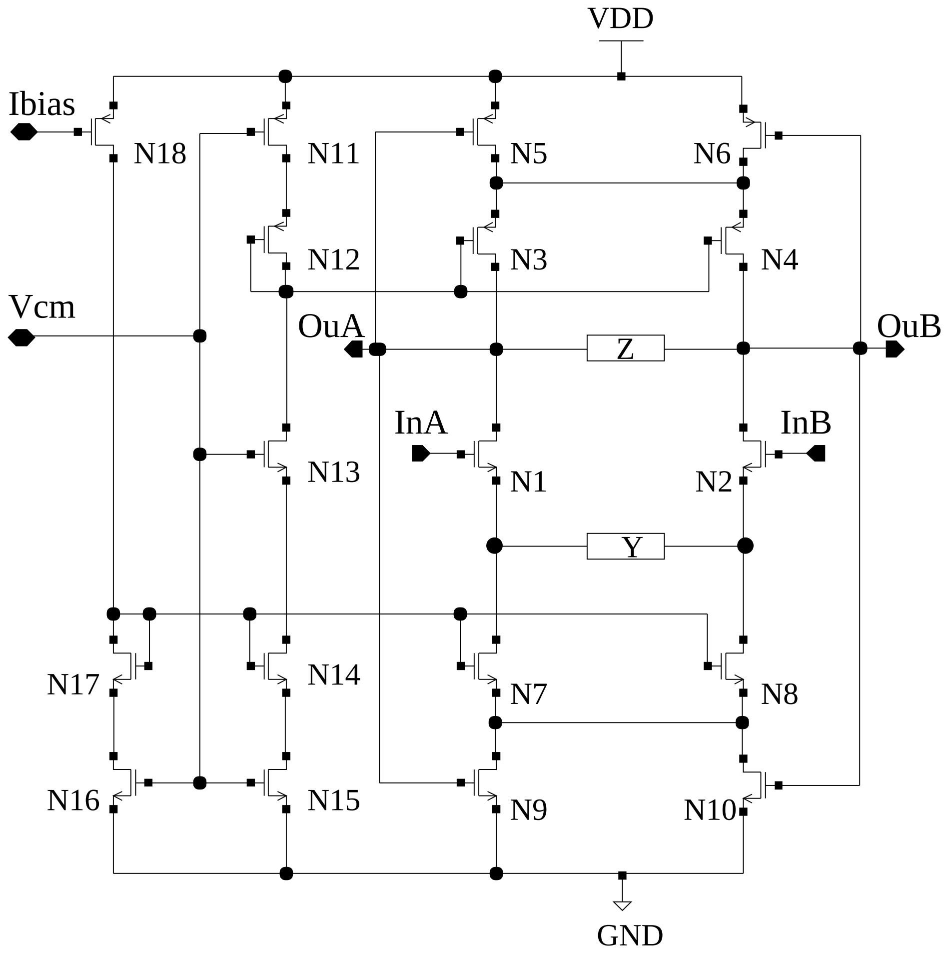


Figure 6.15: Differential amplifier schematic.

field effect transistor (FET) resistances via common mode output voltage. Common mode feedback drives the common mode output voltage to the reference voltage Vcm. This reference voltage is common to the differential amplifier and the baseline restoration circuit (Section 6.7) and is set to 1.5 V. The bias current (I_{bias}) is set by a bias network shown on the Appendix B. The drain currents of the input pair N_1/N_2 is set by the mirrors N_{14} and N_{17} and it is a factor four higher than the bias current.

6.6.1 Qualitative Analysis

Assuming a basic differential pair described in Figure 6.16(a) with similar input transistors, similar drain resistances ($R_{D1} = R_{D2} = R_D$) and neglecting the load (Z) and source (Y) impedances, it can be shown [105] that the gain of this circuit is written as:

$$(V_{out1} - V_{out2}) = -g_m R_D (V_{in1} - V_{in2}) \ , \tag{6.13}$$

where g_m is the transconductance of the input transistors, R_D the drain resistance, V_{DD} the power supply and V_{out} and V_{in} the output and input voltage of each node. If V_{in1} is much more negative than V_{in2}, $M1$ is turned off while $M2$ is on and the drain current of $M2$ (I_{D2}) is equal to the bias current I_{SS}. Thus, $V_{out1} = V_{DD}$ and $V_{out2} = V_{DD} - R_D I_{SS}$. As V_{in1} increases and becomes closer to V_{in2}, M_1 gradually turns on drawing a fraction of I_{SS} from R_{D1} and lowering V_{out1}. Since the sum of the transistors drain current is $I_{D1} + I_{D2} = I_{SS}$, the drain current of M_2 decreases and V_{out2} rises.

As V_{in1} becomes more positive than V_{in2}, M_1 carries a greater current than does M_2 and V_{out1} drops below V_{out2}. As a consequence, $V_{out1} = V_{DD} - R_D I_{SS}$ and $V_{out2} = V_{DD}$. When both transistors carry the same current ($V_{in1} = V_{in2}$), the output voltages are given by $V_{out1} = V_{out2} = V_{DD} - R_D I_{SS}/2$, as shown in Figure 6.16(b).

On a differential pair, the maximum (V_{DD}) and minimum ($V_{DD} - R_D I_{SS}$) voltage levels are well defined and are independent of the input common-mode level. This is important to suppress the effect of input level variations.

6.6.2 Quantitative Analysis

If load (Z) and source (Y) impedances in Figure 6.16(a) are considered, the differential amplifier transfer function is written as:

$$ft = -\frac{2 g_m R_D (Z + R_D)}{(2 + Y g_m)(Z + R_D)} \ , \tag{6.14}$$

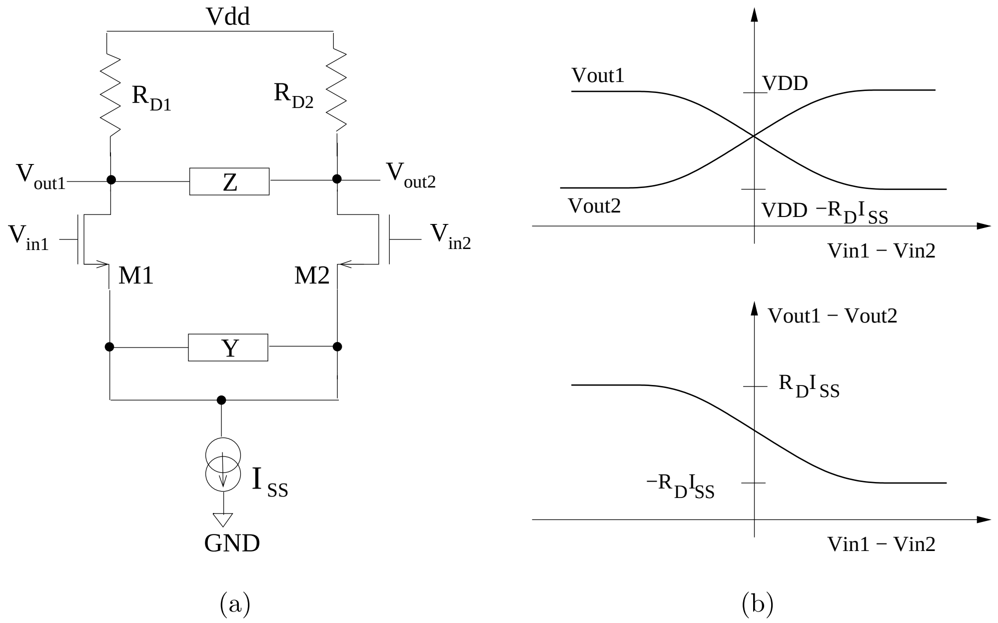


Figure 6.16: (a) Basic differential amplifier. (b) Input-output characteristics of a differential pair.

where

$$Y = \frac{R_1(R_2 + 1/(C_2 s))}{R_1 + R_2 + 1/(C_2 s)} \text{ and } \mathrm{Z} = \mathrm{R}_3 \ . \tag{6.15}$$

In this case the gate capacitances of the subsequent stages and the source/drain capacitances of the input and output transistors are neglected. The values used for positive (negative) polarity amplifier are: R_1 =3.78 Ω, R_2 =2.52(1.26) KΩ, R_3 =7.56 kΩ and C_2 =1.(2.) pF. The differential amplifier transfer function can be simplified and written as:

$$ft = gain * \frac{s + 1/\tau_1}{s + 1/\tau_2} \ , \tag{6.16}$$

where τ_1=6.3 ns (10. ns) and τ_2=3.2 ns (3.9 ns) for the positive (negative) input polarity amplifiers.

Figure 6.17 shows the differential amplifier output at 60 pF input capacitance for positive and negative input polarity with a delta input charge 60 fC.

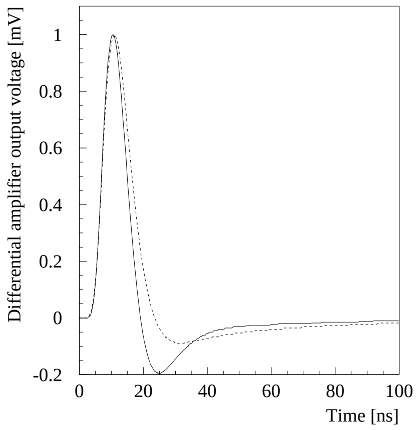


Figure 6.17: Positive (full line) and negative (dashed line) polarity amplifiers, shaper and differential amplifier normalized output voltage, considering a delta input charge of 60 fC and 60 pF input capacitance.

The differential amplifier shows a linear voltage gain of 1.6 (6.3 mV/fC) and 2.0 (7.4 mV/fC) for the positive and negative input polarity, respectively, over the extended signal range. The peak voltage as a function of the input charge is shown in Figure 6.18. Since the gain is determined by the ratio of load to source resistance, it is desensitized to process variations. The input capacitance dependence of the sensitivity and the peaking time are shown in Figure 6.19.

The AC characteristics of the differential amplifier (equivalent frequency spectrum of the pulse at the differential amplifier output) are shown in Figure 6.20. The gain is approximately -32 dB (-28 dB) for the positive (negative) input polarity amplifier, in the range of 6 to 24 MHz with a -3 dB bandwidth of about 145 MHz. The bandwidth of the differential amplifier is limited by the load resistance and the total capacitance of the output node which consists of the parallel capacitance of the output transistor drains, traces and gate input of subsequent stage.

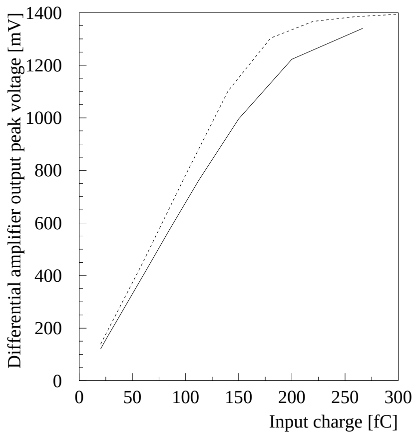
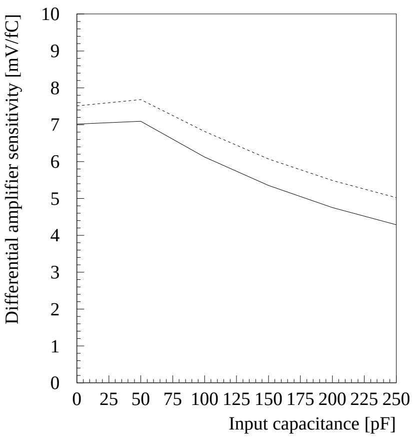
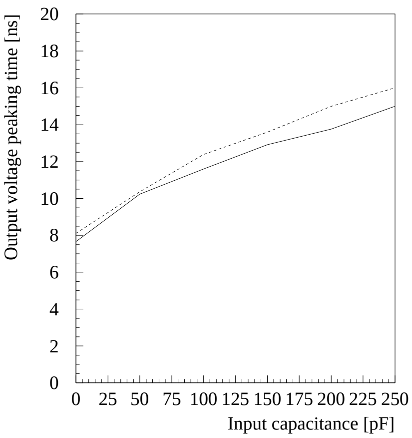


Figure 6.18: Positive (full line) and negative (dashed line) input polarity amplifiers, shaper and differential amplifier linearity at 60 pF input capacitance. The gain is about 6.3 mV/fC and 7.4 mV/fC for the positive and negative input polarity, respectively.

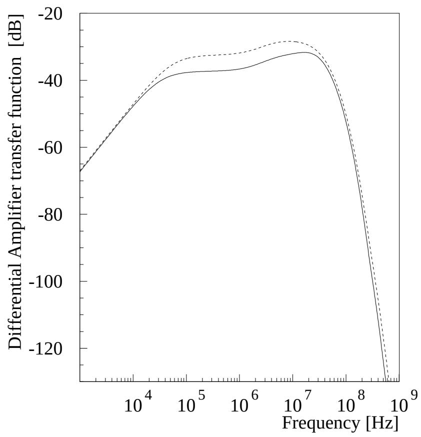


(a)

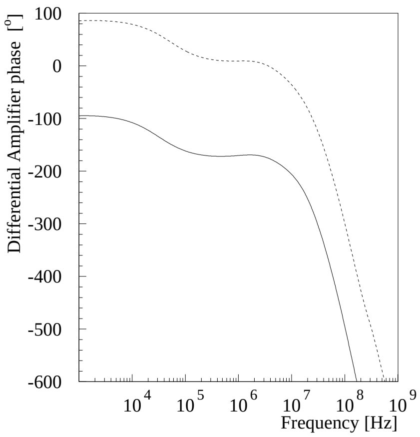


(b)

Figure 6.19: Sensitivity (a) and peaking time (b) of the positive (full line) and negative (dashed line) input polarity amplifiers, shaper and differential amplifier as a function of the input capacitance.



(a)



(b)

Figure 6.20: Positive (full line) and negative (dashed line) input polarity amplifiers, shaper and differential amplifier frequency response Bode plots. The positive and negative polarity shows a gain of -32 dB and -28 dB, respectively, in the range of 6 to 24 MHz with the -3dB point at 145 MHz.

6.7 Baseline Restoration Circuit

An active baseline restoration (BLR) is implemented in the CARIOCA chip. This circuit, shown in Figure 6.21, consists of three amplifiers with the same structure of the one in Figure 6.15. The only difference is that the bias current mirror has a gain 1, what makes the input pair drain current equal to the bias current. The standing current in the first and third amplifiers ($BLR1$ and $BLR3$) is set by a polysilicon resistor R refereed to the power supply, and not by I_{bias}. This current it is not fixed on the second amplifier ($BLR2$) because it has influence in the circuit time constant, as described below.

The BLR input samples the voltage on the differential amplifier output, performs some analog signal processing and feeds back the signal to the input of the differential amplifier, driving the voltage to a common-mode level. To accommo-

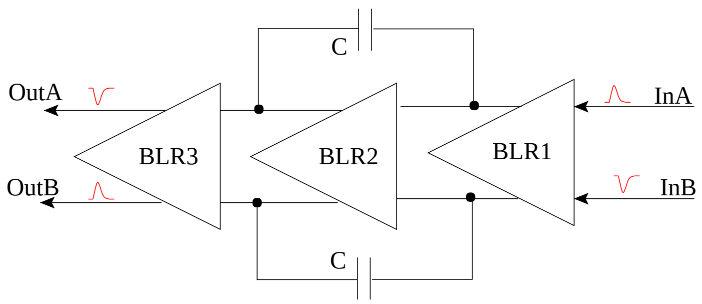


Figure 6.21: Schematic of the baseline restoration circuit.

date high rate operation, the BLR has to drive the differential amplifier output to a common-mode voltage ignoring excursions above the baseline due to large signals. In this way it keeps the signal average near the common-mode voltage, eliminating or reducing baseline shifts.

For linear circuit elements, the BLR is identical to a simple RC coupled stage and it feeds back to the input the same signal from the output, resulting in a bipolar shape. In the present circuit, a bipolar shape can not be used because of the required dead time (50 ns). If the amplifier is non linear, it just feeds part of the signal, making the baseline recover to a common-mode voltage. This non linearity of the circuit is given by the first amplifier ($BLR1$) that has a clipping voltage (V_{clip}) of about 50 mV. The level at which the clipping voltage takes place is controlled by the size and drain current of the amplifier input transistor. This means that if the differential amplifier output signal is higher than V_{clip}, just the amount of signal up to V_{clip} is integrated and feed back into the differential amplifier.

For input signal excursions below the clipping voltage, the circuit looks linear and it works as an integrator. While for large excursions the input transistor of $BLR1$ (gm_1) saturates and it senses only the clipping voltage level, ignoring the large input signals. The open loop gain of the baseline restoration circuit is given by

$$i_3 = -\frac{V_{out} gm_1 gm_3}{sC} \ , \tag{6.17}$$

while the closed loop gain is given by

$$V_{out} = A(i_{in} + i_3)R = ARi_{in}\left(\frac{s}{s + 1/\tau}\right) \ , \tag{6.18}$$

where

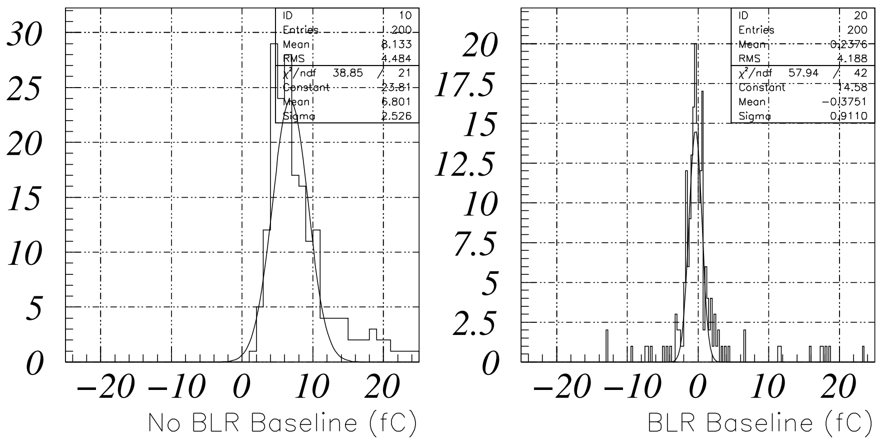
$$\tau = \frac{C}{gm_1 gm_3 AR} \tag{6.19}$$

is the circuit time constant. A is the gain of the differential amplifier equal to 1.6 and 2.0 for the positive and negative polarity circuits, respectively. R is the loading impedance of the shaper, $R4$ in Figure 6.10, equal to 3 kΩ, C is the integrator capacitance (15 pF) and gm_1 and gm_3 are the transconductance of the input transistors of the first and third BLR stage, respectively. By adjusting these parameters it is possible to tune the time constant. As longer is the time constant, smaller is the impact on the shape of the signal and more stable is the circuit.

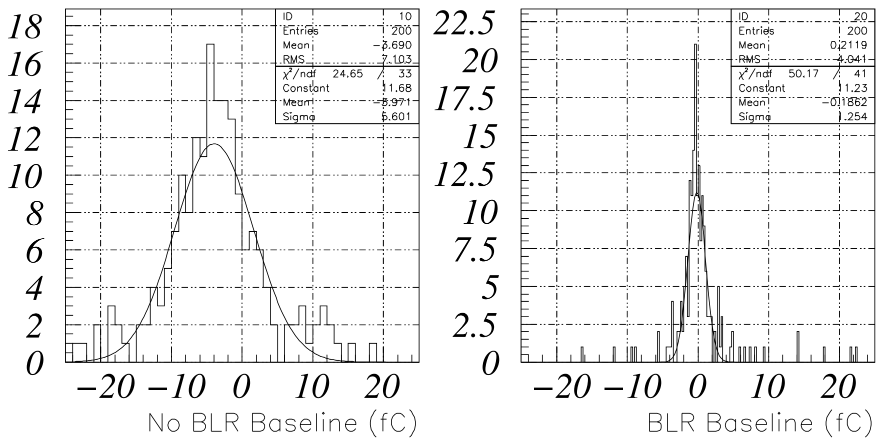
The optimum value for the BLR time constant is about 5 ns and this is obtained from MWPC simulations, as described in [89]. Figure 6.22 shows the simulated cathode and anode baseline shift with and without BLR circuit, for a minimum ionizing particle of 100 fC at 1 MHz rate. If no BLR circuit is considered a baseline shift corresponding to 6.8 fC and -4.0 fC is find for cathode and anode, respectively. Applying a BLR with time constant of 5 μs the baseline shift reduces to 0.2 fC (-0.4 fC) for the cathode (anode).

6.8 Discriminator

The discriminator, whose design is based on an existing circuit [106], is a high-gain differential amplifier with symmetric current-mirror loads. Figure 6.23 shows its schematic. When the voltage on the node InA increases, the drain current of



(a)



(b)

Figure 6.22: Simulated cathode (a) and anode (b) baseline shift with and without BLR circuit, for a minimum ionizing particle of 100 fC at 1 MHz rate.

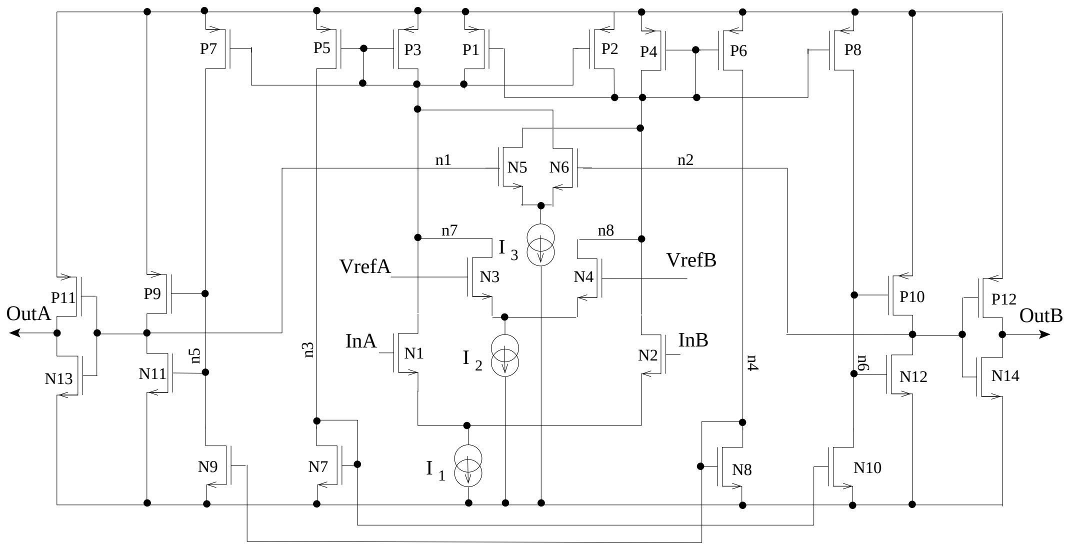


Figure 6.23: Discriminator circuit schematic.

N_1 increases, making the voltage on the node n_1 decreases. That is, the input voltage is reproduced on the drain node of N_1 with a gain given by Equation 6.13.

The threshold voltage is set in a differential way on the nodes $VrefA$ and $VrefB$ and these voltages unbalance the current through the main differential pair. Suppose the voltage on InA becomes more negative, the current flowing on N_1 decreases, and if $VrefA$ is positive the current flowing on N_3 increases. Since the sum of the currents has to be the same, it result in a shift on the DC voltage level of n_1, that in this case becomes more positive.

The current on n_1 and n_2 are mirrored to the next stages and summed on n_5 and n_6. From these nodes there is a very high gain inverter with a positive feedback (hysteresis). The hysteresis is given by a second differential pair $N5/N6$ which unbalances the current on the main differential pair and contributes to increase the gain of the circuit. The amount of hysteresis is programmable by means of a current source (I_3), which shifts the effective discriminator threshold. The bias currents I_1, I_2 and I_3 are supplied from an external input through current mirrors.

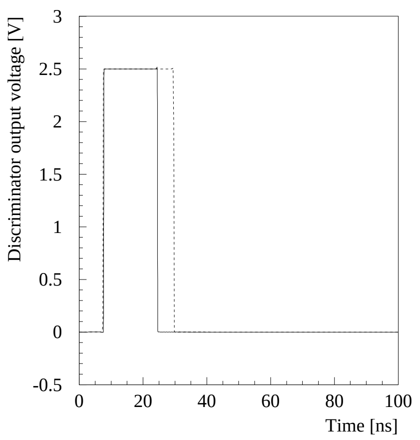
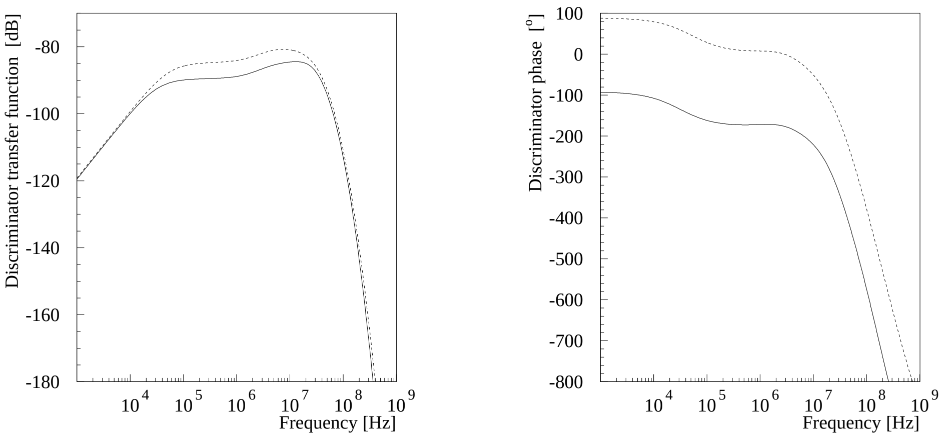


Figure 6.24: Positive (full line) and negative (dashed line) polarity amplifiers, shaper, differential amplifier and discriminator output voltage for a delta input of 60 fC, 60 pF input capacitance and 10 fC threshold.

Figure 6.24 shows the discriminator output voltage for the positive and the negative input polarity circuits with 60 fC input charge and 60 pF input capacitance, considering a threshold of 10 fC. The equivalent frequency spectrum of the pulse on the discriminator output node is shown in Figure 6.25. The gain of -84 dB peaks in the range from 7 to 13 MHz.

The discriminator performance is very important for the chamber time resolution. Measurements, described in Section 7.6.1, have shown that the discriminator circuit adds very little to the intrinsic time resolution due to time walk[2].

[2]Time walk is the effect where different signal amplitudes produces different threshold crossing times, due to finite signal rise time at the discriminator input



(a) (b)

Figure 6.25: Equivalent frequency spectrum of the pulse on the discriminator output node for the positive (full line) and the negative (dashed line) input polarity circuits. The gain of -84 dB peaks in the range from 7 to 13 MHz.

6.9 LVDS Driver Properties

The LVDS driver provides an LVDS-like low-level logic output, with nominal swing of 160 mV centered at 1.2 V with 100 Ω termination resistor, corresponding to the reduced range link described in [107]. This cell consists of a single to differential converter, a main LVDS driver stage and a bias network, shown in Figure 6.26. The detailed schematic is shown in Appendix B. This driver is obtained directly from standard CERN-CMOS cell libraries.

6.10 Input/Output Pad Protection

The pads are divided into analog input/output (I/O), digital and power supply pads. The digital pads are obtained from the LVDS driver and they are protected from normal static discharges due to handling. The power supply pads do not

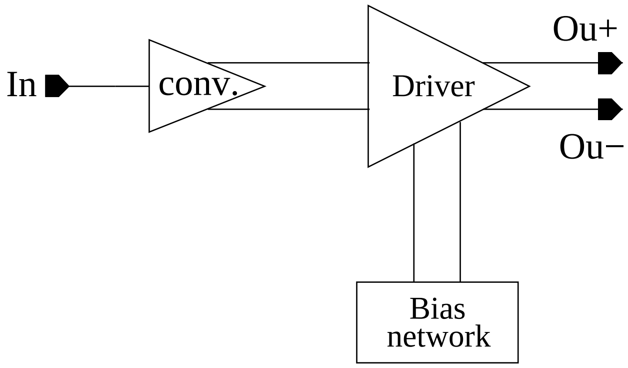


Figure 6.26: Block diagram of the LVDS driver.

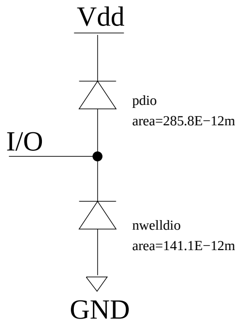


Figure 6.27: Analog input/output pad protection schematic.

handle any protection and a dedicated filter has to be used on the CARIOCA printed circuit board.

The analog I/O pads, shown in Figure 6.27, use a dedicate electrostatic discharge (esd) protection circuit that are more robust without degrading the amplifier performance. This additional protection, alone, is not relied upon to protect the CARIOCA chip from high voltage discharges in the chamber.

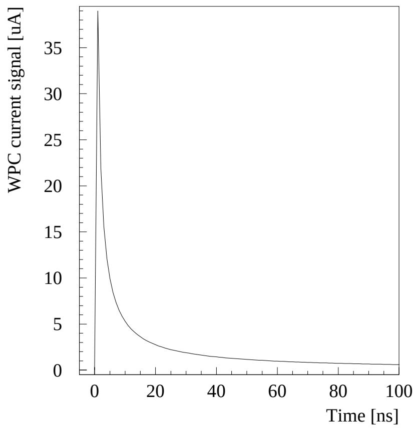


Figure 6.28: MWPC current signal normalized to $39\,\mu$A, corresponding to an input charge of 100 fC at 60 pF input capacitance.

6.11 Simulation with MWPC-like signal

Figure 6.28 shows a MWPC current signal normalized to $39\,\mu$A, corresponding to 100 fC of input charge at 60 pF input capacitance. This signal has a very fast rise time with a $1/(t + t_0)$ tail that well simulates the expected current from the wire pad chamber. The response of the CARIOCA circuit to this input signal is shown in Figure 6.29.

In order to simulate the baseline shift on the chamber a special input signal is created. This input signal contains a 1 MHz random sequence of $1/(t + t_0)$ pulse 20 us long, with a Landau pulse height distribution. Figure 6.30 shows the circuit response for this input signal. One can see that the baseline has a large shift at the amplifier output, but it well recover to zero at the discriminator input.

6.12 Inverted Polarity Behaviour

The simulated response of the CARIOCA chip to an input signal of the type MWPC-like with inverted polarity is shown in Figure 6.31. Although the negative

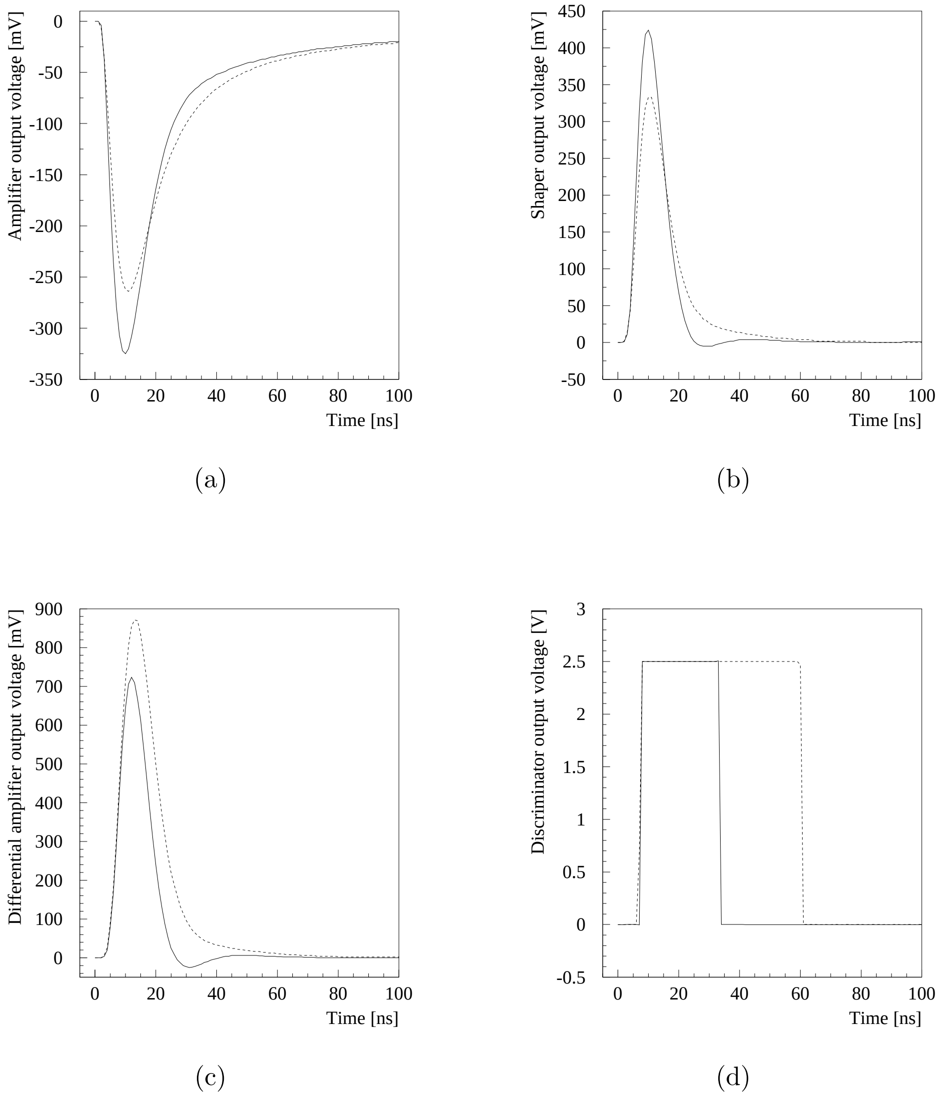
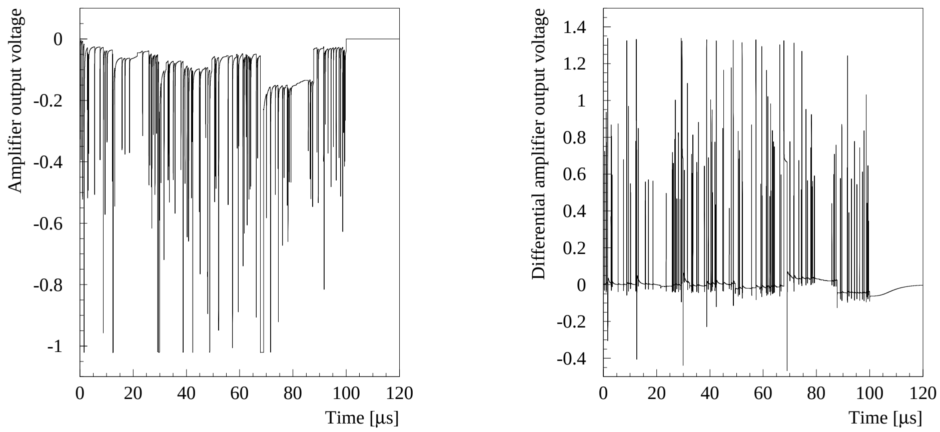


Figure 6.29: CARIOCA chip response to a $1/(t + t_0)$ input signal normalized to an input charge of 100 fC at 60 pF input capacitance. (a) Amplifier, (b) shaper, (c) differential amplifier and (d) discriminator output for a threshold of 10 fC. The full line shows the response of the positive input polarity chip, while the dashed line shows the response of the negative one.



(a) (b)

Figure 6.30: CARIOCA positive input polarity analog signal chain simulation after the amplifier (a) and before the discriminator (b), for a $1/(t + t_0)$ input signal at 1 MHz rate. Both waveforms are normalized to about 1.

input polarity circuit is more sensitive to a positive input signal than the positive circuit is for a negative input, it recovers faster than the positive circuit to the noise level. The discriminator is not fired for both amplifiers, if a threshold of 10 fC is adopted.

6.13 Saturation Behaviour

The saturation behaviour is an important characteristic in a circuit. When a front-end saturates it takes a certain time to recover to the standard state and this time is considered as a dead time, since no data can be taken during this period. Although the MWPC has an average collected charge at about 50 fC, some times it can happen that there is a very high signal in the chamber coming from background.

These very energetic particles can saturate the front-end electronics, resulting

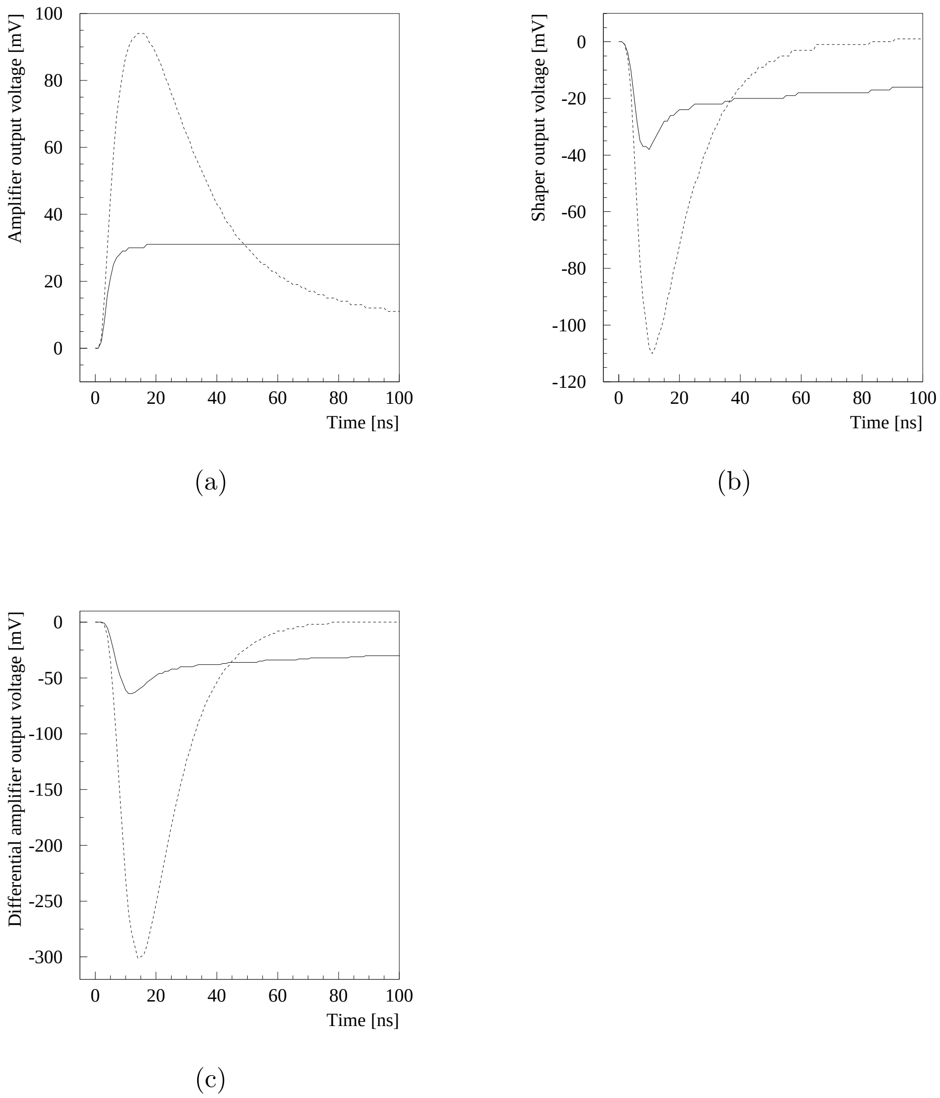


Figure 6.31: Simulated response of the CARIOCA chip to a $1/(t + t_0)$ input signal with inverted polarity, normalized to 50 fC of input charge. (a) Amplifier, (b) shaper and (c) differential amplifier output . The full line shows the response of the positive input polarity chip, while the dashed line shows the response of the negative one.

in a dead time or, in the worst case, a collapse of the amplifier. To simulate these effects on the CARIOCA front-end, an input signal composed by a delta pulse with very high amplitude followed by another delta pulse with small amplitude is used. The simulated dead time of the positive (negative) input polarity chip is about 200 ns (100 ns) for an input charge of 1 pC, increasing to 2.6 μs (330 ns) for a 500 pC charge.

If the induced charge has inverted polarity, i.e., if the induced charge on the anode (cathode) has positive (negative) polarity, the recovering time is of the order of 1.3 μs (positive) and 300 ns (negative) for an equivalent input of 1 pC.

6.14 Monte Carlo Simulation

Transistor length, width and threshold voltage are important parameters for the good behaviour of the circuit. These parameters can vary in the fabrication process, as discussed in the Appendix A. In order to verify how robust the CARIOCA circuit design is against process variations, a Monte Carlo simulation is used. The Monte Carlo simulation varies the transistor matching characteristics, changing the voltages on the internal nodes of the circuit. For this study, 100 Monte Carlo events using HSPICE simulator are generated with a random distributions of the design parameters, considering the process variations, and no significant DC fluctuation is observed in the circuit. The most sensible parts of the circuit are the discriminator input nodes. On these nodes, the simulation showed a differential voltage offset of about 3.5 mV rms, what is 20 times smaller than the nominal MWPC threshold value of 70 mV differential (Section 5.8), corresponding to about 10 fC.

6.15 Circuit Layout

The layout of an integrated circuit defines the geometries that appear on the masks used in the chip fabrication. Most of the dimensions in a layout are dictated by design rules. Except the width and length of the transistors that are determined by circuit design. The design rules are a set of rules that guaranties proper transistor and interconnect fabrication. They strictly dependent on the used technology. Details on the fabrication process and the layout techniques are described in the Appendix A.

CARIOCA circuit layout uses radiation tolerant techniques. Each sub-circuit is laid out independently forming a single block and making easier the coupling of sub-circuits. In order to test the CARIOCA sub-circuits, several prototypes were produced. Prototypes design and production are discussed in the next chapter.

Chapter 7

CARIOCA Prototypes

7.1 Introduction

In order to evaluate the CARIOCA circuit with a step by step approach, seven prototypes were produced in a 0.25 μm CMOS technology during the years 2000 and 2001. The layout of the prototypes is done with enclosed transistor structure and guard-rings [108], known to be tolerant to ionizing radiation effects. Because of the additional parasitics and the layout constrains, the same circuit with standard layout would exhibit better speed and noise performance. This development is done in the framework of the CERN RD49 project [14].

In this chapter I present the design and test of the CARIOCA prototypes. Most results presented here were already presented in international conferences and workshops and are published in [109], [110], [102], [111] and [112].

7.2 Prototype I - Positive Polarity Amplifier

The first CARIOCA prototype was produced in April of 2000 with the aim of testing the current-mode amplifier concept. The prototype is a eight-channel low noise amplifier for positive readout, three-stage discriminator and LVDS driver,

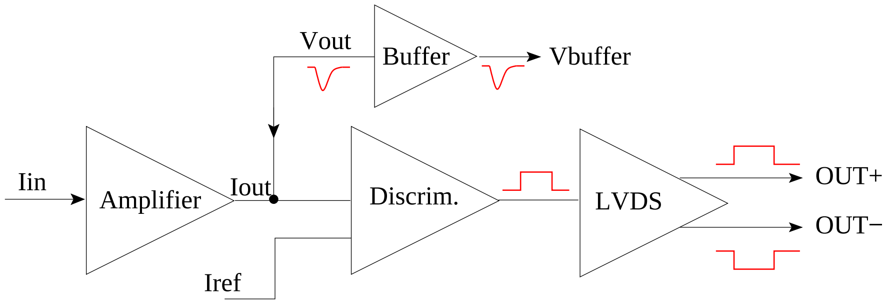


Figure 7.1: Block diagram of a single channel of the CARIOCA prototype I.

operating at 2.5 volts. The overall chain is DC, allowing very high counting rate readout operation without baseline shift effects. The analog structure of a single channel is shown in Figure 7.1. Each channel is a single ended input and differential output front-end, with independent biasing and threshold circuit, which may avoid crosstalk between channels. This front-end is optimized for detector capacitances up to 120 pF.

The amplifier, described in Section 6.4, is designed in two versions: one for the readout of MWPC of the LHCb Muon System and the other for silicon strip detectors. The main difference between these two versions is the current gain at the output of the amplifier. For the MWPC a gain 6 is used and for the silicon detector a current gain of 64, due to the smaller detector signal. Its schematic is shown in Figure 6.2(a). This thesis presents only the requirements and results for the low gain CARIOCA amplifier developed for the LHCb muon chambers, which is more challenging in terms of detector capacitance. The output current of the amplifier is sent to the current discriminator and, in parallel, is converted into voltage by an internal buffer. The buffer, shown in Figure 7.2, is used to drive the amplifier output voltage to the chip pad without increasing considerably the capacitance on the discriminator node.

The discriminator, shown in Figure 7.3, consists of three stages: a current discriminator, a voltage sensing amplifier and a buffer followed by a LVDS driver.

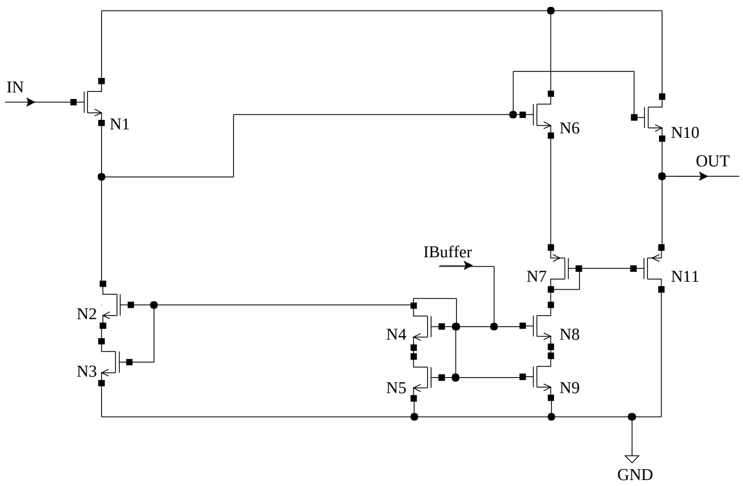


Figure 7.2: Buffer to drive the output voltage from the amplifier to the chip pad.

The current discriminator is based on a current to voltage converter that feeds a voltage comparator. In order to achieve both high speed and sensitivity the current to voltage converter is a p-channel transistor in common gate configuration. The amplifier output current is sensed by the common gate branch and when this current is greater than the unbalanced drain current between $P1$ and $P2$, the current on $P1$ branch is turned off and the unbalanced voltage on this node is sensed by the transistors $N6$ and $N7$. The unbalanced current is the threshold current, that is fixed by the width of the transistors $P1$ and $P2$ and their bias current (I_{bias}) as follows:

$$I_{th} = \frac{W_{P2} - W_{P1}}{W_{P2}} I_{bias} \ . \tag{7.1}$$

In order to cancel the amplifier offset, a compensation circuit which forces a positive offset is added to the discriminator with an additional bias source (I_4) and a low pass filtering capacitor ($C1$). The current discriminator is a low power discriminator with the advantage of a differential output with a good common mode rejection. The output of the differential amplifier is sensed by a buffer and sent to the LVDS driver, described in Section 6.9.

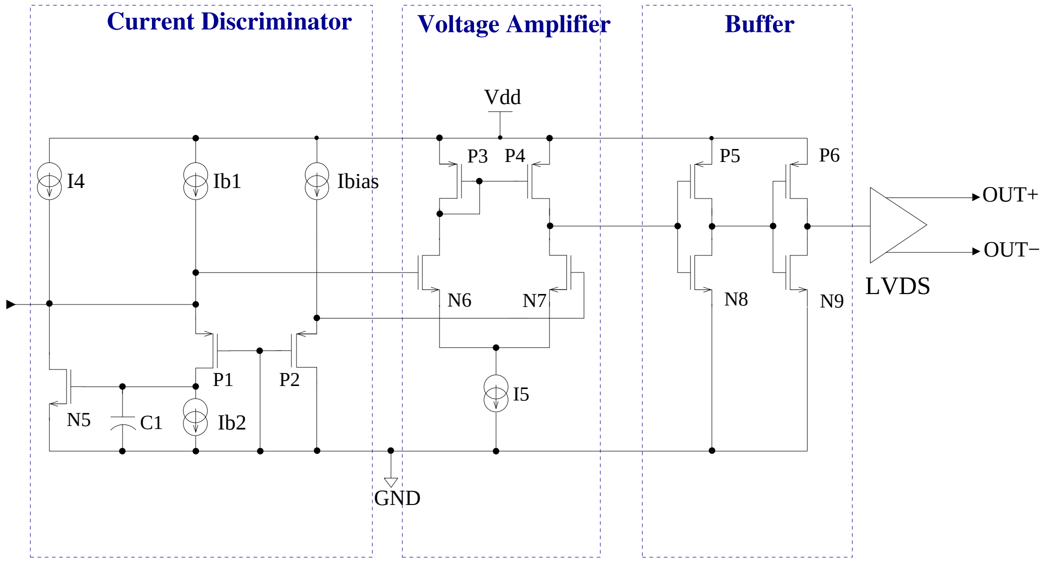


Figure 7.3: Three stage discriminator: a current discriminator, a voltage amplifier and a buffer followed by an LVDS driver

7.2.1 Chip Layout

The first CARIOCA prototype has four channels with low gain (current gain equal to 6) and four with high gain (current gain of 64) amplifiers, fabricated in a $2{\times}2\,\mathrm{mm}^2$ die. The eight amplifier inputs are located at the left side and the sixteen digital outputs on the right side. Each channel has independent bias and threshold lines that are connected to top and bottom pads. Amplifier analog output, from the buffer, is read only for two channels. Power lines are provided independently to the amplifier and the discriminator, avoiding coupling between digital and analog signals through the power supply. The power lines are connected to a pad on the top and on the bottom of the chip to reduce the voltage drop across the chip. Between each channel there is a thick line of $8\,\mu$m width composed of all metal layers and connected to ground. This line works as a barrier and is used to minimize the crosstalk between channels.

The chip has a total of 54 pads and it is packaged in a 72-pin package, with

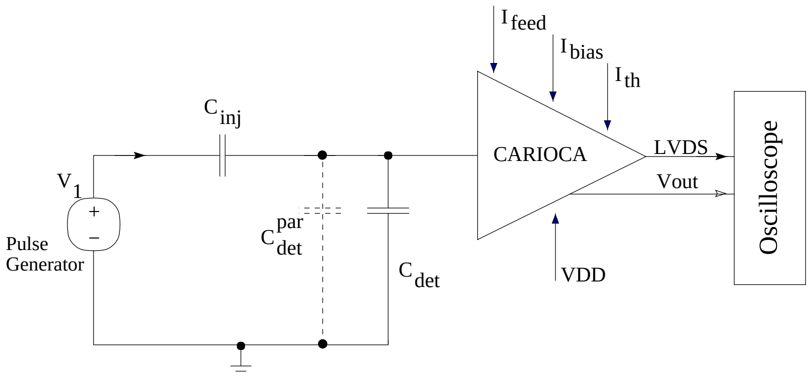


Figure 7.4: Experimental setup to test the CARIOCA prototype I.

10 mm of internal cavity. This results in, at least, a 4 mm bonding wires, which have a self inductance that may disturb the circuit speed and crosstalk evaluation.

7.2.2 Measurement Results

The CARIOCA positive polarity amplifier prototype successfully operates with 2.5 V power supply. The test setup consists of a pulse generator, a board housing the chip, a power supply and a digital scope. A voltage step signal (V_1) of 5 ns rise-time applied to a 1.8 pF injection capacitor (C_{inj}) in series with the amplifier input is used as input signal, as shown in Figure 7.4. This long signal rise time shifts the peak position with respect to a delta pulse, reducing the amplifier speed and sensitivity. A parallel capacitance is used to simulate the detector pad capacitance (C_{det}^{par}). The printed circuit board together with the chip package has a parasitic capacitance (C_{par}) to ground that is measured and find to be equal to 17 pF. This parasitic capacitance is added to the input capacitance value in the experimental results. The bias currents are supplied by external resistors located on the printed circuit board. Figure 7.5 shows analog and digital signals for a 72 fC input charge at 17 pF capacitance. The analog signal is measured from the buffer connected to the amplifier and the digital one from the LVDS driver.

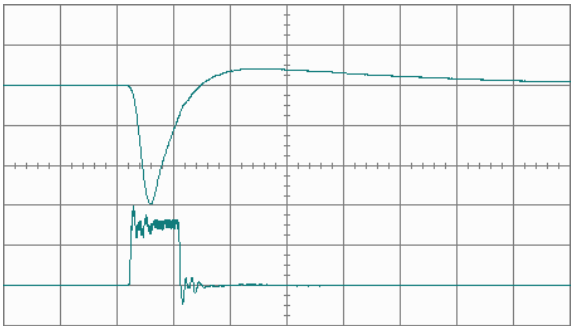
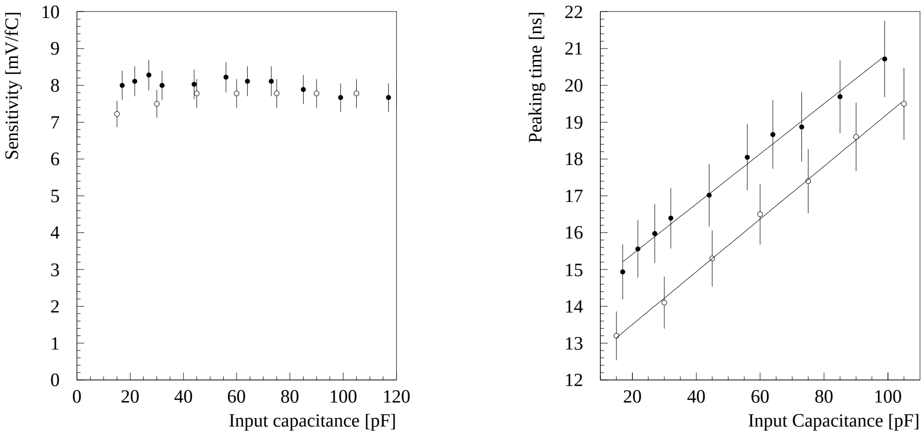


Figure 7.5: CARIOCA prototype I analog and digital output signals for an input charge of 72 fC and 17 pF of input capacitance. The horizontal scale is divided in steps of 50 ns and the vertical scale in steps of 200 mV.

The sensitivity, shown in Figure 7.6(a), is measured for detector capacitances up to 120 pF and it shows good uniformity within 5 %. The gain on the node between the amplifier and the discriminator is about 8 mV/fC. Due to the chip design, this gain depends on the discriminator threshold and the measurements have to be done with a higher threshold current. Therefore, the discriminator can not be used by the MWPC and it has to be replaced.

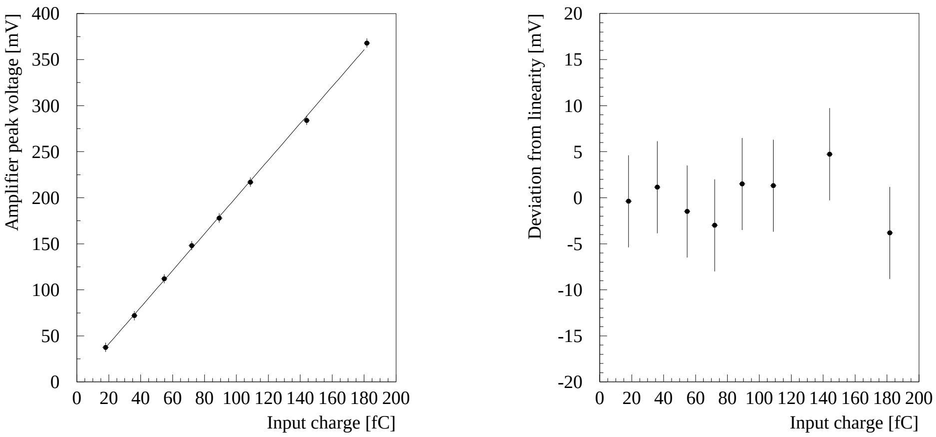
Figure 7.6(b) shows the measured and simulated peaking time versus detector capacitance. The measurement shows a peaking time of 14 ns at zero input capacitance and a weak dependence on the detector capacitance. The discrepancy between measurement and simulation is probably due to additional parasitics and layout constrains, not considered in the simulation. The simulated peaking time for the amplifier alone is about 7 ns. The deterioration of the amplifier speed is due to the increase of capacitance in the coupling with the discriminator stage.

The circuit shows a good linearity up to 250 fC input charge for an input capacitance of 17 pF. Figure 7.7 shows the linearity and the deviation from the linear fit. Both sensitivity and linearity are measured with an external operational amplifier, used to drive the output voltage from the amplifier pad to the oscilloscope input and to provide impedance matching for 50 Ω cable load.



(a) (b)

Figure 7.6: (a) Amplifier sensitivity and (b) peaking time as a function of the detector capacitance for measurements (black circles) and simulation (white circles).



(a) (b)

Figure 7.7: Amplifier output peak voltage (a) and deviation from linear fit (b) as function of the input charge after an amplifier attenuator.

The noise behavior of current mirror has been previously investigated [113]. For the study of the CARIOCA prototype I, a brief calculation is done, considering a weighting function with a bipolar shape, as described in [114]. Parallel, serial and flicker noise are found to be:

$$ENC_P^2 = I_n^2 t_{peak} \ , \quad I_n^2 = 4kT/R_P \tag{7.2}$$
$$ENC_S^2 = \frac{V_n^2 C_{in}^2}{T_{peak}} \ , \quad V_n^2 = 4kTn\gamma/g_m \tag{7.3}$$
$$ENC_{1/f}^2 = A_f C_{in}^2 \ , \tag{7.4}$$

where k is the Boltzmann constant, T the absolute temperature, t_{peak} the signal peaking time, C_{in} the input capacitance and g_m the input transistor transconductance. The noise characteristics of 0.25 μm CMOS technology, discussed in [115], are estimated to be $n = 1.4$, $\gamma = 0.6$ and $A_f = 4.10^{-14}\,\mathrm{V}^2/\mathrm{Hz}$. The equivalent input noise current (I_n^2) is modeled as a noise resistance of 50 Ω in parallel to the input. This calculation gives a parallel noise of 416 e^- with a noise slope of about 36 e^-/pF and an equivalent input noise voltage of 0.7 nV/$\sqrt{\mathrm{Hz}}$.

The noise measurements are performed with a drain current of 2 mA at the input transistor, resulting in a g_m of 30 mΩ^{-1}. The noise is measured by taking the rms of the noise from the digital oscilloscope and dividing the result by the amplifier sensitivity. The results are shown in Figure 7.8 together with the calculations. The measured equivalent noise charge is 1200 e^- with a slope of 45.7 e^-/pF. Noise measurements indicate an excellent performance of the current-mode feedback and agree with noise calculations based on the models for 0.25 μm CMOS technology, considering that the calculation is done only on the amplifier but the measurements are performed on the hole chip and part of the noise originates from the rest of the circuit.

The total power consumption is measured to be 12 mW per channel for a supply voltage of 2.5 V, including bias circuits, discriminator and LVDS driver.

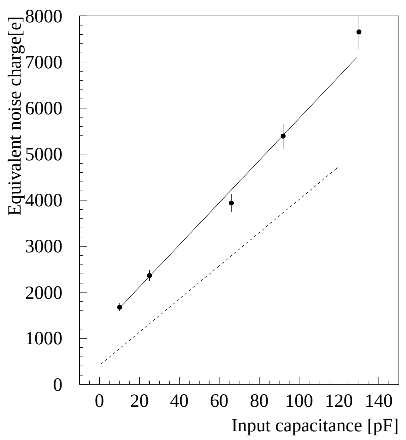


Figure 7.8: Measured equivalent noise charge of prototype I. The dashed line shows the calculation results.

7.3 Prototype II - Fourteen Channels of Positive Polarity Amplifier

The second CARIOCA prototype is a fourteen-channel amplifier, discriminator and LVDS driver implemented in a $2{\times}4\,\mathrm{mm}^2$ die, with a total of 82 pads. This prototype uses the same circuits described in the previous section and it was produced in September of 2000 to study channel-to-channel uniformity and crosstalk. Figure 7.9 shows the analog structure of one channel. Since the aim is to study the uniformity between channels, all channels are identical (with the same gain) and do not have analog output. The bias and threshold currents are provided, by resistors in the PCB, at the same time to seven channels. The chip layout is similar to the first prototype, changing only the die size.

7.3.1 Chip Characterization

A voltage step signal of 2 ns rise time through an injection capacitor of 1.8 pF is used as input signal. This chip is not packaged and is directly bonded on the test

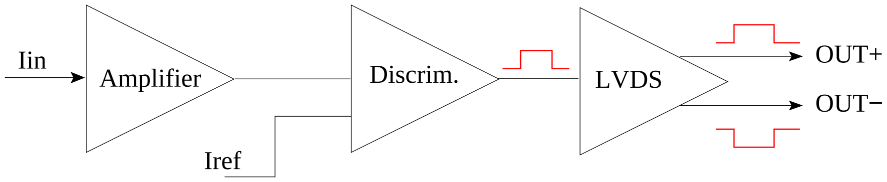


Figure 7.9: Block diagram of the CARIOCA of prototype II channel.

board, to minimize parasitics. Although it is not packaged the board parasitic capacitance to ground is measured to be equal to 10 pF. The LVDS output is read directly by the scope via a high impedance probe. The measurements are taken in an automatic way via a oscilloscope connected to a computer, through a General Purpose Interface Bus[1] (GPIB), running Labview program [116]. The results are compared to the HSPICE simulation of the circuits.

The discriminator effective threshold and noise are measured with the so called S-curve method. This method consists of measuring the probability of threshold crossing as a function of the input charge. In order to measure this probability, 60 samples with 6 input signals at the same charge are sent to the chip and the number of threshold crosses is counted, for a fixed threshold current. This procedure is repeated for at least fifteen different input charges and a probability curve is drawn. Assuming the front-end noise is described by a Gaussian distribution, the probability curve can be fitted with an integral of a Gaussian. In this case, the mean value corresponds to the effective threshold and the sigma to the rms noise. Figure 7.10 shows the probability measurement, for 72 pF input capacitance and a threshold current of 0.7 μA. The measured effective threshold is about 13.4 fC and the noise 0.45 fC ($\sim$2806 e^-). Figure 7.11 shows the correlation between the measured effective threshold and the threshold current, for an input capacitance of 72 pF.

[1]GPIB is a digital 8-bit parallel communication interface, with data transfer rates up to 1 Mbyte/s, specially designed for connecting computers and instruments (standard IEEE 488.1).

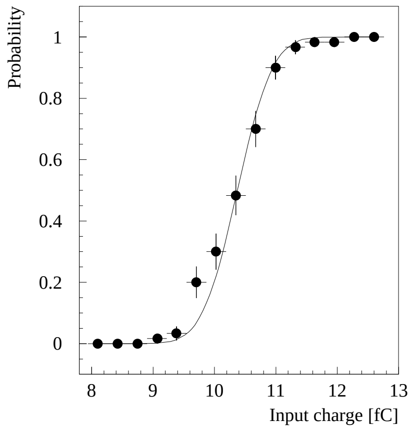


Figure 7.10: Probability of threshold crossing as a function of input charge for 72 pF of input capacitance at a threshold current of $0.7\,\mu$A. The line is the fit with the function integral of a Gaussian distribution.

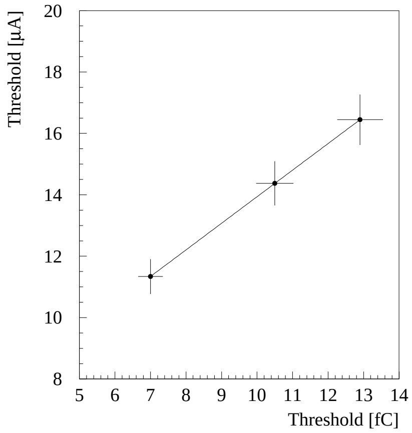


Figure 7.11: Measured effective threshold as a function of the threshold current, for an input capacitance of 72 pF.

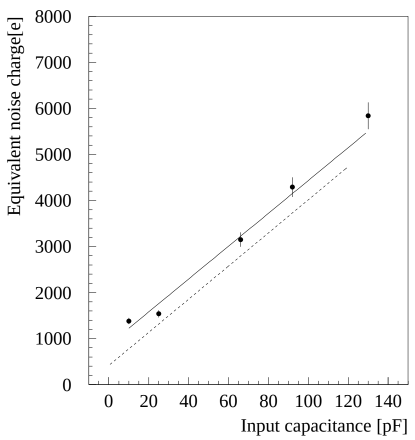


Figure 7.12: CARIOCA prototype II measured equivalent noise charge as a function of the detector capacitance. The dashed line shows the obtained values from the calculation.

The noise behaviour of the CARIOCA prototype II is performed using S-curve measurements for various input capacitance. The result is shown in Figure 7.12 together with the calculation, described in the previous section. The noise is smaller than the noise measured for prototype I because there is one less source of noise; the analog buffer is not present on prototype II. Overall agreement of the noise picture is observed, taking into account that the calculation is done only for the amplifier.

The channel-to-channel uniformity is studied for threshold and equivalent noise charge measurements. This study is done in a total of fourteen channels at a threshold current of 0.7 μA and an input capacitance of 72 pF. The effective threshold shows a rms spread of 0.64 fC for a mean value of 11.03fC. For the noise the rms is 258 e^- for a 3446 e^- mean value. The uniformity is within 6 % and 7 % for both measurements.

Figure 7.13 shows the measured and simulated discriminator time walk for a threshold current of 0.7 μA and a 10 pF input capacitance. The time walk is

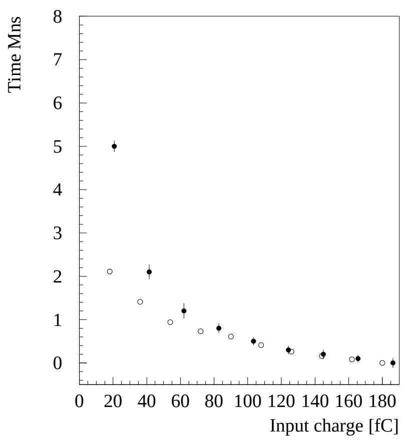


Figure 7.13: Time walk as a function of the input charge. The black circles shows the measurements and the white circles the simulation.

an intrinsic quantity of the circuit, defined as the difference of threshold crossing time produced by different signal amplitudes. The measured time walk is of the order of 2 ns for an input charge range from 40 fC to 180 fC, showing an excellent behaviour of the discriminator.

To measure the crosstalk a signal is injected in one channel and the threshold on the neighbor channels are changed until a charge is measured on their outputs. The ratio between the measured charge in the neighbor channel and the injected charge is defined as crosstalk. Figure 7.14 shows the measured crosstalk for a charge injected in channel 5. This crosstalk is a total crosstalk, including the chip and PCB crosstalk, and it stays below 2 %. This is a good results, considering that no PCB optimization is done.

A total power consumption of 18 mW per channel is measured on this chip. The main contribution came from the LVDS driver that consumes 14 mW per channel.

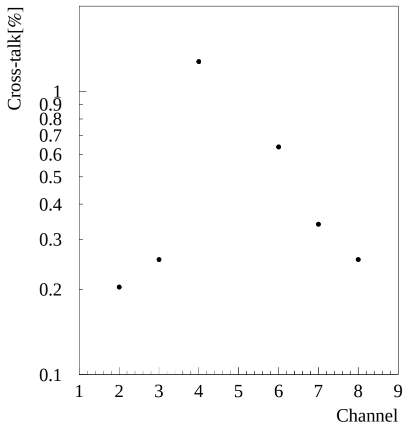


Figure 7.14: Total measured crosstalk for an input charge on channel 5.

7.3.2 Measurements with the Wire Chamber

This CARIOCA chip has been tested on a MWPC prototype described in [117]. The MWPC prototype is a double gap chamber with sensitive area of 16x24 cm^2 and symmetric gas gap equal to 2.5 mm. The chamber is filled with the pre-mixed gas mixture Ar(40%)/CO_2(50%)/CF_4(10%). The anode wires of 30 μm of diameter are grouped in 8 wire pads (W1-W8) of 2x16 cm^2 and 4x16 cm^2, corresponding to a capacitance of 60 pF and 100 pF, respectively. The chamber has also 16 cathode pads (C1A-C8A and C1B-C8B) of sizes 2x8 cm^2 (40 pF) and 4x8 cm^2 (60 pF). The chamber active area is shown on Figure 7.15. The test beam setup is described in detail in [117].

The detection efficiency measured in a 20 ns time window, at 0.7 μA threshold current (corresponding to 11 fC), is shown in Figure 7.16(a) for both 40 pF and 60 pF cathode pads. Figure 7.16(b) shows the chamber time resolution. The measured time resolution is found to be 4.3 ns at the MWPC operating point (3.15 kV), with a threshold of 11 fC. This result can be improved if the threshold is reduced.

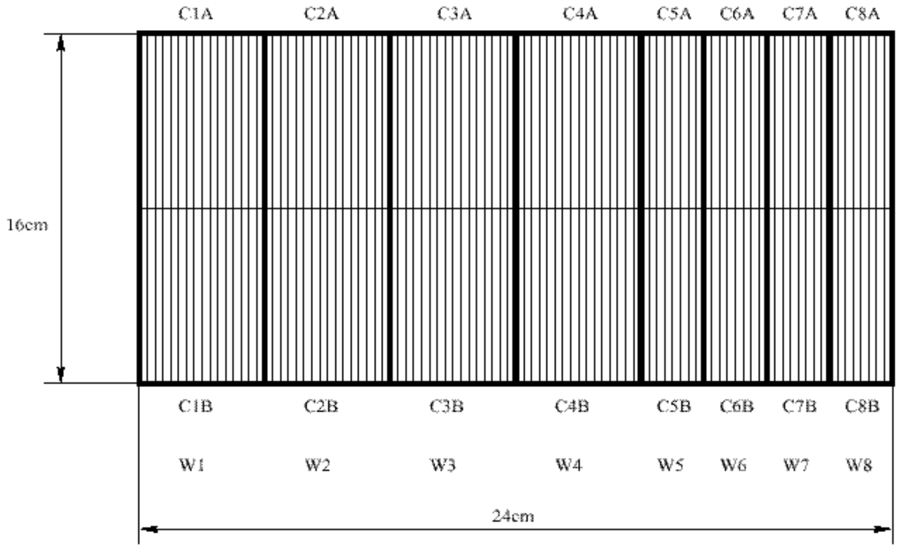


Figure 7.15: Anode and cathode pad structure of the MWPC prototype.

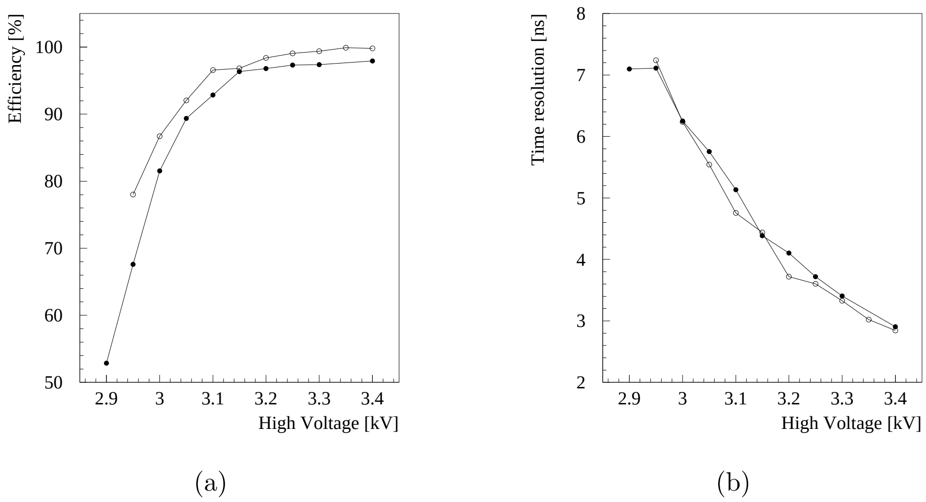


Figure 7.16: Detection efficiency (a) and time resolution (b) of a double-gap MWPC for $2 \times 8\,\mathrm{cm}^2$ (white circles) and $4 \times 8\,\mathrm{cm}^2$ (black circles) pads, at a threshold current of $0.7\,\mu$A (corresponding to 11 fC).

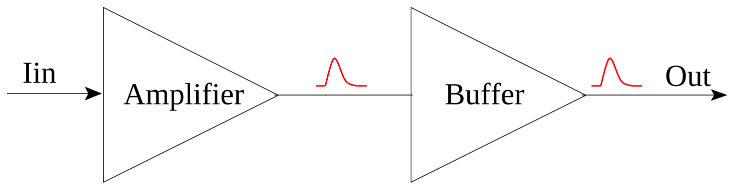


Figure 7.17: Analog structure of the CARIOCA prototype III channel.

7.4 Prototype III - Negative Polarity Amplifier

The third CARIOCA prototype is a eight-channel chip with amplifier for negative input polarities and analog buffer. This prototype was produced in February of 2001 with the aim of testing the negative input polarity amplifier. The chip is a $2{\times}2\,\mathrm{mm}^2$ die with 48 pads. Each channel is composed by a negative input polarity amplifier, described in Section 6.4, and an analog buffer shown in Figure 7.2. Since this was the first design of the negative input polarity amplifier, the additional transistors $N7$ and $N8$, shown on Figure 6.2, were not yet present in the circuit design and layout. Figure 7.17 shows the analog structure of one channel. The amplifier output current is converted into voltage via a diode connected transistor (not shown) and the voltage is driven to the chip pad by the analog buffer. The channels have independent bias currents and the layout is similar to the prototype I layout, without the discriminator. The inputs are located on left side pads, the analog output on right side pads and the bias and power supply lines on top and bottom pads.

7.4.1 Experimental Setup

A special PCB is made to test this prototype, where the chip is soldered directly on the board. The chip output is sent to a commercial wide-bandwidth operational amplifier, located on the test board, that provides the signal to the oscilloscope. Bias currents are provided independently to each channel by resis-

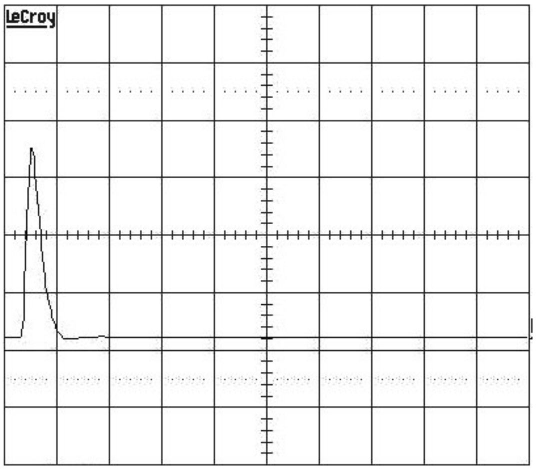


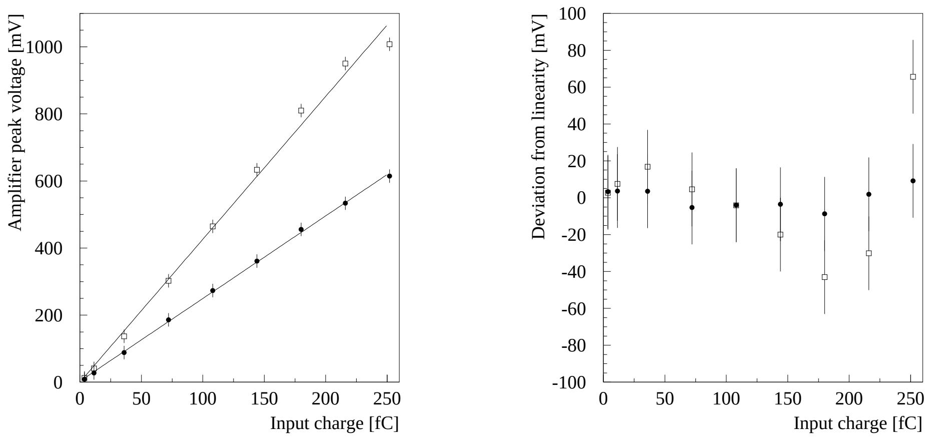
Figure 7.18: Output pulse shape (average of 1000 pulses) of the CARIOCA prototype III for a delta input signal of 34 fC at 68 pF. The horizontal scale is 50 ns per division and the vertical scale is 20 mV per division.

tors in the test board. The parasitic capacitance on the board is found to be 10 pF. The experimental setup is the same used to test prototype II.

A voltage step function of 800 ps rise time sent through a series capacitance of 4.5 pF, with a 51 Ω termination resistor, is used as input signal. Figure 7.18 shows the output pulse shape of the chip for a delta input signal of charge 34 fC and input capacitance of 68 pF.

7.4.2 Results

The amplifier output voltage and peaking time are measured through the oscilloscope curve display. Figure 7.19 shows the output voltage as a function of the input charge for two different input capacitances: 27 pF and 220 pF. A 10 % non linearity is observed at 250 fC input charge for a 27 pF input capacitance. This small non linearity is due to a saturation on the diode connected transistor used to convert the amplifier output current into voltage. The sensitivity is 4.3 mV/fC and 2.5 mV/fC, for 27 pF and 220 pF input capacitance, respectively. It depends



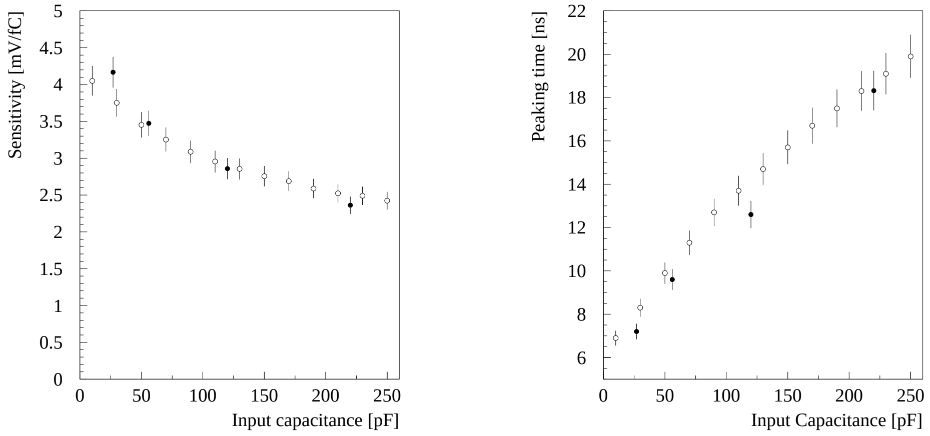
(a) (b)

Figure 7.19: (a) Amplifier output peak voltage and (b) deviation from linearity as function of the input charge for 27 pF (white circles) and 220 pF (black squares) input capacitance. The fit shows a gain of 4.3 mV and 2.5 mV for 27 pF and 220 pF input capacitance, respectively.

on the input capacitance, as shown in Figure 7.20(a) for an input charge of 36 fC, decreasing by 40 % for input capacitances in the range from 10 to 250 pF.

Figure 7.20(b) shows the measured and simulated amplifier peaking time as a function of the input capacitance. The peaking time varies from 7 to 20 ns in the input capacitance range from 10 pF to 250 pF. The measured equivalent noise charge, shown in Figure 7.21, results in a noise of 975 e^- with a slope of 48 e^-/pF. The calculation is not yet done for this chip, but the measurement shows a good behaviour of the circuit.

The crosstalk is 0.8 % for the neighbour channel and smaller than 0.1 % for the next channels, showing an excellent performance of the circuit design. The channel-to-channel uniformity is measured for a delta input signal of 34 fC at 68 pF input capacitance. The results show a 3.5 % non uniformity for the sensitivity and about 5 % for the peaking time, what is within the measurement



(a) (b)

Figure 7.20: (a) Amplifier sensitivity and (b) peaking time dependence on the input capacitance for 36 fC input charge. The black circles show the measurement and the white circles the simulation.

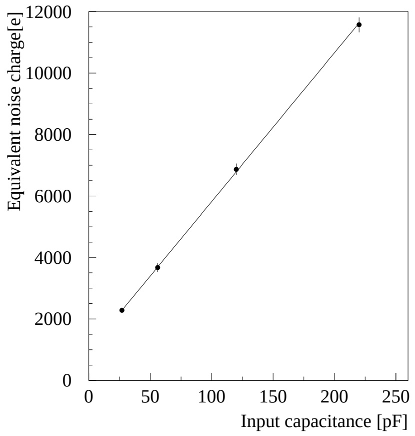


Figure 7.21: Measured equivalent noise charge for the negative polarity amplifier.

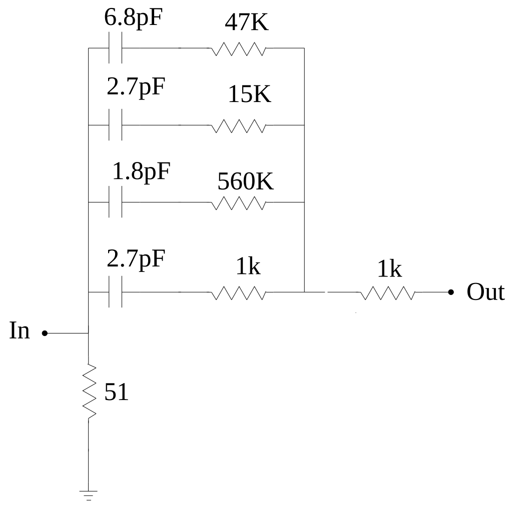


Figure 7.22: Schematic of the 1/t signal injector.

uncertainty.

In order to simulate the signal from the MWPC anode pad a 1/t signal injector, shown in Figure 7.22, is used. This injector is calibrated in charge with respect to a delta input signal, assuming that equal input charges give output signals of equal amplitude. Figure 7.23 shows the output signal for a 1/t input signal of 34 fC at 68 pF input capacitance. Since this chip has no shaper, the 1/t injector gives rise to a long output signal with a DC component.

7.5 Prototype IV - Positive Polarity Amplifier and Shaper

This CARIOCA prototype is a four-channel chip, fully differential. Each channel consists of two positive input polarity amplifiers and a differential shaper, followed by two analog drivers. The channel analog structure is shown in Figure 7.24. One amplifier is used to readout the input signal from the MWPC and the other has floating input, to provide correct DC balance to the shaper. In this way it improves the common mode rejection to pickup, crosstalk and noise on the

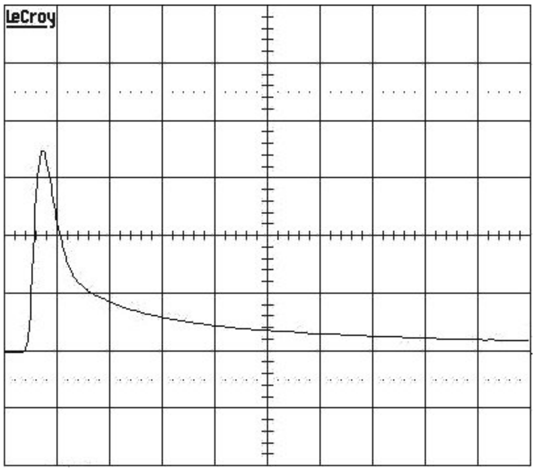


Figure 7.23: Output pulse shape (average of 1000 pulses) of the CARIOCA prototype III for a 1/t input signal with 34 fC and 68 pF input capacitance. The horizontal scale is 50 ns per division and the vertical scale is 20 mV per division.

power supply lines. Both amplifiers have the structure shown in Figure 6.2 and they are already tested with the previous prototypes. The shaper, shown in Figure 6.10, is a fast differential amplifier with common-mode feedback. The tail cancellation in performed by a double pole/zero compensation network, displayed in Equation 6.12. The analog driver, already shown in Figure 7.2, is used to drive the shaper output to the chip pad.

The chip was produced in April of 2001 in a $2{\times}2\,\mathrm{mm}^2$ die, with 46 pads. The amplifier bias currents are provided to each pair of amplifiers at the same time. Each shaper has independent bias current. The power supply is laid out independently for the amplifiers and the shapers. The chip layout structure is similar to the previous prototypes.

7.5.1 Results

The CARIOCA prototype IV successfully operates at 2.5 V of power supply. The measurements are taken using the same test environment and the methods

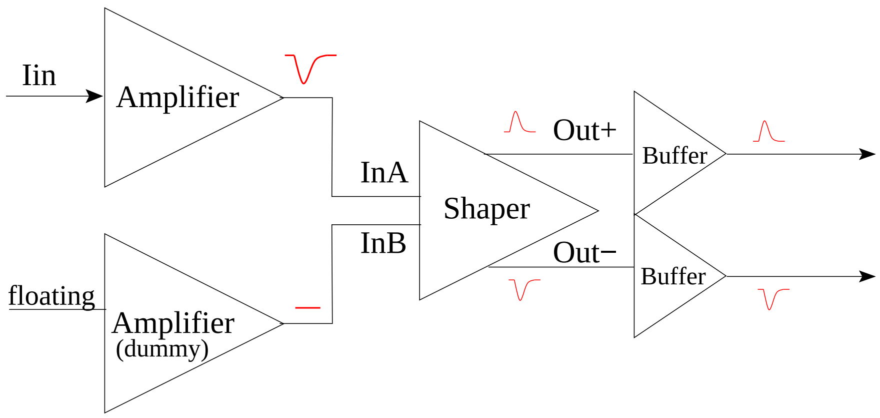
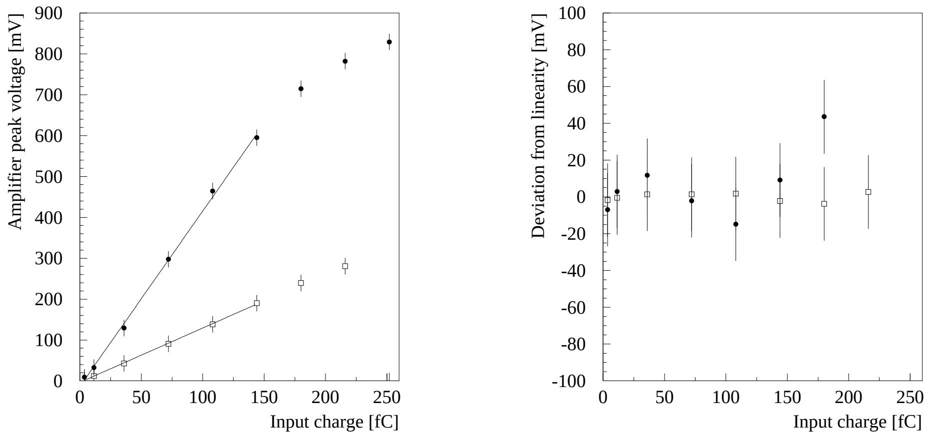


Figure 7.24: Analog structure of one channel of CARIOCA prototype IV.

previously described. The measured signal amplitude as a function of the input charge is shown in Figure 7.25, together with the deviation from linearity, for 27 pF and 220 pF input capacitance. The sensitivity up to 150 fC is found to be 4.3 mV/fC and 1.3 mV/fC at 27 pF and 220 pF input capacitance, respectively. A non linearity of about 20 % is observed for 250 fC input charge, at 27 pF input capacitance. The sensitivity dependence on the input capacitance, shown in Figure 7.26(a) for a delta input signal of 36 fC, is of the same order of the one measured for the previous prototype and its is manly due to the amplifier.

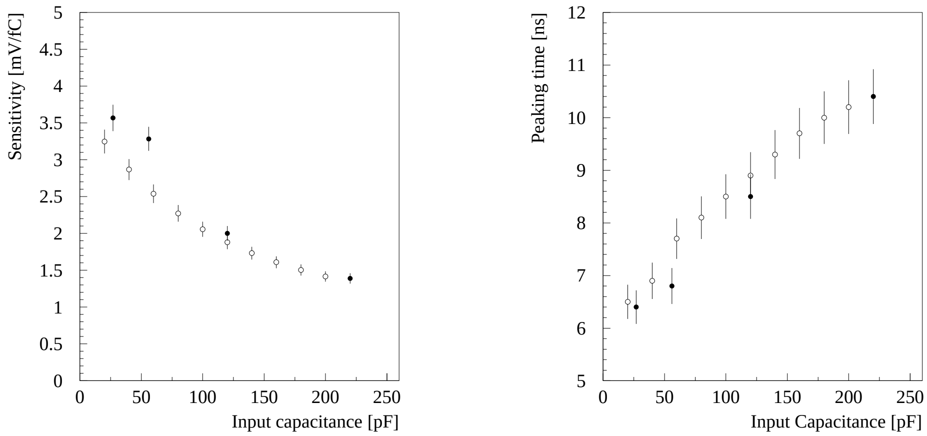
The peaking time shown in Figure 7.26(b) ranges from 6.5 to 10.5 ns and is faster than the prototype III. This is due to the higher bandwidth of the shaper circuit. The results obtained with this prototype are different from previous prototypes I and II, because on the first two prototypes the amplifier was coupled with the current discriminator that changed the amplifier behavior; not allowing the good measurement of the amplifier characteristics.

Figure 7.27 shows the measured equivalent noise charge, that is found to be equal to 2671 e^- with a slope of 54.6 e^-1/pF. The noise is higher than the measured noise for the positive input polarity amplifier alone, because this chip has two amplifiers contributing to the noise.



(a) (b)

Figure 7.25: (a) Shaper output peak voltage and (b) deviation from linearity as function of the input charge for 27 pF (black circles) and 220 pF (white squares) input capacitance. The fit up to 150 fC shows a gain of 4.3 mV and 1.3 mV for 27 pF and 220 pF input capacitance, respectively.



(a) (b)

Figure 7.26: Sensitivity (a) and peaking time (b) for 36 fC input charge versus input capacitance for measurement (black circles) and simulation (white circles).

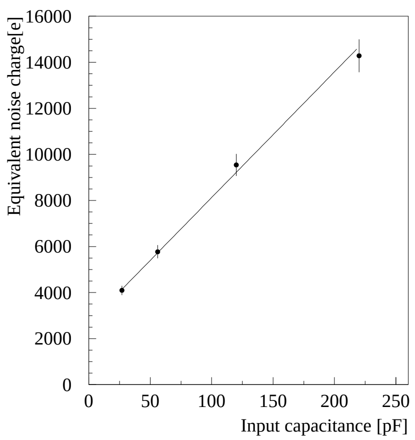


Figure 7.27: Measured equivalent noise charge for the CARIOCA prototype IV.

Figure 7.28 shows the chip output voltage for a 1/t signal injector with 280 fC input charge and 56 pF input capacitance. The top curve is the difference of positive and negative outputs. Middle curves are positive and negative outputs and the bottom one the sum of these two outputs. The output signal is not exactly differential, being the sum not zero. However, the tail cancellation is not spoiled at large input charge. The output signal width is less than 30 ns, as required, and it displays a small overshoot of about 40 ns after the signal peak.

7.5.2 Shaper Test on MWPC Prototype

The CARIOCA prototype IV is tested in a LHCb wire pad chamber prototype [78], with ^{241}Am source. The chip is connected to a cathode pad readout of 50 pF capacitance and the chamber operates at 2.95 kV. Figure 7.29 shows the negative output pulse of the shaper circuit, with a perfect tail cancellation.

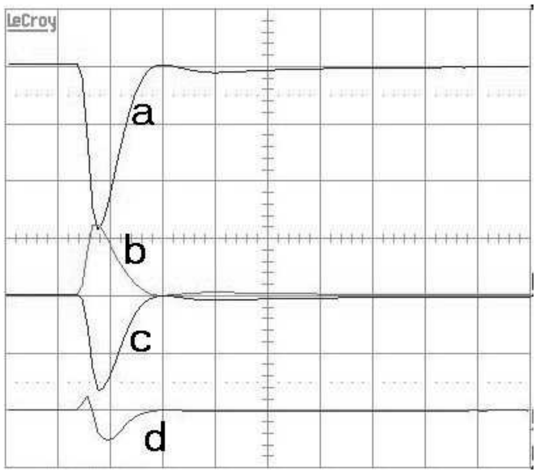


Figure 7.28: Shaper output pulses for a 1/t input signal with 280 fC charge at an input capacitance of 56 pF. (a) difference of positive and negative outputs; (b) positive output; (c) negative output and (d) sum of these two outputs. The horizontal scale is 20 ns per division and the vertical scale is 300 mV per division.

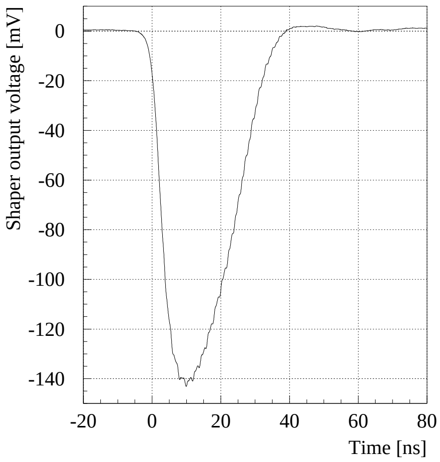


Figure 7.29: Shaper negative output voltage for the 50 pF MWPC cathode pad.

7.6 Prototype V - Positive ASD Polarity

This prototype is a four-channel amplifier, shaper and discriminator (ASD) chip, implemented in a $2{\times}4\,\mathrm{mm}^2$ die with a total of 64 pads. It was build in August of 2001 with the aim of testing the discriminator circuit. The chip contains four channels of positive input polarity amplifier, followed by shaper, discriminator and LVDS driver; fully differential. A block diagram of one channel is shown in Figure 7.30. The amplifier and shaper circuits are described in the previous sections. The shaper differential output is AC coupled to the discriminator input. The AC network (not shown) is used to fix the DC voltage in front of the discriminator. This DC voltage is given by a common-mode voltage set to 1.5 V. The discriminator is a high gain differential amplifier with symmetric current mirror loads. The circuit is similar to the one described in Section 6.8 and shown in Figure 6.23. The main difference is the gain. On this CARIOCA prototype the discriminator circuit has less gain than what is expected. This is corrected for the final CARIOCA prototype.

The layout of the chip is similar to the previous prototypes. The amplifier bias currents are provided to each pair of amplifier at the same time, while each shaper and each discriminator have independent bias current. The power supply is laid out independently for the amplifiers, the shapers and the discriminators.

7.6.1 Chip Test

The CARIOCA prototype V is bonded in the printed circuit board, to minimize parasitics and, consequently, the deterioration of the performance. The chip output (LVDS output) is terminated with a $100\,\Omega$ resistor on the board and is directly read by the oscilloscope through a high impedance probe. The channels are independently provided with bias currents via resistors on the board, supplied with 2.5 V. The experimental setup uses a pulse generator, a power supply and a digital oscilloscope connected to a computer via GPIB interface. All the mea-

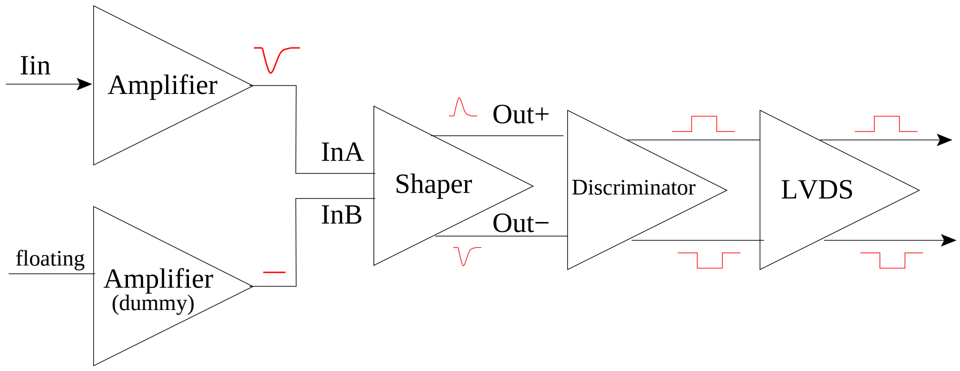


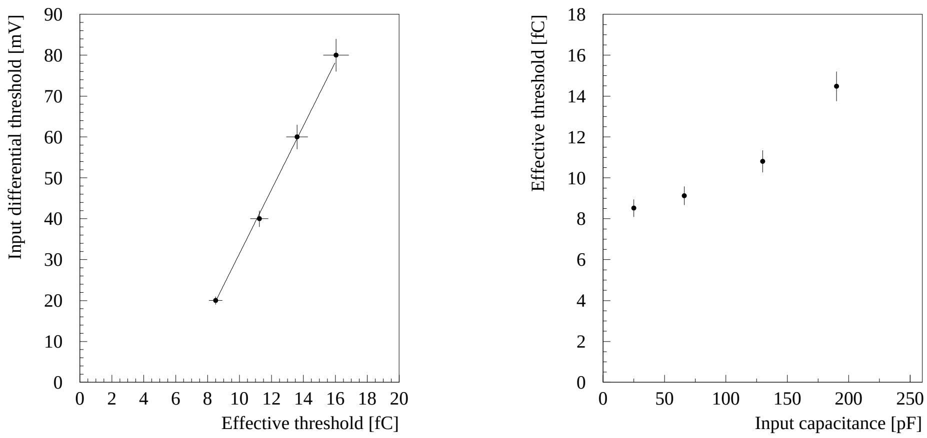
Figure 7.30: Block diagram of one channel of the CARIOCA prototype V.

surements are taken and analyzed with Labview program. Since this prototype has no analog output, it is not possible to measure the amplifier characteristics.

Figure 7.31(a) shows the correlation between the input differential threshold and the measured effective threshold for delta input pulses at 56 pF input capacitance. The slope of this curve is about 8 mV/fC and it gives the circuit sensitivity in front of the discriminator. The effective threshold dependence on the input capacitance is shown in Figure 7.31(b) for a differential threshold input of 20 mV, corresponding to a charge detection of 8 fC. The sensitivity reduces to 50 % in the capacitance range from 10 to 250 pF and well agree to the results shown in Figure 7.26(a).

The equivalent noise charge is measured for different input capacitance, using the S-curve method described in section 7.3.1. Figure 7.32 shows the measured equivalent noise charge for delta input signals. A linear fit, considering a 5 % error on the data, gives a noise of 1744 e^- with a slope of 40.5 e^-/pF. The value is smaller than the noise measured for prototype IV and it can be explained by pick-up present in the prototype IV test board. Analog signal processing is much more sensitive than digital one.

One important characteristic of the circuit is the time walk, that is the difference in threshold crossing times. This quantity is a dominant factor in the



(a) (b)

Figure 7.31: (a) Relation between the input differential threshold and the The slope is about 8 mV/fC. (b) Measured effective threshold as a function of the input capacitance for 20 mV input differential threshold.

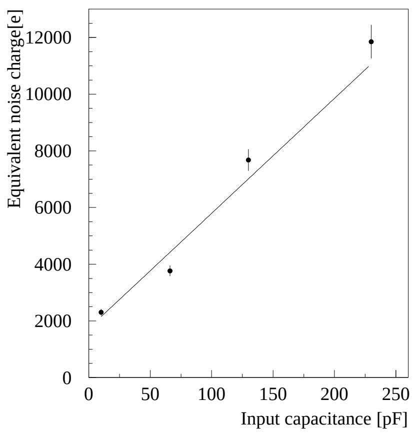


Figure 7.32: Measured equivalent noise charge as a function of the input capacitance for the CARIOCA prototype V.

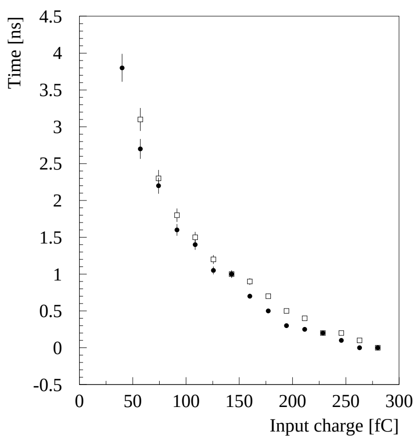


Figure 7.33: Measured time walk as a function of the input charge for CARIOCA prototypes IV (square) and V (circle). This measurement uses a 1/t input signal at 56 pF input capacitance and 20 mV differential input threshold.

detector time resolution measurement. Figure 7.33 shows the measured time walk for CARIOCA prototypes IV and V, considering a 1/t input pulse at 56 pF input capacitance and 20 mV differential input threshold. The similarity of the measured values for both chips shows that the discriminator circuit adds very little to the intrinsic time resolution due to time walk. A time walk of 2.7 ns is obtained for an input charge range from 50 fC to 260 fC, showing an excellent performance of the circuit and agreeing with the requirements.

The channel-to-channel uniformity is measured with a 36 fC delta input signal and 56 pF input capacitance. The threshold measurement shows a 30 % peak-to-peak non uniformity. This large spread can be explained by the non uniformity of the resistance and capacitance used on the AC network at the discriminator input. Each of this element has an error of about 20 %, quoted by the manufacturer. This circuit is not present on the final prototype. The crosstalk is measured to be smaller than 0.5 %. This results is limited by the measurement method, that do not allow a lower limit.

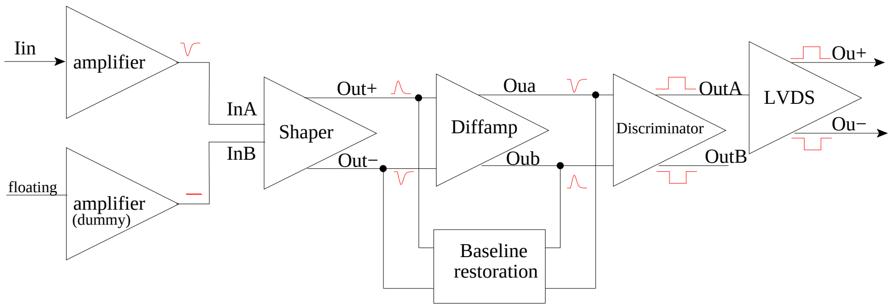


Figure 7.34: Block diagram of one channel of the CARIOCA ASDB prototype.

7.7 Prototype VI - Positive ASDB Polarity

The seventh CARIOCA prototype is a nine-channel ASD chip with baseline restoration circuit (ASDB). It is fabricated in a $3{\times}4\,\mathrm{mm}^2$ die with 74 pads. Each channel is composed by two positive input polarity amplifiers, a shaper, a differential amplifier, a baseline restoration, a discriminator and a LVDS driver, as shown in Figure 7.34.

The amplifier, shaper and discriminator circuit are already tested and the results are shown in the previous sections. The differential output of the shaper is sent to the differential amplifier. The differential amplifier is an additional circuit, described in Section 6.6, implemented to cancel the amplifier signal tail. It works as gain and shaping stage and is complementary to the shaper circuit. It has the advantage of give a correct DC balance to the discriminator input, despising the use of a dedicated AC network. The DC output voltage of this amplifier is established by common mode feedback, that drives the output voltage to a reference voltage. This reference voltage of 1.5 V is common to the differential amplifier and the baseline restoration.

In parallel to the differential amplifier there is a baseline restoration circuit, already described in Section 6.7. It consists of three amplifiers that samples the voltage on the differential amplifier output, performs some analog signal

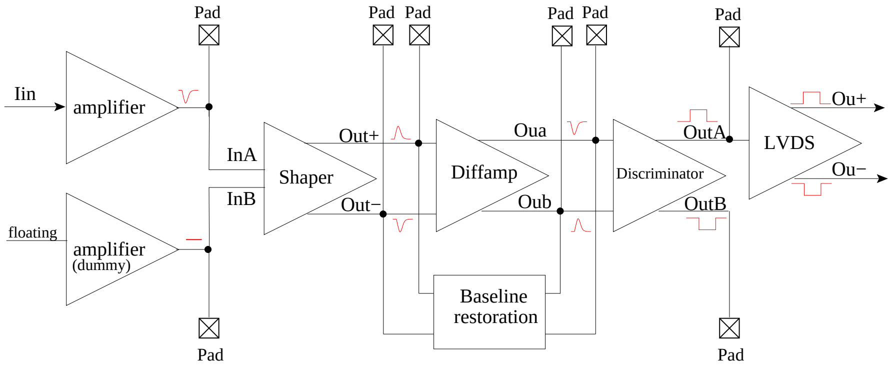


Figure 7.35: CARIOCA ASDB prototype channel 9 block diagram and pad connections.

processing and feeds back the signal to the input of the differential amplifier, eliminating or reducing baseline shifts. The baseline has a long time constant, around 5 μs, and it does not influences the circuit bandwidth.

The positive output of the discriminator is sent to the LVDS driver, that provides a differential output. Just one discriminator output is used, because the LVDS driver developed for the 0.25 μm technology has single input and there is no need to connect two LVDS driver.

In this prototype there are similar eight channels and an extra channel with analog signal access. This access is used to probe internal circuit nodes to verify circuit stability and offsets. This is possible via seven pads placed across the channel layout. Figure 7.35 shows the block diagram of this extra channel, with the pads connection. On this channel there are four probe pads, not shown in the block diagram, connected to the first and second nodes of the BLR.

The CARIOCA prototype VI is a close to final version of the CARIOCA circuit. This prototype was designed in November of 2001 and the chip should be available for testing in March of 2002. Since it is not yet ready for tests, there are no measurement results presented in this thesis. A detailed description of the chip layout and working properties are discussed in the next section.

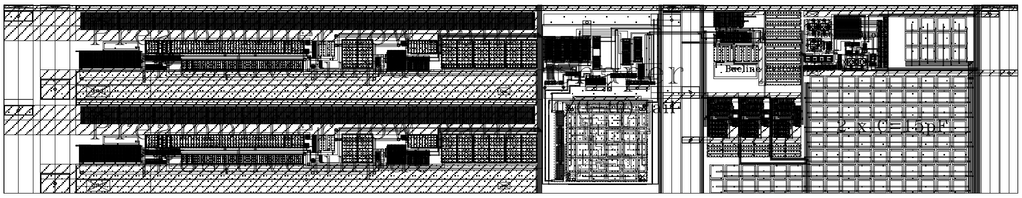


Figure 7.36: Layout of one channel of the CARIOCA positive polarity ASDB.

7.7.1 Circuit Layout

In the present prototype, nine channels of the CARIOCA ASDB are implemented in a 3 mm×4 mm die. Enclosed devices are used in the layout of nmos transistors, implying a limit on the length and width of these transistors. The resistors are made with polysilicon and the capacitors use a metal-insulator-metal process described in Section A.5.2. Each channel has a size of 1717.42μm by 319.12μm and the layout is shown in Figure 7.36. To reduce the channel-to-channel crosstalk a barrier of 8 μm width with all metal layers connected to the substrate is created between each channel.

Figure 7.37 shows the pad positions of the positive input polarity chip. All analog inputs are placed on the left side of the chip while the LVDS outputs are in opposite side. The top and bottom sides are used by the bias lines, the power supply and the monitoring pads. A pad description is shown in Tables 7.1 and 7.2. The power supply buses are connected to pads on both top and bottom side of the chip to minimize the voltage drop along the circuit. In order to minimize the noise coupling between the power lines and the substrate, the signal chain is divided into four main parts: (1) amplifier, (2) shaper, differential amplifier and baseline restoration, (3) discriminator and (4) LVDS driver. Both V_{DD} and ground are provided independently to each of these parts.

Internal nodes of the circuit can be verified by seven pads placed across the layout of channel 9. The pads location are shown in Figure 7.35. The DC voltage across the baseline restoration circuit can be verified by four probe pads connected

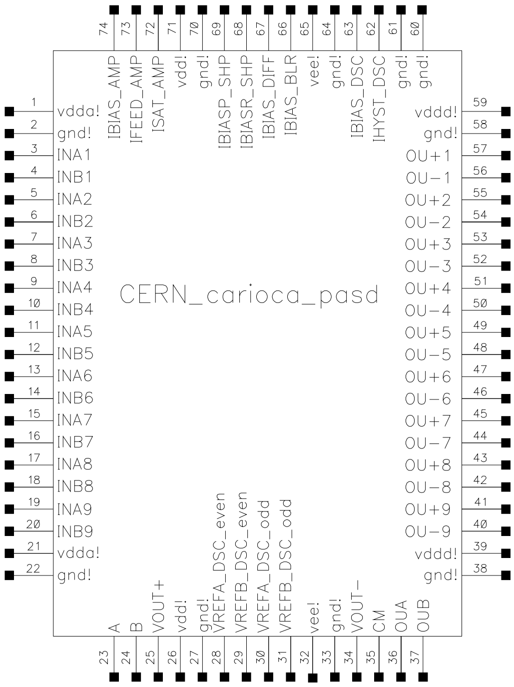


Figure 7.37: CARIOCA positive polarity ASDB chip pin-out diagram.

to the first and second nodes of the BLR. However these pads are accessible only by means of a probe station.

Each die has a 74 pads of $107\,\mu\text{m}\times 107\,\mu\text{m}$ metal layer, with a pitch of $125\,\mu\text{m}$. The internal pad is a $50\,\mu\text{m}\times 50\,\mu\text{m}$ metal layer. To test the main functionality of the circuit the last channel (number 9) is not needed and the number of used pads reduce to 61. In this case the chip can be packaged on a 64-pin package with an internal dimension of about $6\times 6\,\text{mm}^2$.

7.7.2 Working Properties

The CARIOCA ASDB circuit works at 2.5 V power supply and has to be provided with a total of 9 bias currents. The optimum values for these currents are summarized in Table 7.3. These values should not vary by more than 10 %, in order to keep the optimum circuit performance.

Pad N^o	**Pad Name**	**I/O Type**	**Description**
1 & 21	vdda!	Power	Amplifier power supply (+2.5 V)
2 & 22	gnd!	Power	Amplifier ground (0 V)
3 to 19	INA1:INA9	Analog In +	Signal input
4 to 20	INB1:INB9	Analog In -	Dummy input
23	A	Monitoring	Amplifier output from INA9
24	B	Monitoring	Amplifier output from INB9
25	VOUT+	Monitoring	Shaper positive output (ch. 9)
26 & 71	vdd!	Power	Shaper, differential amplifier and BLR power supply (+2.5 V)
27 & 70	gnd!	Power	Shaper, differential amplifier and BLR ground (0 V)
28	VREFA_DSC (even)	Voltage Input	Positive threshold voltage for even channels (2,4,6 and 8)
29	VREFB_DSC (even)	Voltage Input	Negative threshold voltage for even channels (2,4,6 and 8)
30	VREFA_DSC (odd)	Voltage Input	Positive threshold voltage for odd channels (1,3,5,7 and 9)
31	VREFB_DSC (odd)	Voltage Input	Negative threshold voltage for odd channels (1,3,5,7 and 9)
32 & 65	vee!	Power	Discriminator power supply (+2.5 V)
33 & 64	gnd!	Power	Discriminator ground (0 V)

Table 7.1: Pads information of the CARIOCA ASDB prototype for positive read-out, named CERN_carioca_pasd.

Pad N^o	**Pad Name**	**I/O Type**	**Description**
34	VOUT-	Monitoring	Shaper negative output (ch. 9)
35	CM	Monitoring	Common mode voltage (ch. 9)
36	OUA	Monitoring	Differential amplifier negative output (ch. 9)
37	OUB	Monitoring	Differential amplifier positive output (ch. 9)
38 & 58	gnd!	Power	LVDS driver ground (0 V)
39 & 59	vddd!	Power	LVDS driver power supply
			(+2.5 V)
40 to 56	OU-9:OU-1	Analog Out -	LVDS negative output
41 to 57	OU+9:OU+9	Analog Out +	LVDS positive output
60 & 61	gnd!	Power	Discriminator ground (0 V)
62	IHYST_DSC	Current Input	Discriminator hysteresis current
63	IBIAS_DSC	Current Input	Discriminator bias current
66	IBIAS_BLR	Current Input	BLR bias current
67	IBIAS_DIFF	Current Input	Differential amplifier bias current
68	IBIASR_SHP	Current Input	Bias current for the shaper input
69	IBIASP_SHP	Current Input	Shaper bias current
72	ISAT_AMP	Current Input	Amplifier saturation current
73	IFEED_AMP	Current Input	Amplifier feedback current
74	IBIAS_AMP	Current Input	Amplifier bias current

Table 7.2: Pads information of the CARIOCA ASDB prototype for positive read-out, named CERN_carioca_pasd.

The positive input polarity amplifier is supplied with three currents: bias current (IBIAS_AMP), feedback current (IFEED_AMP) and saturation current (ISAT_AMP). IBIAS_AMP is responsible for the input transistor drain current, while IFEED_AMP is used on the output current mirror, setting the DC output current. The saturation current is an additional current that is added to the positive input polarity amplifier to increase the amplifier linear range, as described in Section 6.4.2.

The shaper uses a current (IBIASR_SHP) to bias the transistor on the current-to-voltage converter, shown in Figure 6.9. IBIASP_SHP works as a bias current for the main differential pair. The differential amplifier and the baseline network are biased by IBIAS_DIFF and IBIAS_BLR, respectively. The discriminator circuit is supplied with two currents: IBIAS_DSC and IHYST_DSC. IBIAS_DSC is responsible for the main differential pair biasing. IHYST_DSC is the hysteresis current.

7.7.3 Simulation Results

Simulations of the CARIOCA prototype VI shows a voltage gain of 6.3 mV/fC at the discriminator input, up to a charge of 250 fC with good linearity, shown in Figure 7.38. The sensitivity and the voltage peaking time show a small dependence on the input capacitance, as illustrated in Figure 7.39, also for the node in front of the discriminator. The circuit speed degrades with the input capacitance, but for large capacitances it has still a fast peaking time.

The circuit shows a small time walk of about 1.6 ns for the input charge range from 50 fC to 260 fC, as shown in Figure 7.40. The simulated power consumption of one channel is 28.2 mW, for 2.5 V power supply. The simulation results perfectly agree with the LHCb Muon System requirements. Since simulations and measurements of previous prototypes showed good agreement, measurement results within 10 % fluctuation of the values above are expected for this prototype.

Pad Name	**Current (μA)**	**DC voltage (V)**	**Proposed Connection**
IBIAS_AMP	150	1.146	9 kΩ refereed to +2.5
IFEED_AMP	6	1.943	315 kΩ refereed to 0.0
ISAT_AMP	530	1.221	2.3 kΩ refereed to 0.0
IBIASP_SHP	20	1.253	63 kΩ refereed to 0.0
IBIASR_SHP	40	0.900	40 kΩ refereed to +2.5
IBIAS_DIFF	55	1.653	30 kΩ refereed to 0.0
IBIAS_BLR	50	1.764	35 kΩ refereed to 0.0
IBIAS_DSC	100	1.520	15 kΩ refereed to 0.0
IHYST_DSC	6	0.665	305 kΩ refereed to +2.5

Table 7.3: Optimized supply currents for the CARIOCA ASDB prototype VI. DC voltage is the measured voltage on the chip pad, when it is powered. These current values can be obtained with the proposed resistor connection.

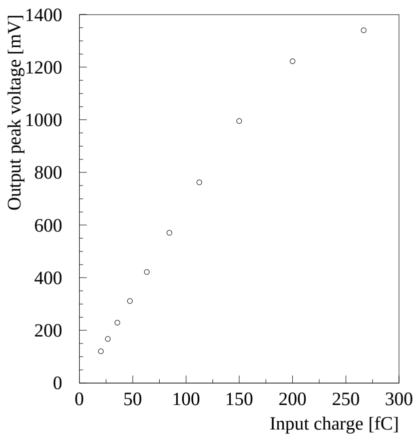


Figure 7.38: Simulated peak voltage at the discriminator input of CARIOCA prototype VI, for a delta input signal at 60 pF input capacitance. The fit up to 250 fC shows a gain of 6.3 mV.

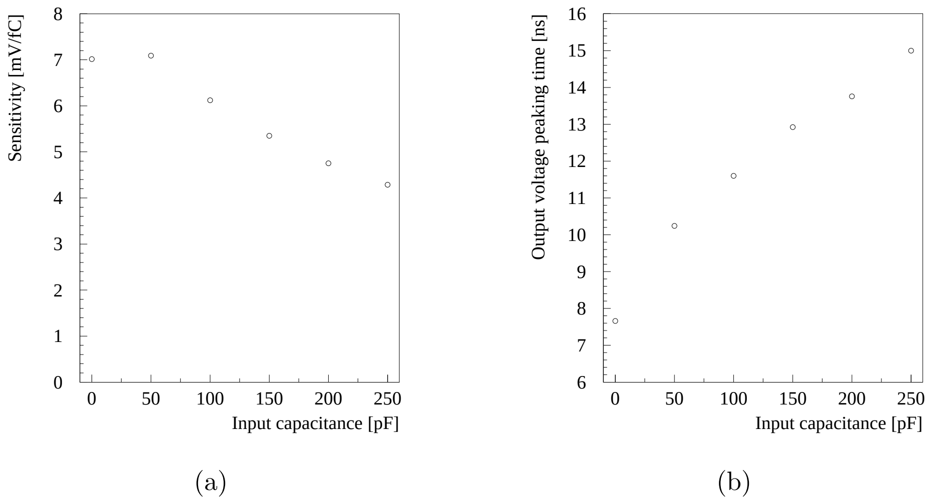


Figure 7.39: Simulated sensitivity (a) and peaking time (b) dependence on the input capacitance for 60 fC input charge.

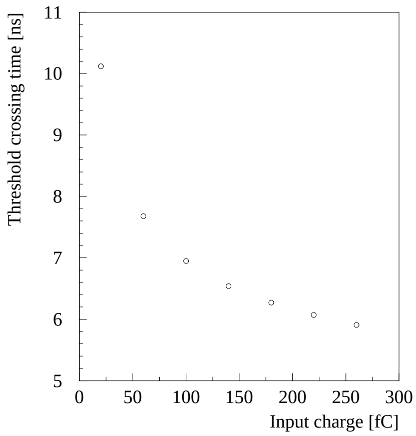


Figure 7.40: Prototype VI discriminator time walk as a function of the input charge, for 60 pF input capacitance.

7.8 Prototype VII - Negative ASDB Polarity

The CARIOCA prototype VII is a nine-channel ASDB chip with baseline restoration circuit (ASDB). It is implemented in $3{\times}4\,\mathrm{mm}^2$ die with 74 pads. Each channel is composed by two negative input polarity amplifier, a shaper, a differential amplifier, a baseline restoration, a discriminator and a LVDS driver, as shown in Figure 7.34. The chip circuit and layout are similar to the CARIOCA prototype VI, differing only by the amplifier input polarity and one bias current (ISAT_AMP) that is not present on the negative polarity amplifier. Figure 7.41 shows the pad position of this prototype. The CARIOCA prototype VII pads are described in Tables 7.4 and 7.5. This prototype was developed in the same time of the prototype VI and it is also not ready for tests. The working properties are similar to the positive input polarity chip and are summarized in Table 7.6. The only difference between the positive polarity circuit (CERN_carioca_pasd) and the negative negative polarity (CERN_carioca_nasd) is the feedback current polarity (IFEED_AMP).

The simulation of the CARIOCA prototype VII shows a voltage gain of 7.4 mV/fC up to a charge of 200 fC, at the discriminator input. The linearity is shown in Figure 7.42 for an input capacitance of 60 pF. Figure 7.43 shows the sensitivity and the voltage peaking time dependence on the input capacitance. The discriminator time walk, shown in Figure 7.44, is similar to the prototype VI. The simulated power consumption of one channel is 23.9 mW, for 2.5 V power supply. This prototype consumes less power compared to prototype VI, because it drives less current. It does not have the additional current ISAT_AMP.

The results presented in this chapter proves that the CARIOCA circuit works for a for a large range of input capacitances, keeping low noise and high speed.

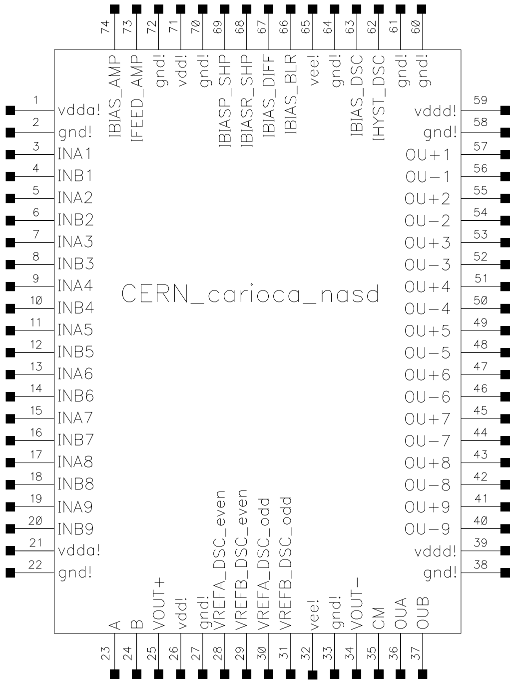


Figure 7.41: CARIOCA negative polarity ASDB chip pin-out diagram.

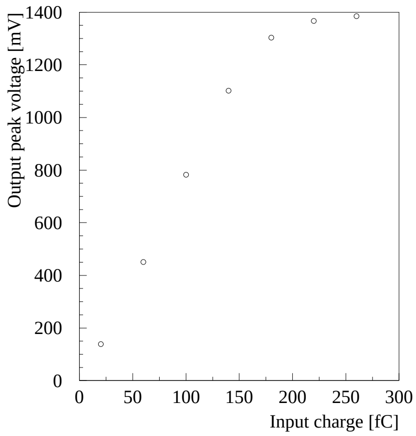


Figure 7.42: Simulated peak voltage at the discriminator input of CARIOCA prototype VII, for a delta input signal at 60 pF input capacitance. The fit up to 250 fC shows a gain of 6.3 mV.

Pad N^o	Pad Name	I/O Type	Description
1 & 21	vdda!	Power	Amplifier power supply (+2.5 V)
2 & 22	gnd!	Power	Amplifier ground (0 V)
3 to 19	INA1:INA9	Analog In -	Signal input
4 to 20	INB1:INB9	Analog In +	Dummy input
23	A	Monitoring	Amplifier output from INA9
24	B	Monitoring	Amplifier output from INB9
25	VOUT+	Monitoring	Shaper positive output (ch. 9)
26 & 71	vdd!	Power	Shaper, differential amplifier and BLR power supply (+2.5 V)
27 & 70	gnd!	Power	Shaper, differential amplifier and BLR ground (0 V)
28	VREFA_DSC (even)	Voltage Input	Positive threshold voltage for even channels (2,4,6 and 8)
29	VREFB_DSC (even)	Voltage Input	Negative threshold voltage for even channels (2,4,6 and 8)
30	VREFA_DSC (odd)	Voltage Input	Positive threshold voltage for odd channels (1,3,5,7 and 9)
31	VREFB_DSC (odd)	Voltage Input	Negative threshold voltage for odd channels (1,3,5,7 and 9)
32 & 65	vee!	Power	Discriminator power supply
			(+2.5 V)
33 & 64	gnd!	Power	Discriminator ground (0 V)

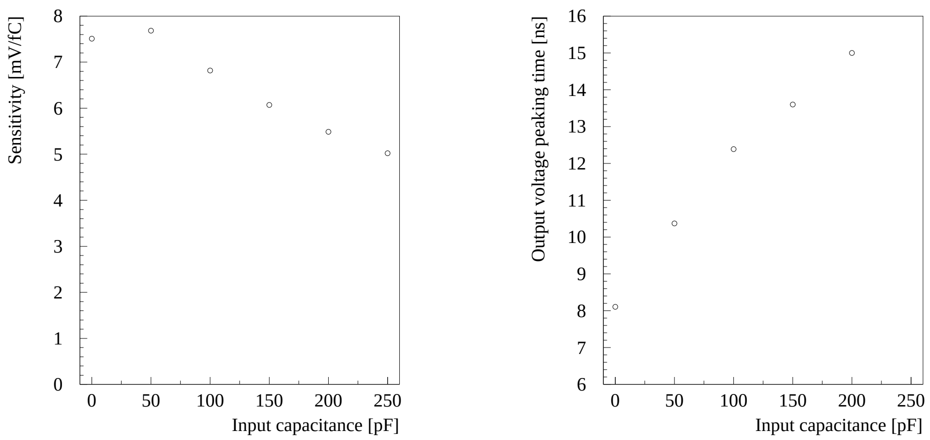
Table 7.4: Pads information of the CARIOCA ASDB prototype for negative readout, named CERN_carioca_nasd.

Pad N^o	**Pad Name**	**I/O Type**	**Description**
34	VOUT-	Monitoring	Shaper negative output (ch. 9)
35	CM	Monitoring	Common mode voltage (ch. 9)
36	OUA	Monitoring	Differential amplifier negative output (ch. 9)
37	OUB	Monitoring	Differential amplifier positive output (ch. 9)
38 & 58	gnd!	Power	LVDS driver ground (0 V)
39 & 59	vddd!	Power	LVDS driver power supply
			(+2.5 V)
40 to 56	OU-9:OU-1	Analog Out -	LVDS negative output
41 to 57	OU+9:OU+1	Analog Out +	LVDS positive output
60 & 61	gnd!	Power	Discriminator ground (0 V)
62	IHYST_DSC	Current Input	Discriminator hysteresis current
63	IBIAS_DSC	Current Input	Discriminator bias current
66	IBIAS_BLR	Current Input	BLR bias current
67	IBIAS_DIFF	Current Input	Differential amplifier bias current
68	IBIASR_SHP	Current Input	Bias current for the shaper input
69	IBIASP_SHP	Current Input	Shaper bias current
72	gnd!	Power	Amplifier ground (0 V)
73	IFEED_AMP	Current Input	Amplifier feedback current
74	IBIAS_AMP	Current Input	Amplifier bias current

Table 7.5: Pads information of the CARIOCA ASDB prototype for negative readout, named CERN_carioca_nasd.

Pad Name	**Current (μA)**	**DC voltage (V)**	**Proposed Connection**
IBIAS_AMP	150	1.146	9 kΩ refereed to +2.5
IFEED_AMP	6	0.570	315 kΩ refereed to +2.5
ISAT_AMP	530	1.221	2.3 kΩ refereed to 0.0
IBIASP_SHP	20	1.253	63 kΩ refereed to 0.0
IBIASR_SHP	40	0.900	40 kΩ refereed to +2.5
IBIAS_DIFF	55	1.653	30 kΩ refereed to 0.0
IBIAS_BLR	50	1.764	35 kΩ refereed to 0.0
IBIAS_DSC	100	1.520	15 kΩ refereed to 0.0
IHYST_DSC	6	0.665	305 kΩ refereed to +2.5

Table 7.6: Optimized supply currents for the CARIOCA ASDB prototype VII.



(a) (b)

Figure 7.43: Simulated sensitivity (a) and peaking time (b) dependence on the input capacitance for 60 fC input charge.

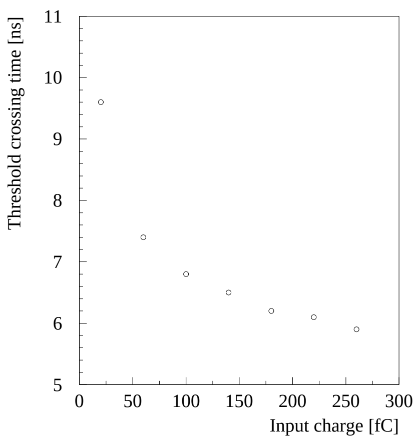


Figure 7.44: Prototype VII discriminator time walk as a function of the input charge, for 60 pF input capacitance.

7.9 Radiation Tests

Irradiation test are not yet done in any prototype, but previous results [118] using 0.25 μm CMOS technologies combined with enclosed layout transistors and guard-rings have shown a very good resistance to total dose radiation damage up to 30 mRad.

7.10 Summary

This thesis presented the design and test of the CARIOCA integrated circuits, developed for anode and cathode readout of Multi Wire Proportional Chambers. For the test of this front-end, seven prototypes were produced. These prototypes are build with the aim of testing the circuits used on the final chip in a step-by-step approach. The chips were produced in a 0.25 μm CMOS technology, using radiation tolerant layout techniques. The circuit showed a good behavior of the current-mode amplifier, that is of new concept. For the first five prototypes the measured characteristics satisfy the LHCb Muon System requirements and a good overall agreement is observed between the measurements and HSPICE simulation results. Prototypes VI and VII are under test at CERN.

Parte IV

Conclusão

Capítulo 8

Conclusão

Esta tese apresenta dois trabalhos desenvolvidos no âmbito das colaborações internacionais DELPHI e LHCb, ambas no CERN. A procura por sinais de violação da paridade R no DELPHI, foi feita utilizando-se os dados de colisões e^+e^- do LEP, coletados durante os anos de 1997 à 2000, com energia de centro de massa entre 183 GeV e 208 GeV e luminosidade integrada de aproximadamente 654 pb^{-1}. Neste trabalho assumiu-se que a massa do sneutrino é maior que 300 GeV/c^2 e que a violação espontânea da paridade R ocorre somente na 3ª geração. Neste caso, o modo dominante de decaimento do chargino é o processo $\tilde{\chi}^+ \rightarrow \tau^+ J$.

A procura por $\tilde{\chi}^+ \rightarrow \tau^+ J$ resultou em 72 candidatos e 72.3 ± 2.5 eventos de *background*, selecionados com uma eficiência de 19.8 ± 0.6 %. Nenhuma evidência de violação espontânea da paridade R foi observada e um limite superior de 0.14 pb na seção de choque de produção do chargino foi encontrado, considerando-se 95 % de *confidence level*. O chargino só pode ser produzido com seção de choque ≤ 0.14 pb se a sua massa for ≥ 103.8 GeV/c^2, como ilustrado na Figura 3.11. Com estes limites foi possível construir os domínios de exclusão do plano (μ, M_2) dos parâmetros do MSSM, mostrados na Figura 3.12.

O circuito integrado CARIOCA, desenvolvido para leitura anódica e catódica de câmaras proporcionais multifilares, foi produzido na tecnologia de 0.25 μm

CMOS. Este circuito faz uso de técnicas de layout que o tornam mais resitente a radiação. Para testar independentemente diferentes partes do circuito, sete protótipos foram construídos. Testes do circuito mostraram um ótimo desempenho do amplificador de corrente. Resultados experimentais obtidos com os cinco primeiros protótipos mostraram ainda que o circuito satisfaz as condições para utilização no sistema de múons do LHCb. Os protótipos VI e VII estão sendo testado no CERN.

Appendix A

Introduction to CMOS Technologies

In this appendix I give an introduction to CMOS transistor physics and design. I start through a description of semiconductor junctions. In the second section I give an overview of transistor basic operation, models and noise behaviour. The evolution in the technology scaling and the effect of radiation in CMOS devices are discussed in Section A.3 and A.4. In Section A.5 I report on modern MOS technologies processing. Integrated circuit layout and packaging are discussed in Sections A.6 and A.7. Finally, in Section A.8 I show the CMOS transistors models used in the CARIOCA circuit simulation.

A.1 Semiconductors and *pn* Junctions

Semiconductor is a crystal lattice structure that can have free electrons (negative carriers) and/or free holes (positive carriers). Silicon is typical semiconductor that has valence four, i.e., four free electrons per atom to share with neighbor atoms in the crystal lattice covalent bonds. Intrinsic silicon, i.e. undoped silicon, is a pure crystal structure having equal numbers of free electrons and holes. At room temperature, there are approximately 1.5×10^{10} carriers of each type per cm^3.

The silicon can be doped with an impurity of higher valence as phosphorus or arsenic, whose valence is 5. In this case the impurity atoms uses four of its valence electrons to form the crystal bonds and one electron is left free. Such impurity is called *donor* because it can give up a negative carrier to a crystal. A material with a concentration of donor impurity has negative free carries and is called n-type dopant. If the silicon is doped with some impurity atom whose valence is 3, such as boron or aluminum, these atoms try to act as a valence 4 atom, stealing an extra electron from some nearby silicon atom. When it steals an electron it leaves a hole and this hole can wander around in the silicon as a positive carrier. This kind of impurity is called *acceptor* because it "accepts"an electron. A crystal with an excess of positive carries is called p-type semiconductor.

A pn junction is made with one part of the semiconductor doped with n-type and an adjacent part doped with p-type. The p side has a large number of free holes, while the n side has many free electrons. The holes tends to diffuse into the n side and the electrons tends to diffuse into the p side, recombining. Each electron that diffuses leaves a positive charge bound and, similarly, each hole that diffuse leaves a negative charge bound, as shown in Figure A.1. This creates a depletion region at the junction of the two sides, where no free carries exists. As these bound charges are exposed, an electric field (built-in potential) develops going from the n side to the p side. It opposes the diffusion of free carriers until there is no movement of charge under open circuit.

Some times the notation p^+, p^-, n^+, n^- is used for the doped regions. In this case the superscripts indicate the relative doping levels. For example, the p^- region might have an impurity concentration of 5×10^{21} carriers/m^3, whereas the p^+ regions would be doped more heavily to a value around 10^{25} to 10^{27}.

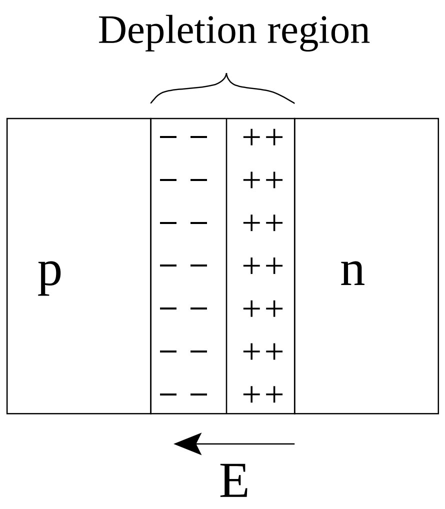


Figure A.1: Example of a *pn* junction.

A.2 MOS Transistors

MOS (Metal-Oxide-Semiconductor) circuits normally uses two complementary types of transistors, n-channel and p-channel, and are called CMOS circuits. While n-channel devices conduct with a positive gate voltage, p-channel conduct via a negative gate voltage. Transistor channel is the area between the two heavily doped regions and its type is determined by doping type. The n-channel transistors are named nmos and the p-channel are named pmos.

Figure A.2 shows a simplified structure of a nmos device on a p-type substrate. The device consists of two heavily doped n regions (n^+), diffused into a lighter doped p material called substrate or bulk (B), forming the source (S) and the drain (D) terminals. A conductive piece of polysilicon[1] (poly), on top of a thin layer of insulator (silicon dioxide), operates as gate (G). The gate is electrically isolated from the n^+ regions, affecting only through capacitive coupling. The distance between drain and source is the channel length (L) and the dimension

[1]Polysilicon is silicon in amorphous (non-crystal) form

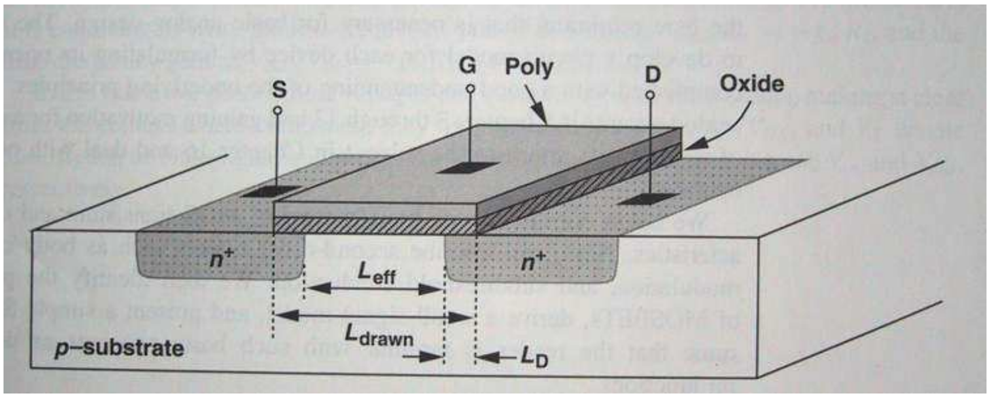


Figure A.2: Structure of a nmos transistor.

perpendicular to the length is the channel width (W). Since during the fabrication the S/D junction diffuses, the actual channel length is slightly smaller and is called effective length (L_{eff}).

There is no physical difference between source and drain. The source terminal of a nmos is defined as the terminal with lower voltage, while for the pmos it is the terminal with higher voltage. When a transistor is turned on, the current flows from the drain to the source in a nmos and from the source to the drain in a pmos. In both cases, the free carries travel from source to drain but the current directions are different because n-channel carriers are negative and p-channel carriers are positive.

Figure A.3 shows a pmos transistor structure. It is build identical to the nmos by negating all of the doping types. In practice both transistors type are fabricated in the same wafer (same substrate) and the pmos is placed in a local substrate of n-type, called n-well. Since in a MOS operation the source/drain junction must be reversed-bias, the bulk terminal of a nmos transistor has to be connected to the most negative supply in the system while for a pmos it is connected to the most positive supply. Figure A.4 shows the circuit symbols used to represent nmos and pmos transistors.

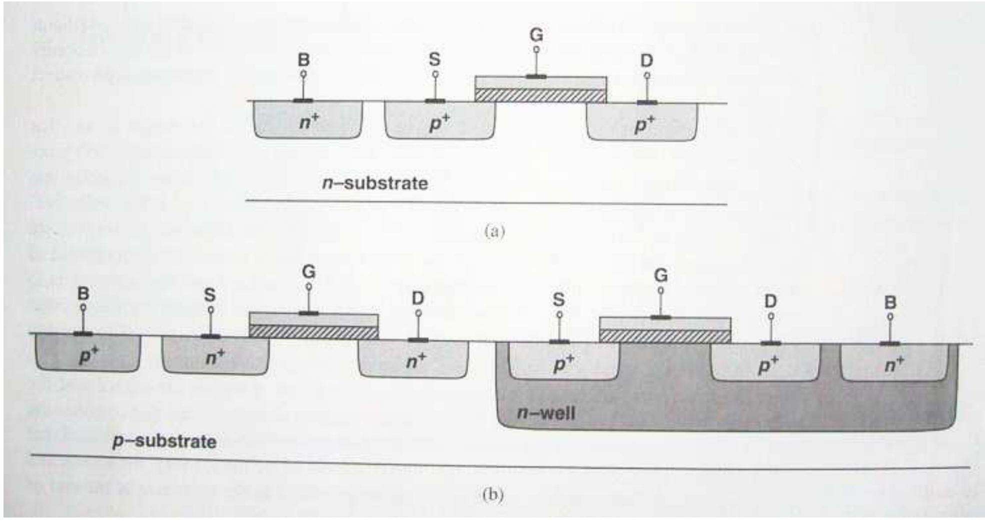


Figure A.3: (a) Structure of a pmos device in a n-type substrate. (b) Structure of a nmos (left side) and pmos (right side) devices in a p-type substrate.

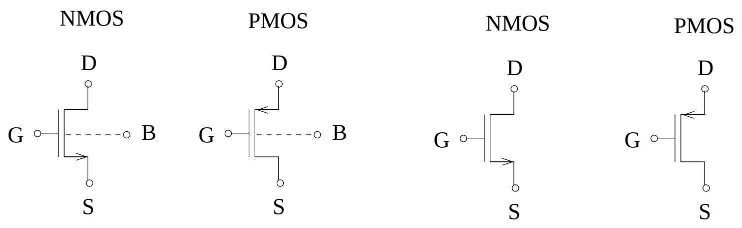


Figure A.4: MOS symbols.

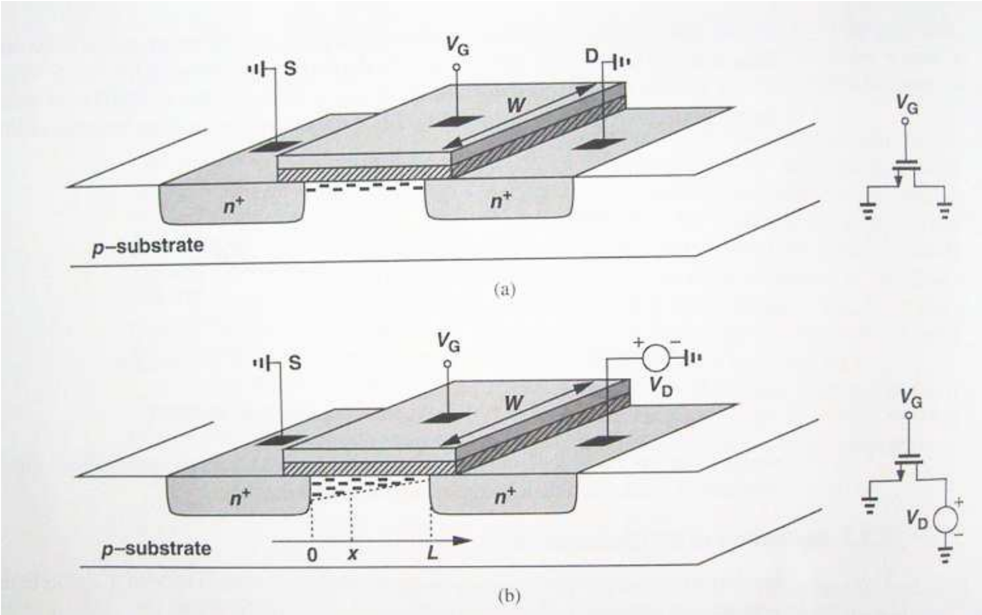


Figure A.5: Channel charge with (a) equal source and drain voltages and (b) unequal source and drain voltages.

A.2.1 Basic Operation

If the terminals S, D and B of a nmos transistor are connected to ground, the device operates as a capacitor. If the gate voltage (V_G) is very negative ($V_G << 0$), positive charges are attracted to the channel region, as shown in Figure A.5(a). Since the substrate is originally p^- doped, this increases the doping to p^+ and results in a accumulated channel, that is equivalent to a circuit with two back-to-back diodes.

If a small positive V_G is applied, positive carries in the channel are repulsed and the channel changes from a p^- doping level to a depletion region. As V_G increases, the gate attracts negative charges from the source and drain regions, forming a n region with mobile electrons connecting D and S, and the transistor is turned-on. It can also be said that the interface is inverted. The value of V_G for which it occurs is called threshold voltage (V_{TH}).

If V_G rises further ($V_G > V_{TH}$), the charge in the depletion region remains almost constant while the channel charge density (charge per unit of length) increases. The charge density is given by:

$$Q_d = WC_{ox}(V_{GS} - V_{TH}) \ , \tag{A.1}$$

where W is the channel width, C_{ox} the gate oxide capacitance per unit of area and V_{GS} the potential difference between G and S terminals. For the $0.25\,\mu$m CMOS technology $C_{ox} \approx 6.9\,\mathrm{fF}/\mu\mathrm{m}^2$. The turn-on phenomenon in a pmos device is similar to that of a nmos but with all polarities reversed.

If the drain voltage (V_D) increases above zero, as shown in Figure A.5(b), a potential difference between D and S exists, resulting in a current flowing from D to S called drain current (I_D). Since the potential varies from zero at S to V_D at D, the local voltage difference between the gate and the channel varies from V_G to $V_G - V_D$. As a consequence, the charge density at point x along the channel is given by:

$$Q_d(x) = WC_{ox}\left[V_{GS} - V(x) - V_{TH}\right] \ , \tag{A.2}$$

where $V(x)$ is the voltage at the point x. I_D can be obtained from the above equation considering that the current is given by:

$$I_D = Q_d \cdot \mu E, \tag{A.3}$$

where μ is the charge carrier mobility and E the electric field. Since $E(x) = -dV/dx$ and $V(x)$ varies from zero at $x = 0$ to V_{DS} at $x = L$, it can be shown [105] that

$$I_D = \mu C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right] \ . \tag{A.4}$$

It is used to call $V_{GS} - V_{TH}$ of saturation voltage (V_{SAT}). For relative small drain-source voltages ($V_{DS} \leq V_{SAT}$) the channel behavior is ohmic and the device is said to operate in the linear (or triode) region.

IF V_{DS} exceeds V_{SAT} ($V_{DS} > V_{SAT}$) I_D becomes relatively constant and the device is said to operate in saturation region. From Equation A.2, when $V(x)$

approaches to V_{SAT} $Q_d(x)$ drops to zero. That is, when V_{DS} is slightly greater than V_{SAT}, the depletion layer stops in $x \leq L$ and the channel is said to be pinched-off. As V_{DS} increases further the point at which $Q_d = 0$ gradually moves toward the source. In analog circuits MOS transistors are most often operating in saturation region and in this case they can be used as a current source.

The analysis presented in this section entailed various simplifying assumptions. Some of these assumptions are not valid in many analog circuits. Second-order effects as mobility degradation, channel length modulation and body effect should be considered for a better description of MOS devices.

A.2.2 Large Signal Models

The large signal model describes the MOS transistor behavior for all bias conditions, depending on V_{GS} and V_{DS}. In this case, three modes of operation can be distinguished: cutoff ($V_{GS} < V_{TH}$), ohmic region ($V_{GS} > V_{TH}$) and saturation region ($V_{DS} > V_{Sat}$). These are DC conditions that where already described in the previous section. The drain current for these conditions is given by:

$$I_D = \{ \begin{array}{ll} \approx 0 & V_{GS} < V_{th} \\ K\left[(V_{GS} - V_{TH})V_{DS} - V_{DS}^2/2\right] & V_{GS} > V_{th},\ V_{DS} < V_{Sat} \\ K(V_{GS} - V_{TH})^2 & V_{GS} > V_{th},\ V_{DS} > V_{Sat} \end{array}, \tag{A.5}$$

where $K = \mu C_{ox} W/L$.

A.2.3 Small Signal Models

The quadratic characteristics described above proves the DC condition of a transistor. If a perturbation in the bias conditions is small, an approximation of the large signal model around the operating points can be employed to simplify the calculations. Since I_D is a function of V_{GS}, a voltage dependent current source can be incorporated. That is, the transistor can be characterized as a voltage controlled current source equal to $g_m V_{GS}$.

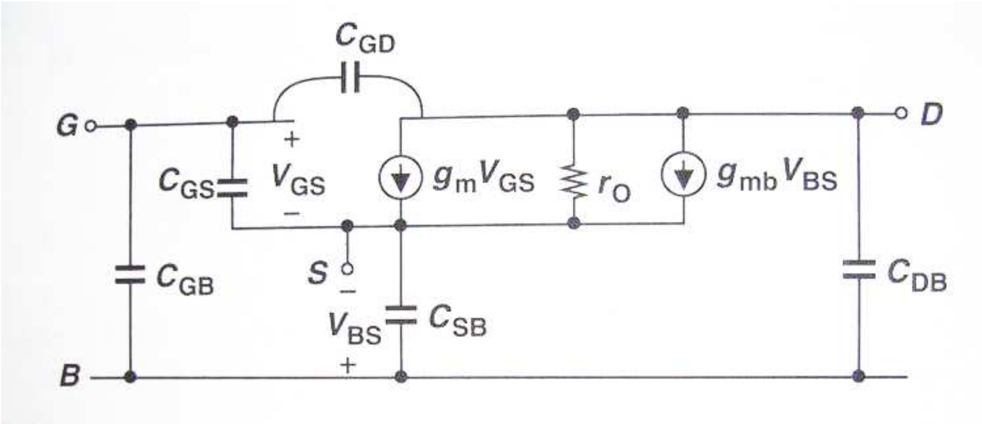


Figure A.6: MOS small signal model.

The drain current also varies with V_{DS}, but the variation is linear and is equivalent to a linear resistor r_O. This output resistance, given by $r_O = \partial V_{DS}/\partial I_D$, influences the performance of many analog circuits, for example limiting the maximum voltage gain of amplifiers.

Besides the gate, the bulk potential influences the threshold voltage and hence the gate source over drive. With all terminals at constant voltage, I_D is a function of the bulk voltage, i.e., the bulk behaves as a second current source equal to $g_{mb}V_{bs}$. The bulk transconductance g_{mb} is ten times smaller than transistor transconductance g_m. Figure A.6 shows a MOS transistor small-signal model. Capacitances can be extracted from physical location of the terminals, although they are not described in this section.

A.2.4 Noise Behaviour

The main MOS noise sources are the channel thermal noise (white noise) which arises from the channel resistance and the 1/f noise. The gate and bulk resistance noise are of minor importance, because they can be kept small by proper layout.

The channel thermal noise is generated by the random motion of the carriers in the channel. For devices in saturation it can be expressed [119] as a drain current power spectral density as

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\gamma(g_m + g_{mb}) \tag{A.6}$$

where k is the Boltzmann constant, T the absolute temperature, Δf the frequency variation and g_m and g_{mb} the gate and bulk transconductance, respectively. γ is a constant that varies from 1/2 to 2/3 from weak to strong inversion for an ideal device. Dividing by g_m^2 we obtain the input noise power spectral density

$$\frac{\overline{v_{ch}^2}}{\Delta f} = 4kT\gamma\frac{g_m + g_{mb}}{g_m}\frac{1}{g_m} = 4kTn\gamma\frac{1}{g_m} \ . \tag{A.7}$$

The flicker noise (1/f noise) is due to random trapping and de-trapping of mobile carriers at the Si-SiO_2 interface and within the gate oxide. Its input power spectral density is given by

$$\frac{\overline{v_{1/f}^2}}{\Delta f} = \frac{K_a}{C_{ox}^2 WL}\frac{1}{f^\alpha} \tag{A.8}$$

where α is a parameter close to 1 and K_a is a technology dependent parameter which expresses the process noise characteristics.

The bulk and gate resistance thermal noise are introduced by the substrate resistance R_B and the gate resistance R_G, respectively. Both thermal noise can be expressed as

$$\frac{\overline{v_{RB}^2}}{\Delta f} = 4kTR_B\frac{g_{mb}^2}{g_m^2} \quad \text{and} \quad \frac{\overline{v_{RG}^2}}{\Delta f} = 4kTR_G \ . \tag{A.9}$$

The total noise power spectral density is then written as

$$\frac{\overline{v_{in}^2}}{\Delta f} = 4kTn\gamma\frac{1}{g_m} + \frac{K_a}{C_{ox}^2 WL}\frac{1}{f^\alpha} + 4kTR_B\frac{g_{mb}^2}{g_m^2} + 4kTR_G \ . \tag{A.10}$$

A.3 Technology Scaling

The downsizing of MOS devices is the technology answer for the need of high performance circuits, with higher integration. Lowering the supply voltage is the most effective way to reduce the power consumption. However the transistor drain current decreases with the reduction of supply voltage and therefore the circuit speed. A solution to increase the transistor drain current under low voltage is to miniaturize the device, which also reduces the capacitances of devices and connections. The design of MOS transistors in every new generation[2] uses the scaling method proposed by R. Dennard [120].

Indications on the future trends can be found in [121]. Figure A.7 shows the technology features scaling foreseen up to the year 2014. It is shown that in the year 2014 transistors will use a supply voltage of 0.3 V and will have gate length of 35 nm. By this time it should be possible to have a chip with more than 4 billion transistors, operating at a frequency above 2 GHz.

A.4 Ionizing Radiation Effects on MOS Devices

There are three primary types of radiation effects: total dose, displacement and single event effects (SEE). The nature of damage created by these effects are different and the impact depends on the device type.

Total dose effects depend on the total ionizing energy absorbed by the material and they result from the interaction of ionizing radiation with device materials, generating charges and changing the device properties. Displacement damage effects result from the atom displacement from their normal sites in a crystal lattice or material structure due to the interaction of energetic particles (non ionizing energy loss). These effects depend on the total fluence of incident particles and the particle type and energy. Single event effects result from the interaction of a single energetic particle passing through a device. These effects are associated with the high density charged track created by the particle and depend on the particle type and energy.

[2] CMOS generation in named by the minimum MOS transistor channel length. For example, technologies that have a minimum $L = 0.25\,\mu$m belong to the $0.25\,\mu$m generation.

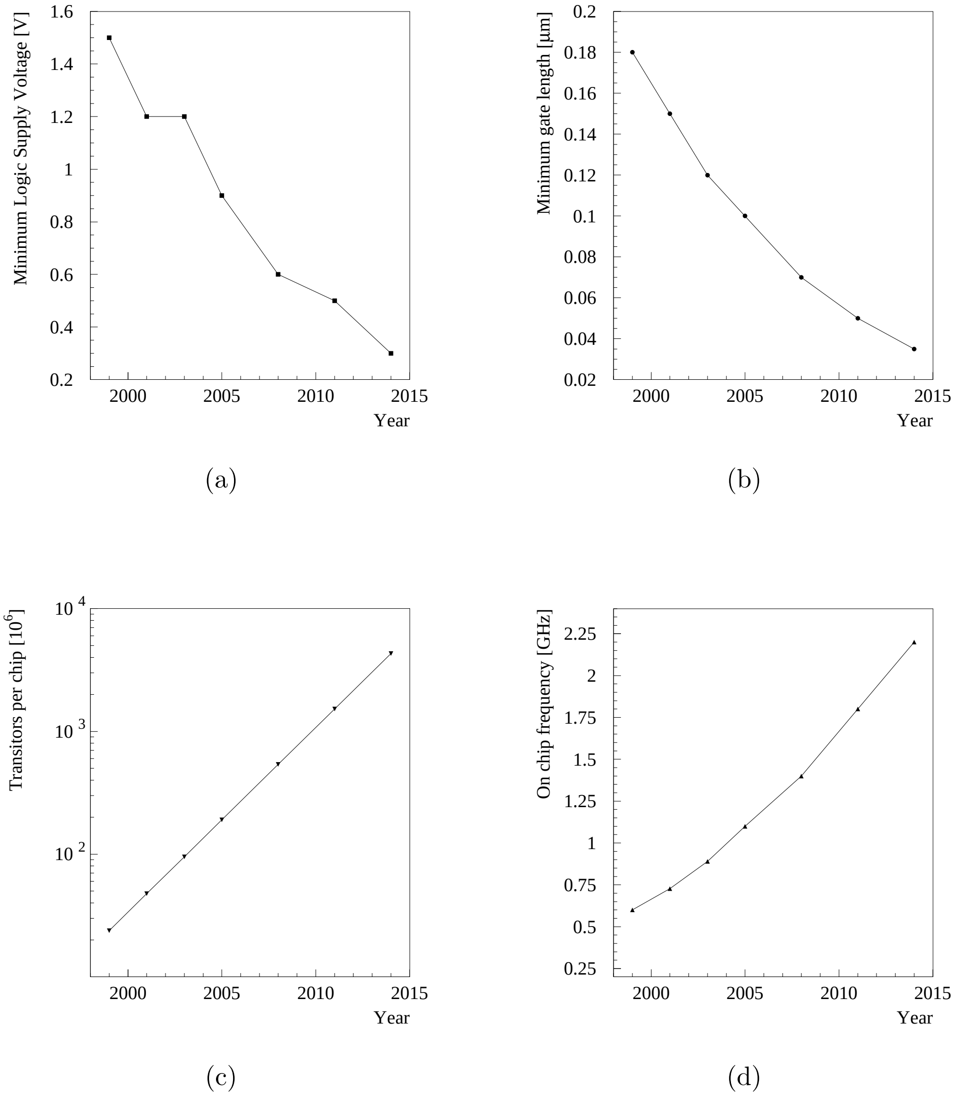


Figure A.7: Technology trends foreseen up to the year 2014. (a) shows the circuit power supply, (b) the transistor gate length, (c) the number of transistors per chip and (d) the chip frequency.

Devices whose characteristics depend on the surface effects, as MOS transistors, are more sensitive to total dose effects than displacement effects, because of the high doping concentration. On the other hand, devices that depend on the bulk conduction, such as silicon particle detectors and optoelectronic devices, are more sensitive to displacement damage. Both surface and bulk devices are affected by SEE, that can create current and voltage transients.

A.5 MOS Fabrication

Many limitations imposed on the circuit performance are related to fabrication issues. Modern CMOS technologies involve more than 200 processing steps, that can be summarized as a combination of the following operations: (1) wafer processing to produce the proper type of substrate; (2) photolithography to precisely define each region; (3) oxidation, deposition and ion implantation to add materials to the wafer and (4) etching to remove materials from the wafer.

The wafer in a CMOS technology must grown as a single-crystal silicon body having small number of defects, being of very high quality. In addition the wafer must contain the proper type and level of doping to achieve the required resistivity. To build the wafers a seed of crystalline silicon is immersed in molten silicon, already with dopants to obtain the desired resistivity, and gradually pulled out while rotating. As a result, a large cylindrical single-crystal is formed and can be sliced thin into wafers. The wafers are then polished and chemically etched to remove damages on the surface that are created during slicing. The wafers have a diameter of about 20 cm and a thickness of approximately 500 to 1000 μm.

Photolithography is the first step to transfer the circuit layout information to the wafer. The layout consists of geometries representing different types of layers. Each layout layer is written to a transparent glass mask via a precisely controlled electron beam. A think layer of oxide is grown to protect the wafer surface and

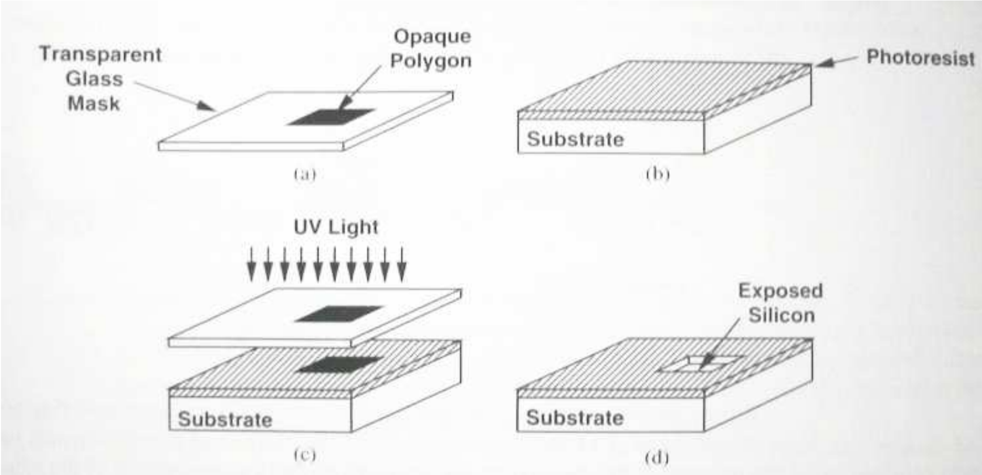


Figure A.8: (a) Glass mask used in photolithography, (b) coverage of wafer by photoresist, (c) selective exposure of photoresist to UV light and (d) exposed silicon after etching.

then the wafer is covered by a thin layer of photoresist[3]. After that, the mask is placed on top of the wafer and the pattern is projected by ultraviolet light (UV). The photoresist becomes harder in the regions exposed to the light and softer under the pattern. The wafer is then placed in an etchant that dissolves the soft area, exposing the silicon surface. This procedure, illustrated in Figure A.8, is repeated to each layer in the circuit.

Silicon dioxide is grown by placing the exposed silicon (resulted from the photolithography) in an oxidizing atmosphere such as oxygen at a temperature around 1000 °C. This is a very critical step in the process, since the oxide thickness determines both current handling and reliability of the transistors, and it has to be controlled to within few percent. For example, the oxide thickness of two transistors in the wafer must differ by less than few angstroms.

In many steps of fabrication dopants must be introduced into the wafer. A common method is the ion implantation, where the doping atoms are accelerated

[3]Photoresist is a material whose etching properties change upon exposure to light.

as a high energy focused beam, hitting the wafer surface and penetrating the exposed areas. The doping dosage is determined by the intensity and duration of the implantation. The depth of the doped region is set by the energy of the beam. Since this implantation damages the silicon lattice, the wafer is subsequently heated to about 1000 °C for 15 to 30 minutes.

The polysilicon in the dielectric layers is then formed by chemical vapor deposition. The wafers are placed in a furnace filled with a gas that creates the desired material trough a chemical reaction. The etching of the materials is an important step to guarantee the precision. This can be done in different ways: (1) wet etching, i.e., place the wafer in a chemical liquid (low precision); (2) plasma etching, i.e., bombard the wafer with a plasma gas (high precision) and (3) reactive etching, where ions produced in a gas bombard the wafer.

A.5.1 Active Devices Fabrication

Device fabrication starts with a p-type silicon wafer. After cleaning, polishing and dioxide deposition (Figure A.9(a)), n-wells are created by a photolithography sequence, consisting of photoresist deposition, exposure to UV light and selective etching (Figure A.9(b)). The remaining photoresist and oxide layers are then removed (Figure A.9(c)). This sequence is repeated to create a channel-stop implant between the transistors (Figure A.9(d)). The photoresist is removed and a thick oxide layer is grown in the exposed silicon areas, producing the field oxide (Figure A.9(e)). Then, a gate oxide is grown, followed by a threshold adjust implant (Figure A.9(f)). The threshold adjust is performed creating a thin sheet of dopants near the surface, making the transistor threshold more positive.

With the gate oxide in place, the polysilicon layer is deposited resulting in the structure shown in Figure A.9(g). The source and drain junctions are then formed by ion implantation, which requires a source/drain mask and two photolithography sequences. First, as illustrated in Figure A.9(h), a negative photoresist is performed exposing the areas to receive a n^+ implant. After, a positive photoresist is used (Figure A.9(i)). The device gate is made before the source and drain terminals to create a self aligned structure, because the source/drain regions are implanted precisely at the edges of the gate area. Once the transistors are fabricated, the electrical connections on the chip through contacts and wires are made.

A.5.2 Passive Devices in MOS Integrated Circuits

Since CMOS process target primarily digital applications, passive components such as resistors and capacitors do not have high quality. The variability of the component value from wafer to wafer can be of $\pm 20\,\%$, what is considered a high value for analog design.

A common method to create resistors is to interrupt the silicide layer that is deposited on top of the polysilicon, creating a region with the resistivity of the polysilicon. The use of silicide on the two ends of the resistor lower the contact resistance, but improves both the resistor value definition and the matching with identical structures. Resistors can also be created using sliced polysilicon, p^+ or n^+ active areas, n-well and metal layers. These types of resistors are rarely used in analog designs because their resistivity varies by $\pm 50\,\%$. In $0.25\,\mu$m CMOS technology the poly resistors, made with polysilicon and $p+$ diffusion, have a square resistivity of $210 \pm 20\,\%\,\Omega$ per square.

Linear capacitors can be fabricated as poly-diffusion, poly-poly, metal-poly or metal-metal structures. The idea is to grow or deposit a thin oxide between two floating conductive layers, forming a dense capacitor with moderate bottom-plate parasitic. The metal-insulator-metal capacitor in the $0.25\,\mu$m CMOS technology has capacitance equal to $C \approx 0.69WL + 0.30(L + W)$, where L and W are capacitor length and width. Transistors can also be used as capacitors, but the value is not linear.

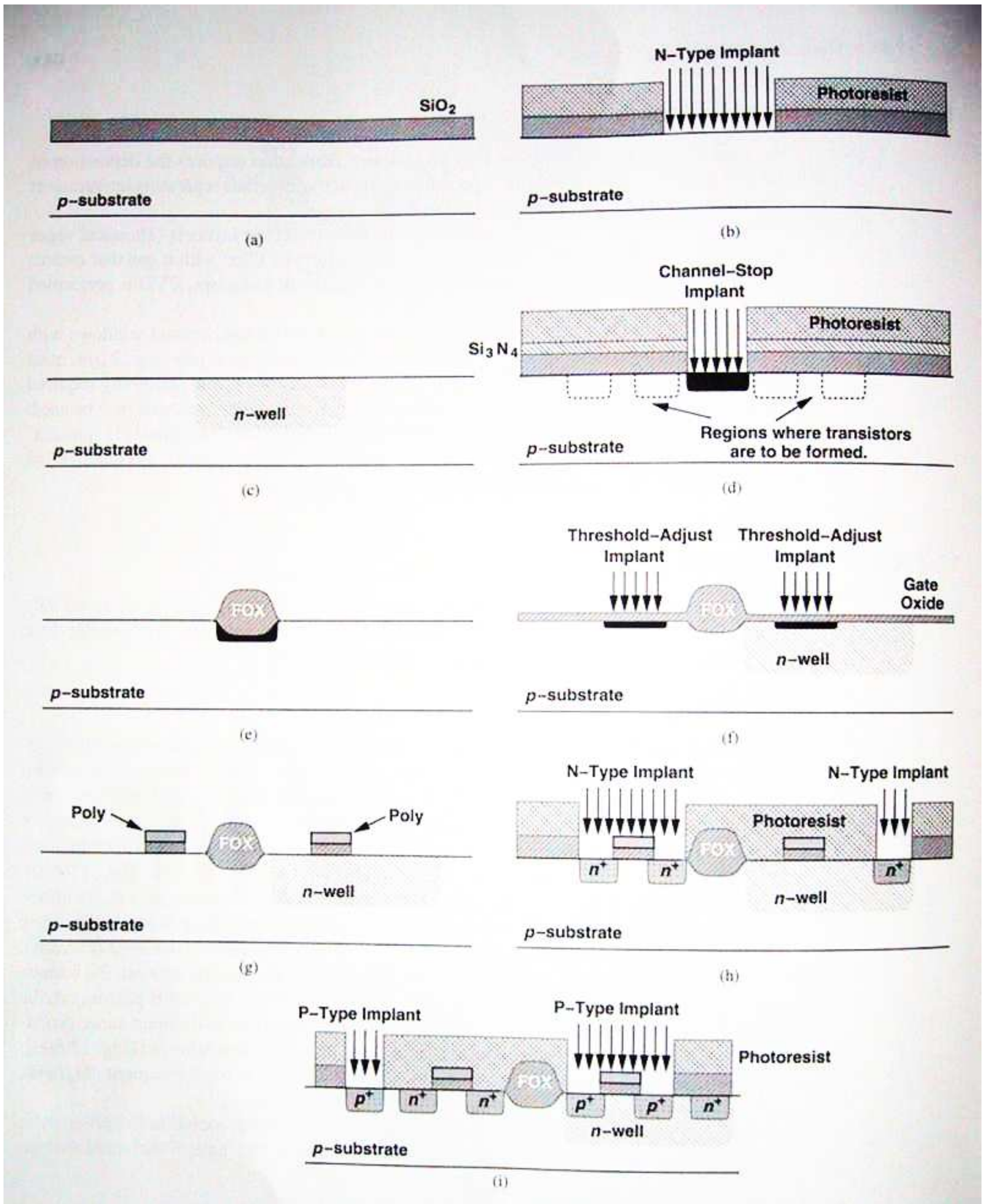


Figure A.9: Fabrication sequence of MOS devices.

A.6 CMOS Layout

The layout of MOS transistors is determined by both device electrical properties required in the circuit and the design rules imposed by the technology. The design rules are strictly dependent on the used technology and the manufacture. For example, widths and lengths of the geometries in the layout must exceed a minimum value imposed by both photolithography and technology process capabilities. If a polysilicon rectangle is more narrow than the rule, it may break or suffer from a large local resistance. In general, the thicker a layer, the greater its minimum allowed width that decreases proportionally as the technology scales. For the $0.25\,\mu$m technology, the minimum width of a polysilicon and a metal layer is $0.25\,\mu$m and $0.5\,\mu$m for a thickness of $0.2\,\mu$m and $1.0\,\mu$m, respectively. In addition to that, a maximum allowable dimension is also required. The thickness of the layers is not controlled by layout designer.

Figure A.10 shows a MOS device. The gate polysilicon and the source and drain terminals are tied to metal (aluminum) wires that serves as interconnects with low resistance and capacitance. Contact windows must be opened in each region, filled with metal and connected to the upper metal wires. The source and drain junctions play an important role in the transistor performance and to minimize the capacitance of both S and D, the total area has to be minimized.

One important effect that should be considered in the circuit design is the antenna effect. This effect is seen when a large area of a metal interconnects with a transistor gate. During the etching of the metal layer, the metal area acts as an antenna collecting ions and rising in potential. Therefore, the gate voltage of the transistor increases so much that the gate oxide breaks down during the fabrication.

In general, the design rules aim to maximize the yield of digital integrated circuits. Analog systems demand many more layout precautions to minimize effects as crosstalk, devices mismatching, noise and etc [105].

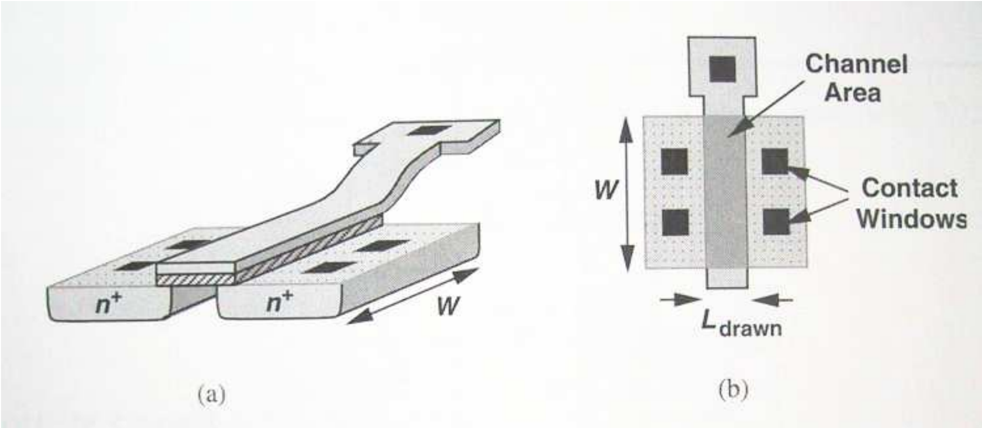


Figure A.10: MOS device views.

A.6.1 Radiation Tolerance Techniques

Radiation tolerance techniques can be used in the transistor layout. By using enclosed geometries and guard rings in the layout of nmos devices the radiation leakage paths along the devices are eliminated [108]. Source-to-drain leakage can be avoided by forcing all source-to-drain current to run under the gate oxide by using a closed gate. These enclosed devices have a minimum width and length, that limit the design flexibility. Detailed description on these techniques can be found in [122].

A.7 Packaging

After fabrication and dicing, most of integrated circuits are packaged. The parasitics associated with the package and connections to the chip introduce difficulties in the evaluation of the actual circuit performance. When a die is mounted in the center cavity of a package and bonded to the pads on the perimeter of the cavity, this structure exhibits the following parasitics: bond wire and trace self-inductance, trace-to-ground and trace-to-trace capacitance and trace-to-trace mutual inductance. Thus, the connection from the circuit and the chip itself is far to be ideal. The speed and accuracy of integrated circuits have increased, but the performance of packages has not improve significantly. Some of the package limitations originates from cost of assembly and mechanical stress, as diameter of bond wires, width and spacing of package pins and width and spacing of the traces in printed circuit boards. For example, each bond wire and its corresponding package trace has a finite self-inductance between 2 nH and 20 nH.

A self-inductance can also be find in the connection to the substrate. That is why some packages contain a metal ground plane to which the die can be attached by conductive epoxy. This plane ends in several package pins tied to the board ground. The effect of self-inductance has also to be considered for input signals, because it forms a low-pass filter attenuating high-frequency components and/or creating ringing in the transient waveform.

In the past 20 years the package dimensions have scaled by less than a factor five, while the speed of many circuits has increased by two orders of magnitude. That is why package parasitics have to be taken into account in the design of integrated circuits.

A.8 PSPICE CMOS Transistor Models

A.8.1 NMOS Transistor

.MODEL NCH NMOS

VERSION=3.1 TOX=+5.84000000E-09 CDSC=0.001427297

CDSCB=0.001256353 CDSCD=0.0002944723 CIT=0 NFACTOR=1.16

XJ=6.163775E-08 VSAT=92300.0 AT=42933.03 A0=0.85553

AGS=0.4315134 A1=0 A2=1 KETA=-3.57129400E-03 NCH=4.588901E+17

NGATE=7.82E19 K1=0.7084805 KT1=-2.47794200E-01 KT1L=1.274724E-09

KT2=-3.85961500E-02 K2=0.01542675

K3=-3.05671300E+00 K3B=2.216323

W0=1.427888E-08 NLX=1E-10 DVT0=1.696754 DVT1=1.181057

DVT2=-8.43515400E-01 DVT0W=-3.04192400E+00 DVT1W=2825243

DVT2W=-3.29162200E-02 DROUT=0.03821881 DSUB=1.809158

VTH0=+6.35800000E-01 UA=7.56534E-11 UA1=5.731119E-09

UB=3.018613E-18 UB1=-7.39994300E-18 UC=3.329672E-10

UC1=-4.41010500E-11 U0=+5.17980100E+02 UTE=-1.02712500E+00

VOFF=-1.43435600E-01 DELTA=0.005387002 RDSW=+6.67390400E+01

PRWG=0.03643927 PRWB=0.5073748 PRT=-6.00000000E+01

ETA0=1.610939

ETAB=-6.60586500E-01 PCLM=3.282407 PDIBLC1=0.01466331

PDIBLC2=-2.78763800E-02 PDIBLCB=-5.14816800E-01

PSCBE1=4.904991E+09 PSCBE2=0.06982773 PVAG=0.7346723

WR=1.03535 DWG=-2.49992000E-08 DWB=8.428967E-09

B0=1.129173E-06 B1=2.697167E-06 ALPHA0=0 BETA0=30

CGSL=+3.45700000E-10 CGDL=+3.45700000E-10 CKAPPA=10.0 CF=0

DWC=-1.84000000E-08 DLC=+4.91000000E-08 LRDSW=24.18693

WUC=-4.46019600E-11 PUA=9.246951E-13 PUC=3.887136E-12

PU0=2.406341 TNOM=25 CGSO=+1.43000000E-11

CGDO=+1.43000000E-11 CGBO=3.204E-11 XPART=0

LINT=+3.00000000E-08 LL=1.911841E-15 WINT=+3.65000000E-08

WL=-1.08000000E-15 WW=1.728073E-16 AF=1.0 KF=+3.00000000E-24

ACM=3 HDIF=+3.80000000E-07 JSW=+2.20000000E-13

CJ=+1.40000000E-03 CJSW=+1.21000000E-10 JS=+4.70000000E-08

MJ=+5.73000000E-01 MJSW=+2.51000000E-01 PB=+9.84000000E-01

PHP=+2.63000000E-01 PTA=+1.99000000E-03 PTP=+8.00000000E-04

CJGATE=+3.20000000E-10 CTA=+1.36000000E-03

CTP=+2.95000000E-03 RSH=+4.00000000E+00

TLEV=+1.00000000E+00 TLEVC=+1.00000000E+00

A.8.2 PMOS Transistor

```
.MODEL PCH PMOS
    VERSION=3.1 TOX=+5.65000000E-09 CDSC=1E-3
    CDSCB=-4.36889000E-04 CDSCD=0 CIT=0 NFACTOR=1.61
    XJ=1.5E-7 VSAT=1.155625E5 AT=100 A0=1.3671683
    AGS=0.2700338 A1=1.01222E-4 A2=0.996841 KETA=-4.50000000E-02
    NCH=4.06263E17 NGATE=5.826E19 K1=0.8766456
    KT1=-2.40580100E-01 KT1L=-4.81895700E-09
    KT2=-5.11666000E-02 K2=-1.58987300E-06
    K3=-3.65882060E+00 K3B=7.5313753
    W0=1.015553E-6 NLX=6.926899E-9 DVT0=3.3314102 DVT1=0.8928799
    DVT2=-2.25280100E-01 DVT0W=0 DVT1W=3.23001E6
    DVT2W=-5.00000000E-02 DROUT=1E-5 DSUB=0.8022905
    VTH0=-4.96200000E-01 UA=1.05077E-10 UA1=5.533021E-11
    UB=1.609702E-18 UB1=-2.20826000E-18 UC=-2.96859000E-11
    UC1=-5.68957000E-11 U0=+1.03800000E-02 UTE=-1.34685850E+00
    VOFF=-9.71750000E-02 DELTA=4.659862E-3 RDSW=+5.00000000E+02
    PRWB=-1.00000000E-03 PRT=450 ETA0=0.1552027
    ETAB=-8.66238000E-02 PCLM=0.9771133 PDIBLC1=1.805729E-3
    PDIBLC2=-1.78205300E-06 PDIBLCB=-5.03397600E-01
    PSCBE1=1.183635E8 PSCBE2=0.0 PVAG=0.047937
    WR=1 DWG=-2.85132000E-09 DWB=5.018987E-9
    B0=-3.89839100E-07 B1=3.714999E-6 ALPHA0=0 BETA0=30
    CGSL=+4.10000000E-10 CGDL=+4.10000000E-10
    CKAPPA=7.319055988 CF=0 DWC=-8.96700000E-09
    DLC=+4.88310000E-08 LKETA=-4.50000000E-03
    LK2=1.838183E-4 LK3B=1.7821951 LRDSW=42.7123941
    LETA0=0 LETAB=-2.80000000E-03 WKETA=-1.15399000E-02
```

WK2=-4.10960000E-03 PKETA=4.493883E-3 PK2=5.160467E-4

PVTH0=3.035167E-3 PUA=2.104599E-13 PUB=3.403636E-22

PUC=1.41059E-12 PU0=3.758094E-5 PVOFF=6.5E-3 PRDSW=0.3594897

PETA0=8.26943E-3 PETAB=2.430395E-3 TNOM=25

CGSO=+0.00000000E+00 CGDO=+0.00000000E+00 CGBO=3.204E-11

XPART=0 LINT=+3.00000000E-08 LL=0 LW=0 LWL=0

WINT=+2.05000000E-08 WL=2.64E-15 WW=4E-15 WWN=1 WWL=0

AF=1.15 KF=+1.00000000E-23 ACM=3 HDIF=+3.80000000E-07

JSW=+2.10000000E-14 CJ=+1.06090000E-03 CJSW=+8.81400000E-11

JS=+1.00000000E-07 MJ=+3.87630000E-01 MJSW=+4.10210000E-01

PB=+7.81710000E-01 PHP=+7.19160000E-01 PTA=+1.85200000E-03

PTP=+1.98850000E-03 CJGATE=+4.03190000E-10

CTA=+9.50210000E-04 CTP=+9.33830000E-04 RSH=+4.00000000E+00

TLEV=+1.00000000E+00 TLEVC=+1.00000000E+00

Appendix B

CARIOCA Sub-circuits Schematic

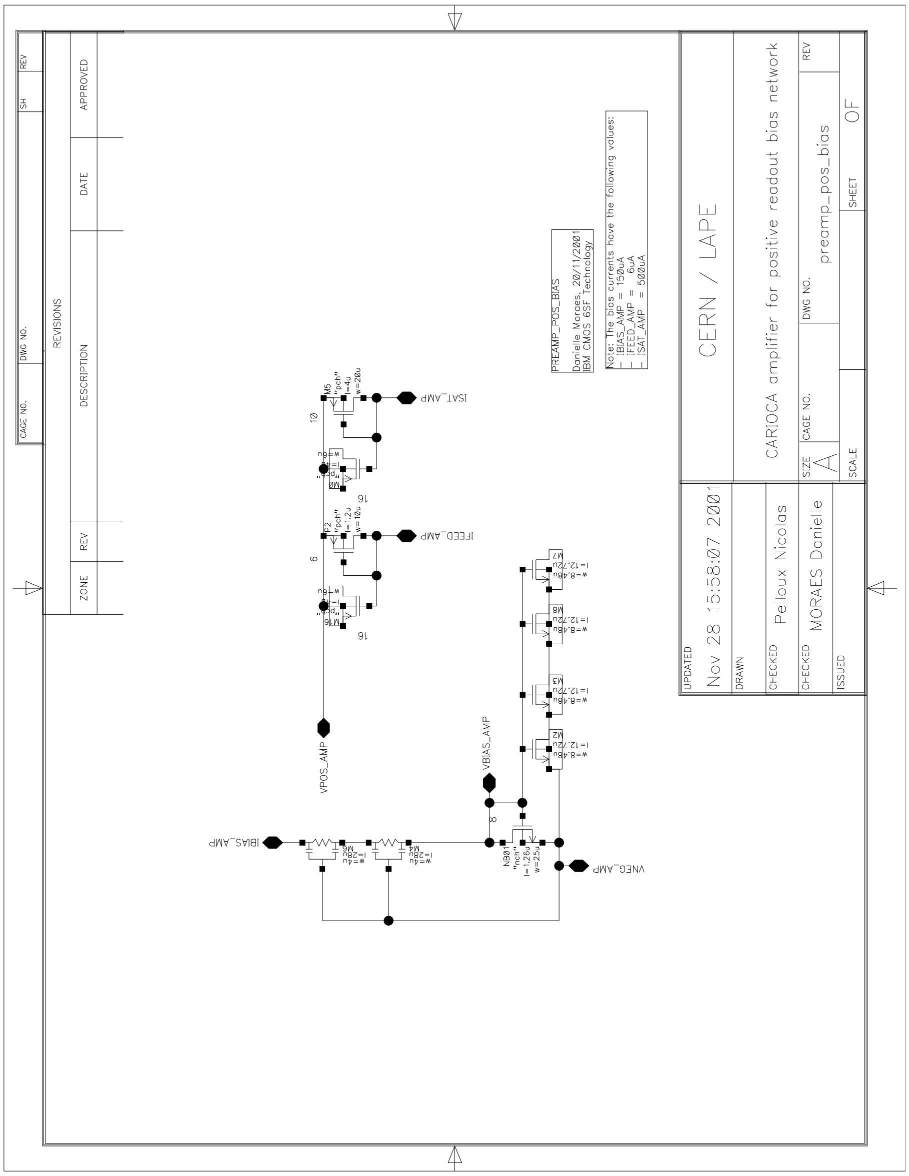


Figure B.1: Schematic of the CARIOCA positive input polarity amplifier bias network.

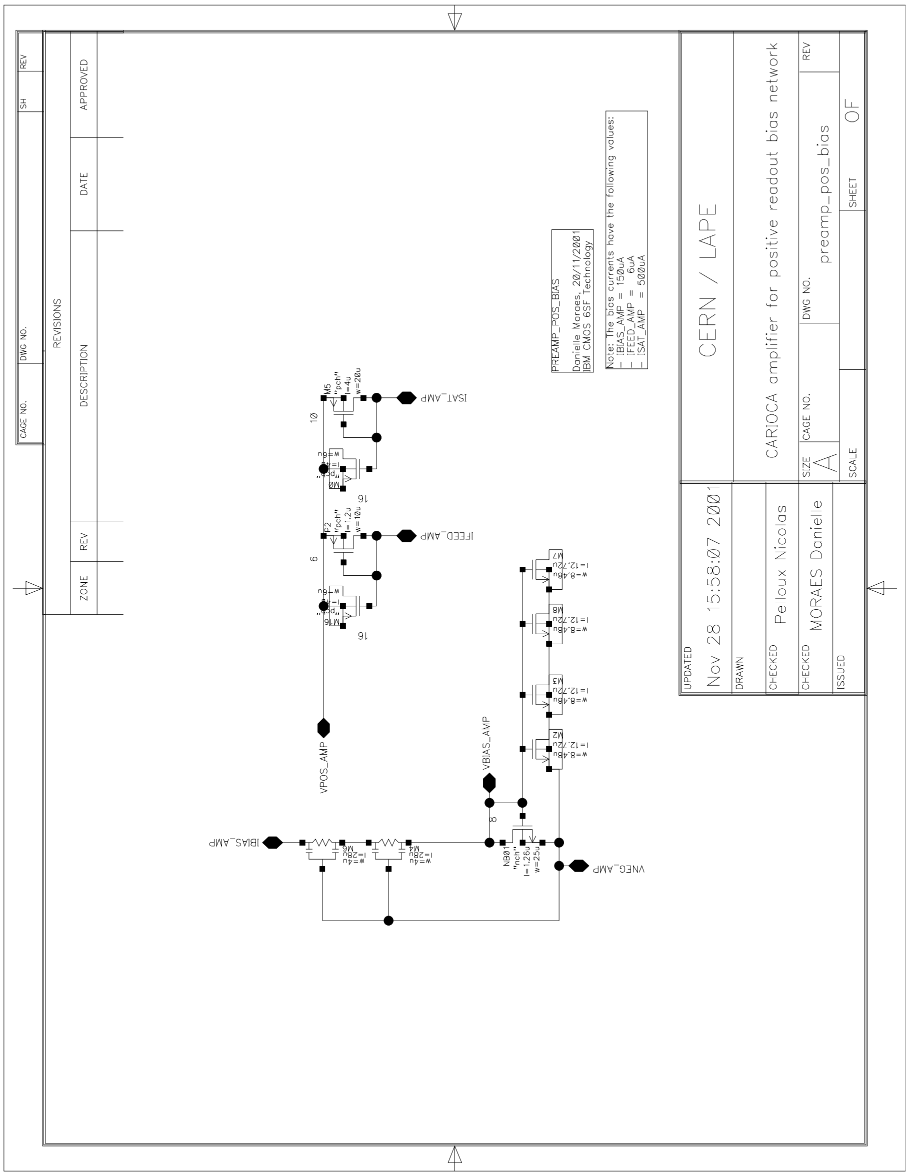


Figure B.2: Schematic of the CARIOCA positive input polarity amplifier bias network.

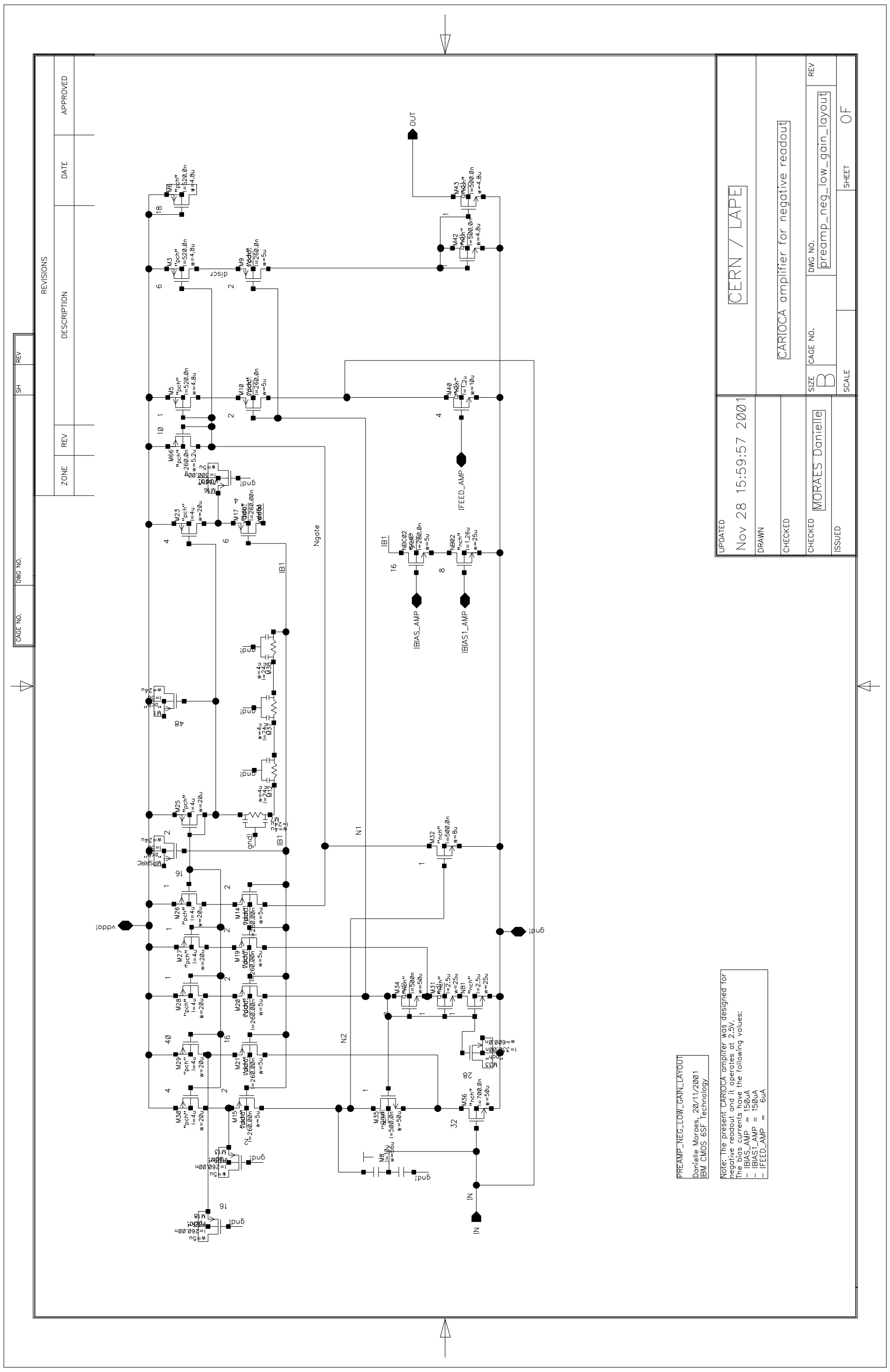


Figure B.3: Schematic of the CARIOCA negative input polarity amplifier.

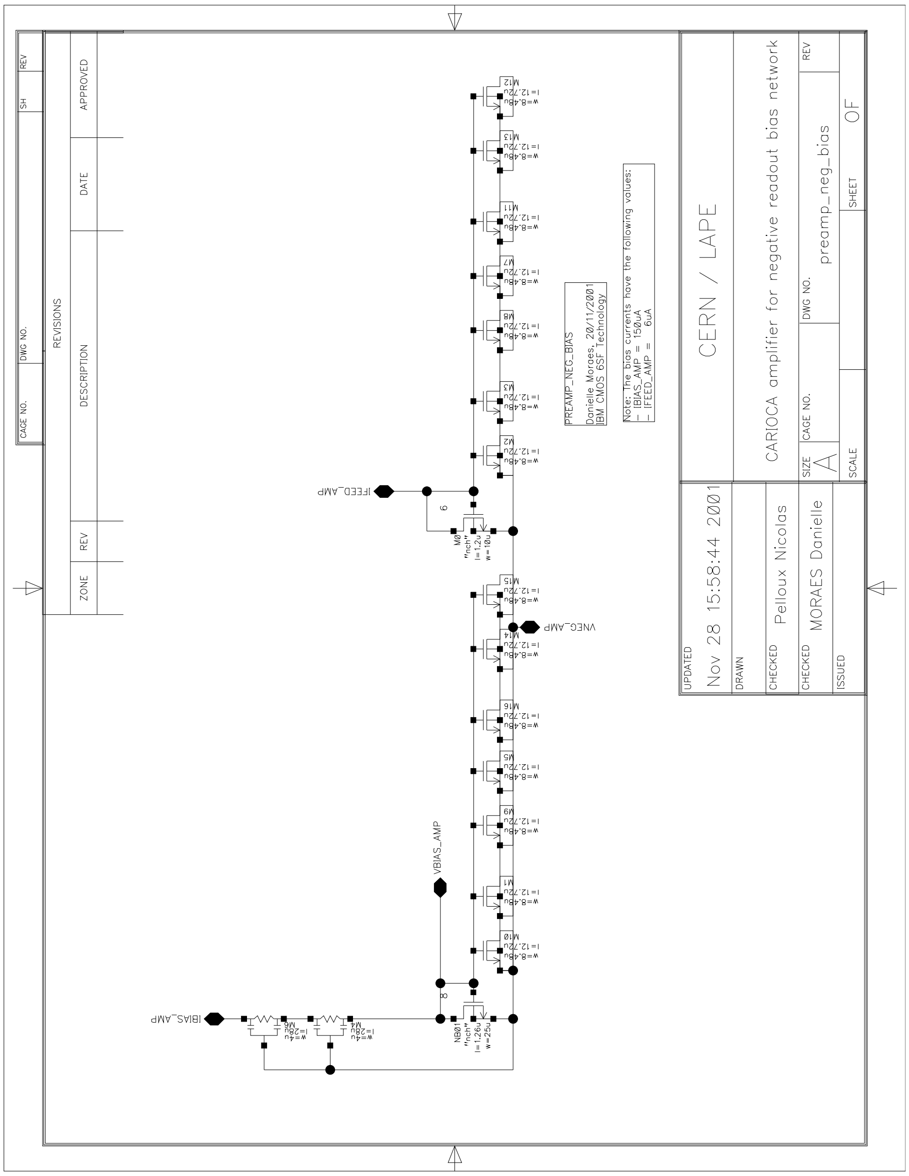


Figure B.4: Schematic of the CARIOCA negative input polarity amplifier bias network.

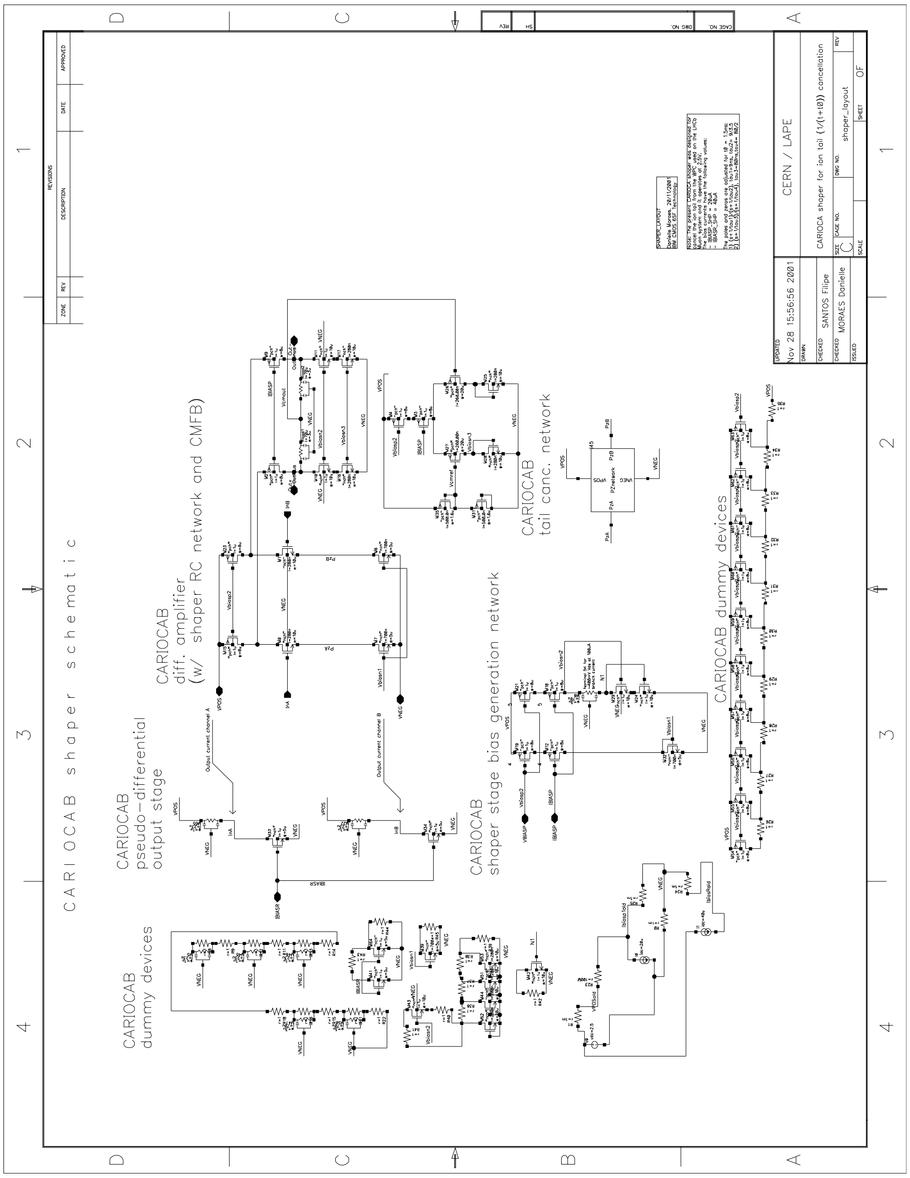


Figure B.5: Schematic of the CARIOCA shaper.

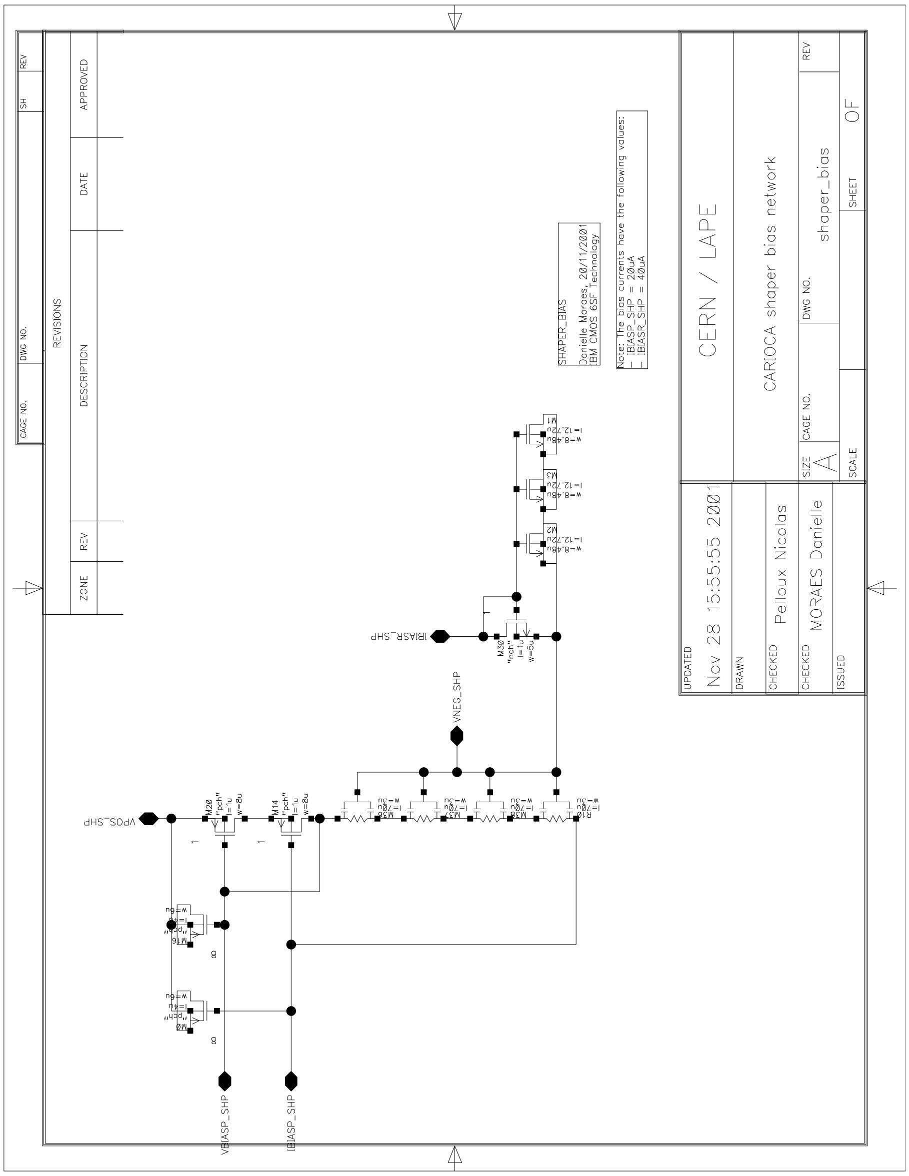


Figure B.6: Schematic of the CARIOCA shaper bias network.

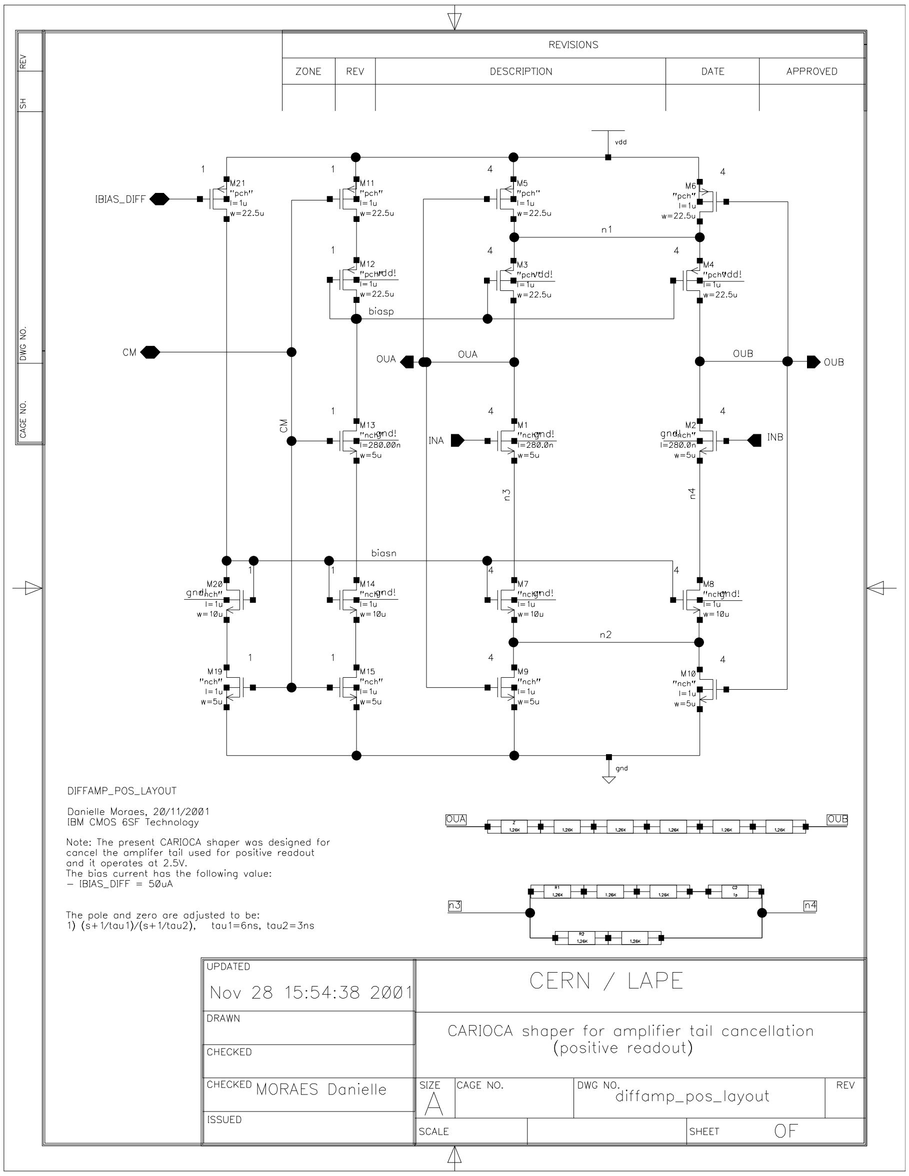


Figure B.7: Schematic of the positive polarity CARIOCA differential amplifier.

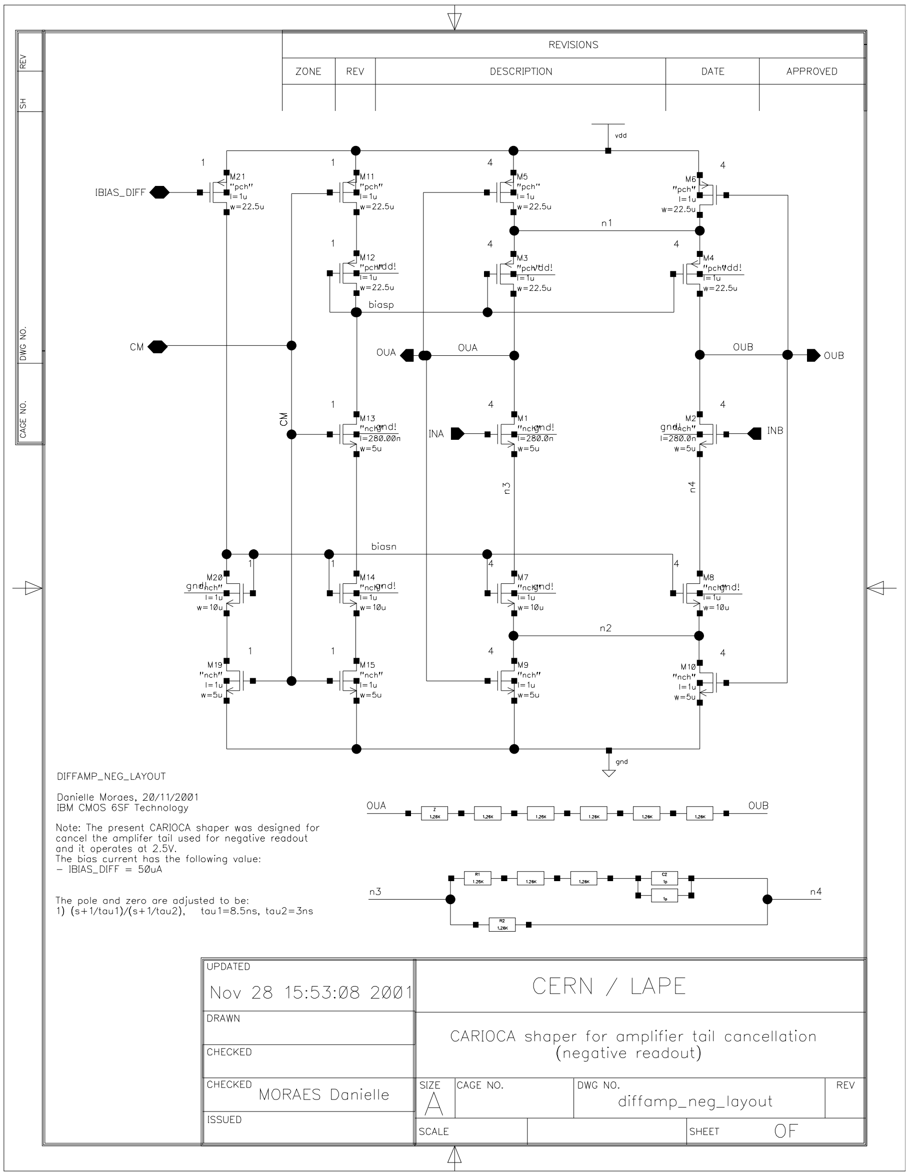


Figure B.8: Schematic of the negative polarity CARIOCA differential amplifier.

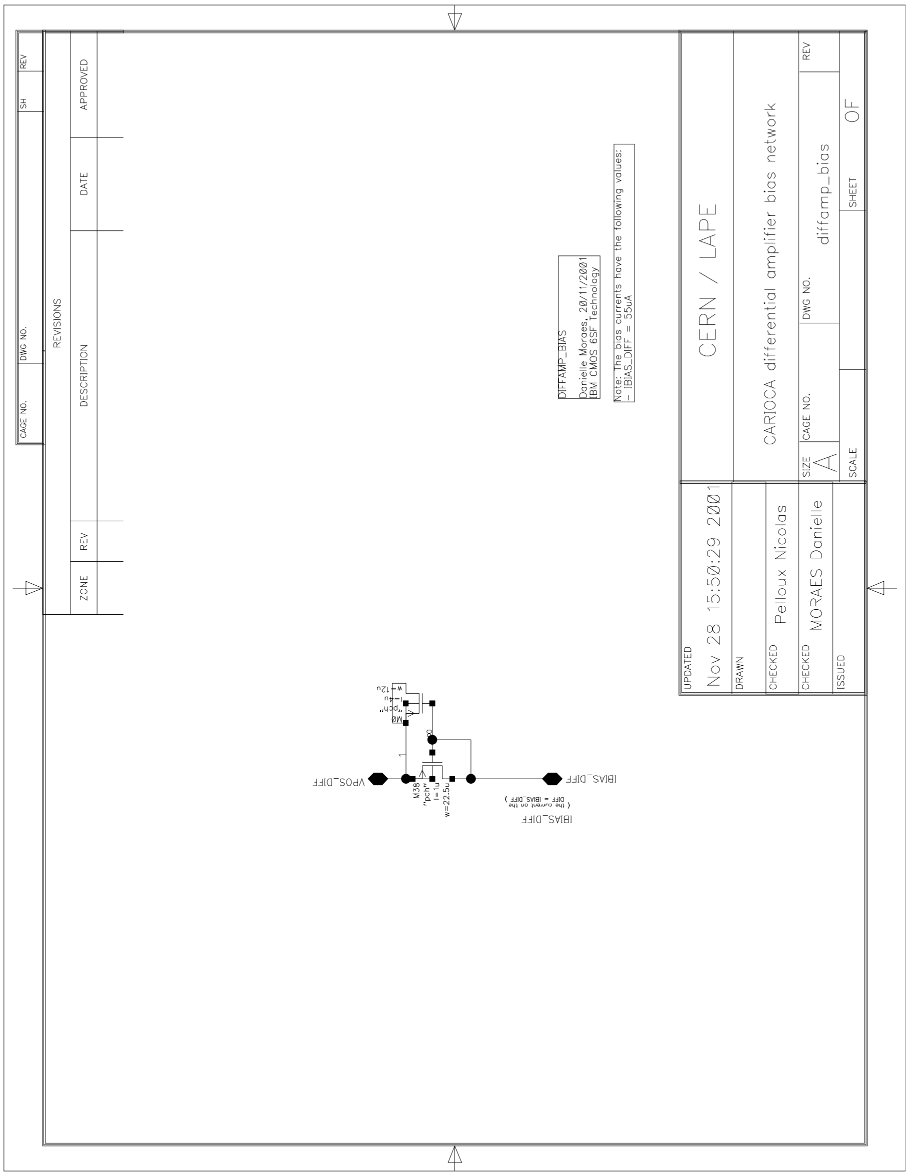


Figure B.9: Schematic of the CARIOCA differential amplifier bias network

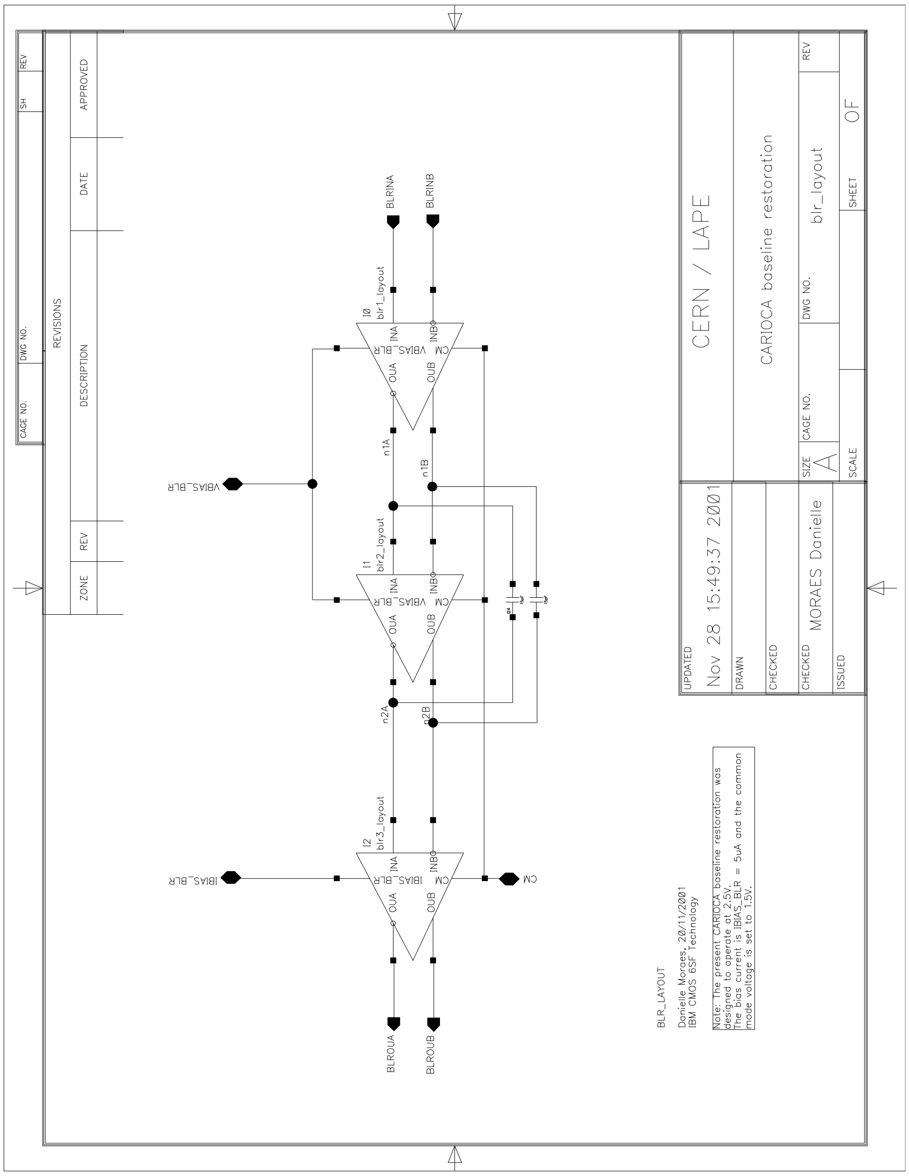


Figure B.10: Schematic of the CARIOCA baseline restoration.

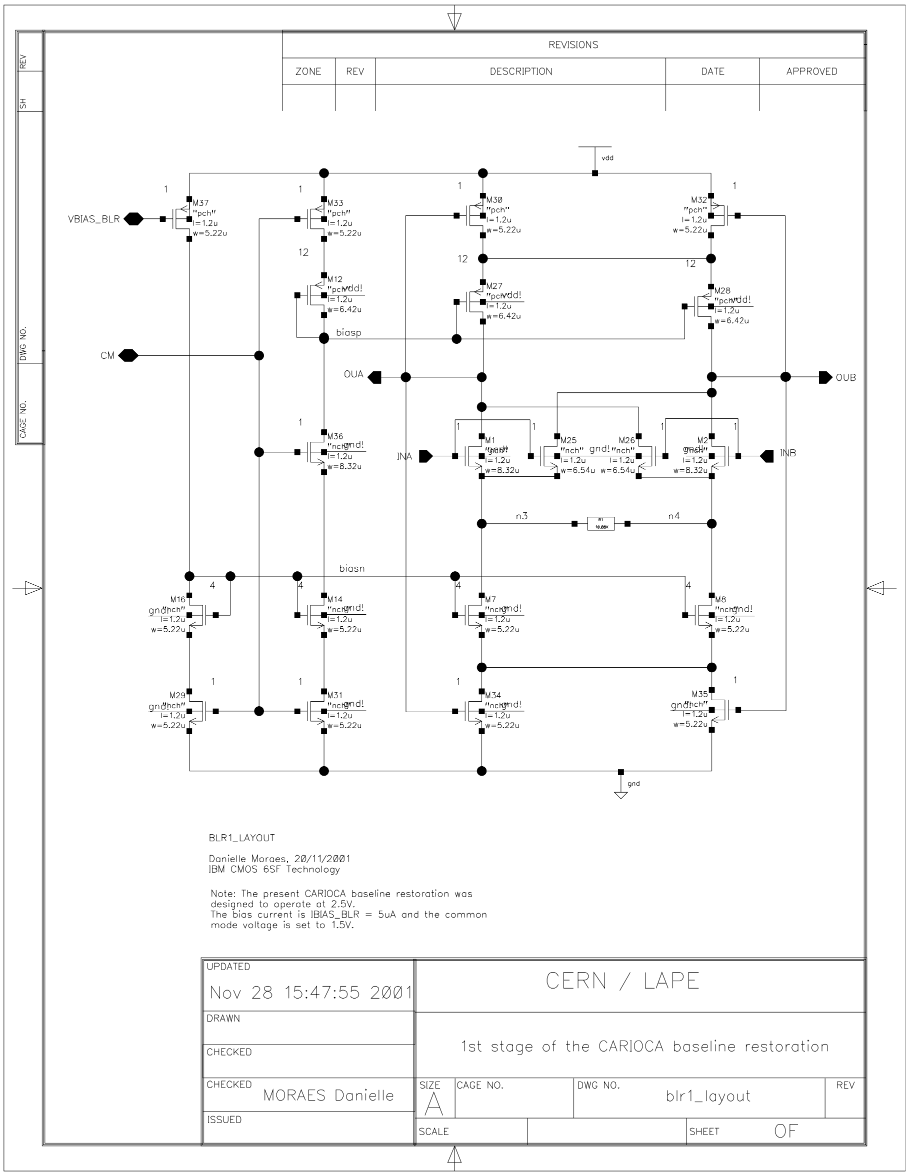


Figure B.11: Schematic of the first stage of the CARIOCA baseline restoration.

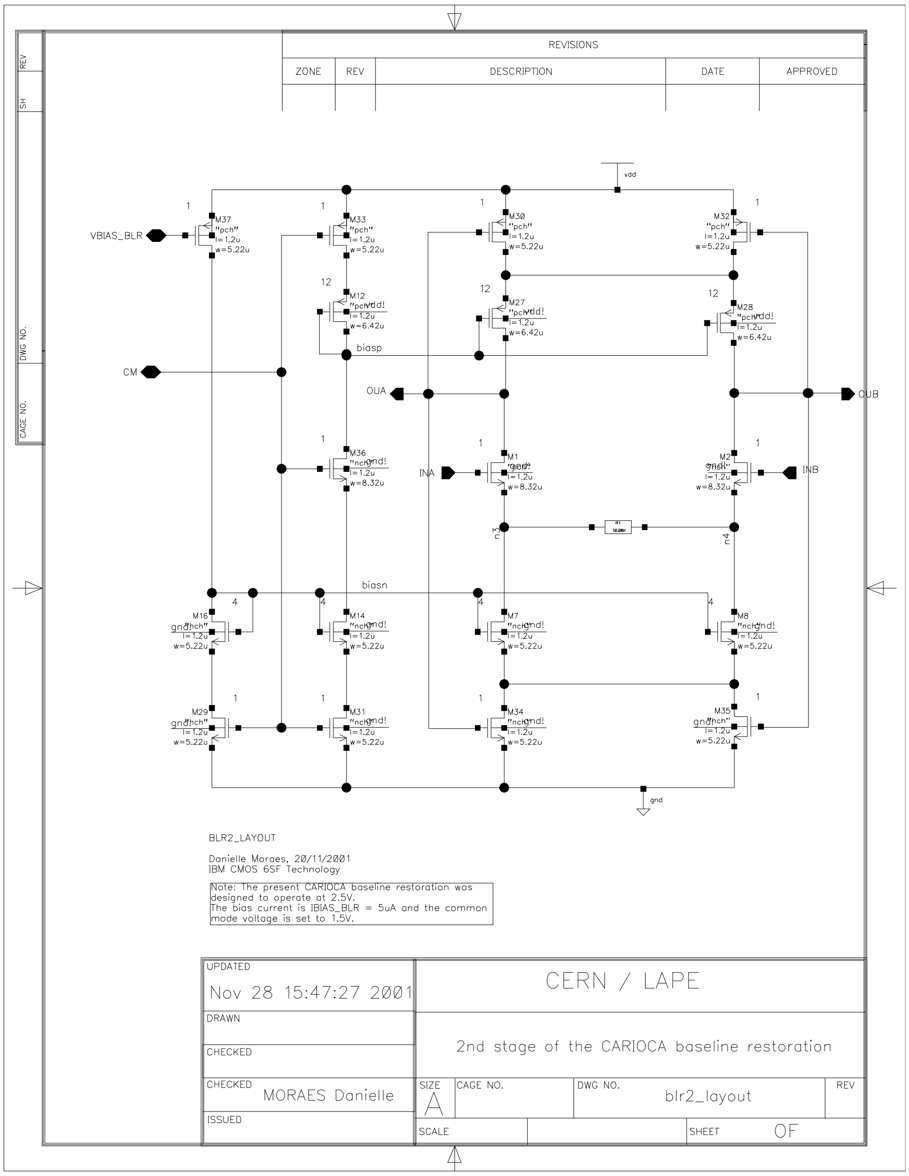


Figure B.12: Schematic of the second stage of the CARIOCA baseline restoration.

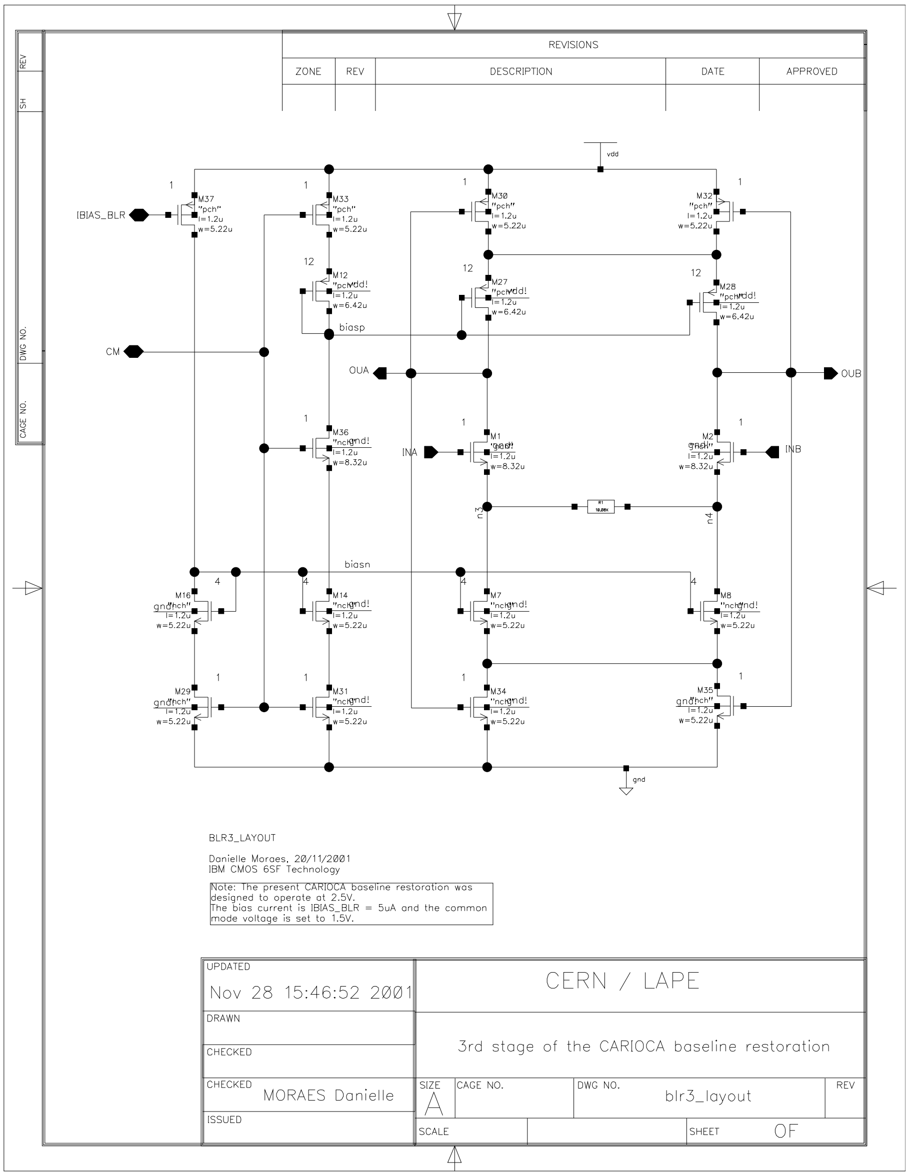


Figure B.13: Schematic of the third stage of the CARIOCA baseline restoration.

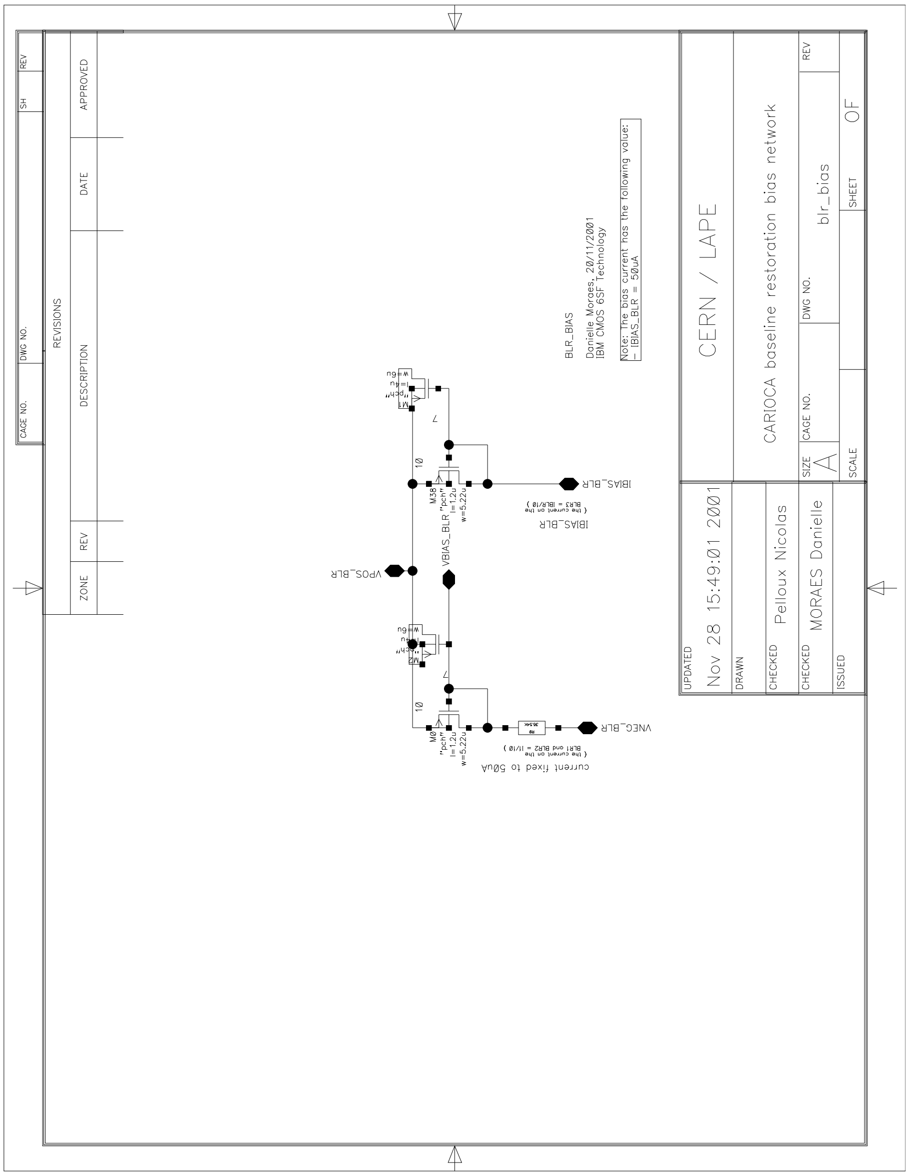


Figure B.14: Schematic of the CARIOCA baseline restoration bias network.

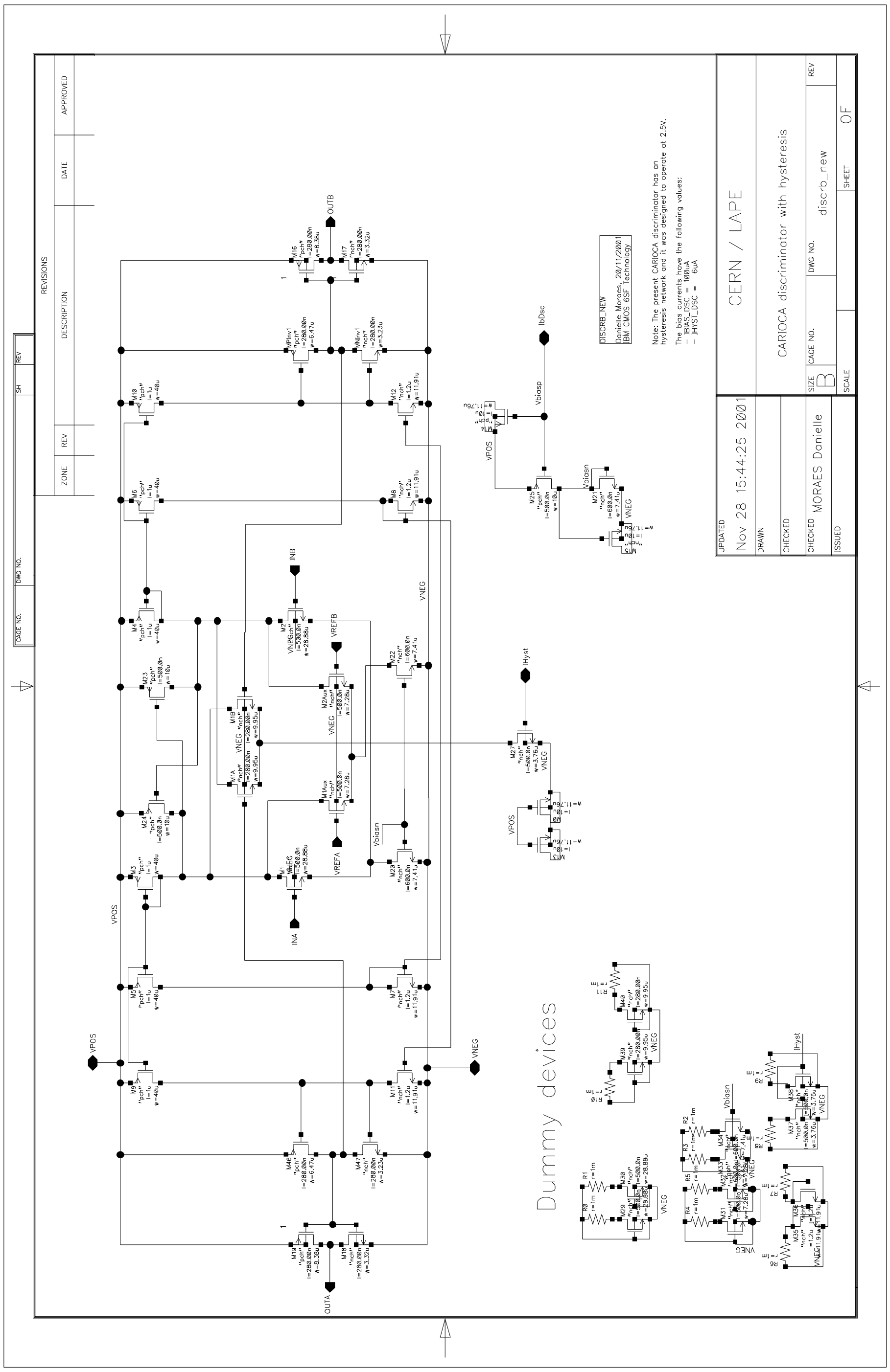


Figure B.15: Schematic of the CARIOCA discriminator.

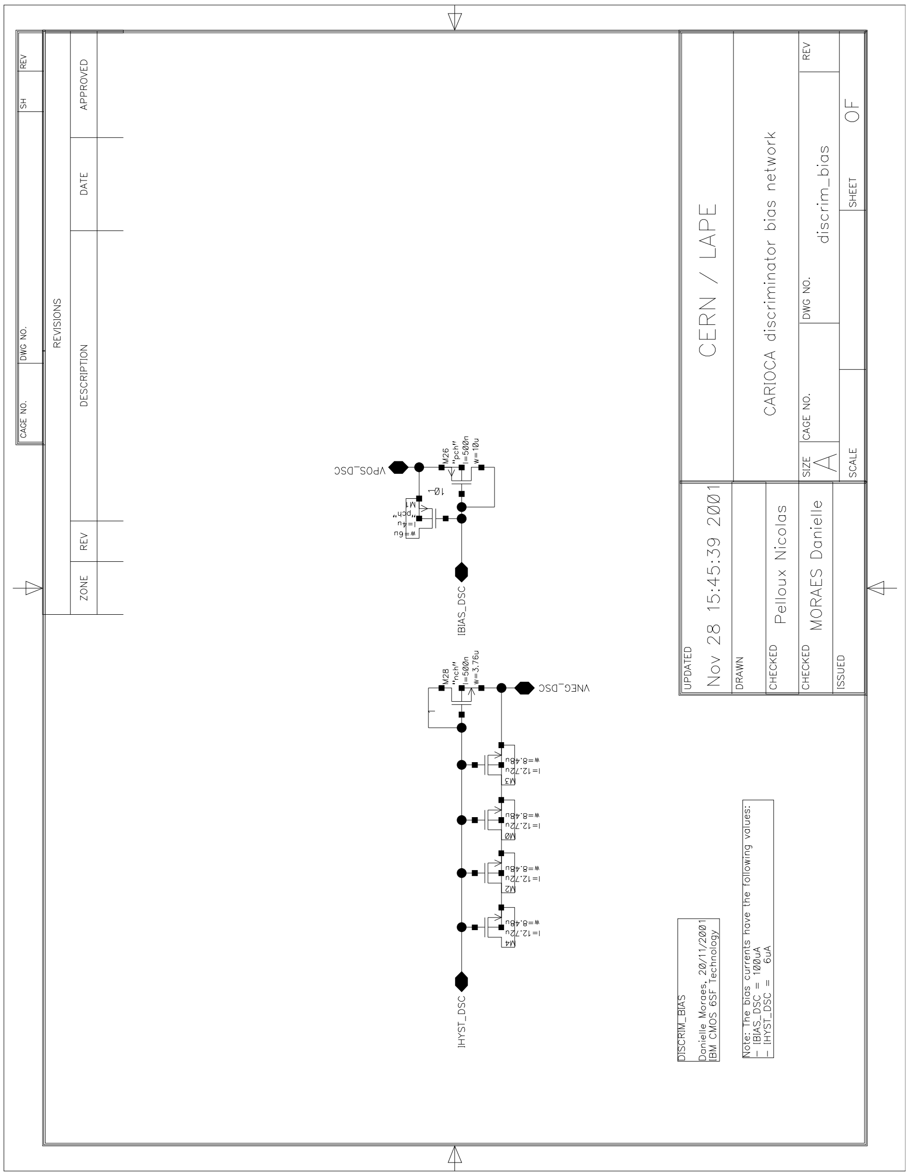


Figure B.16: Schematic of the CARIOCA discriminator bias network.

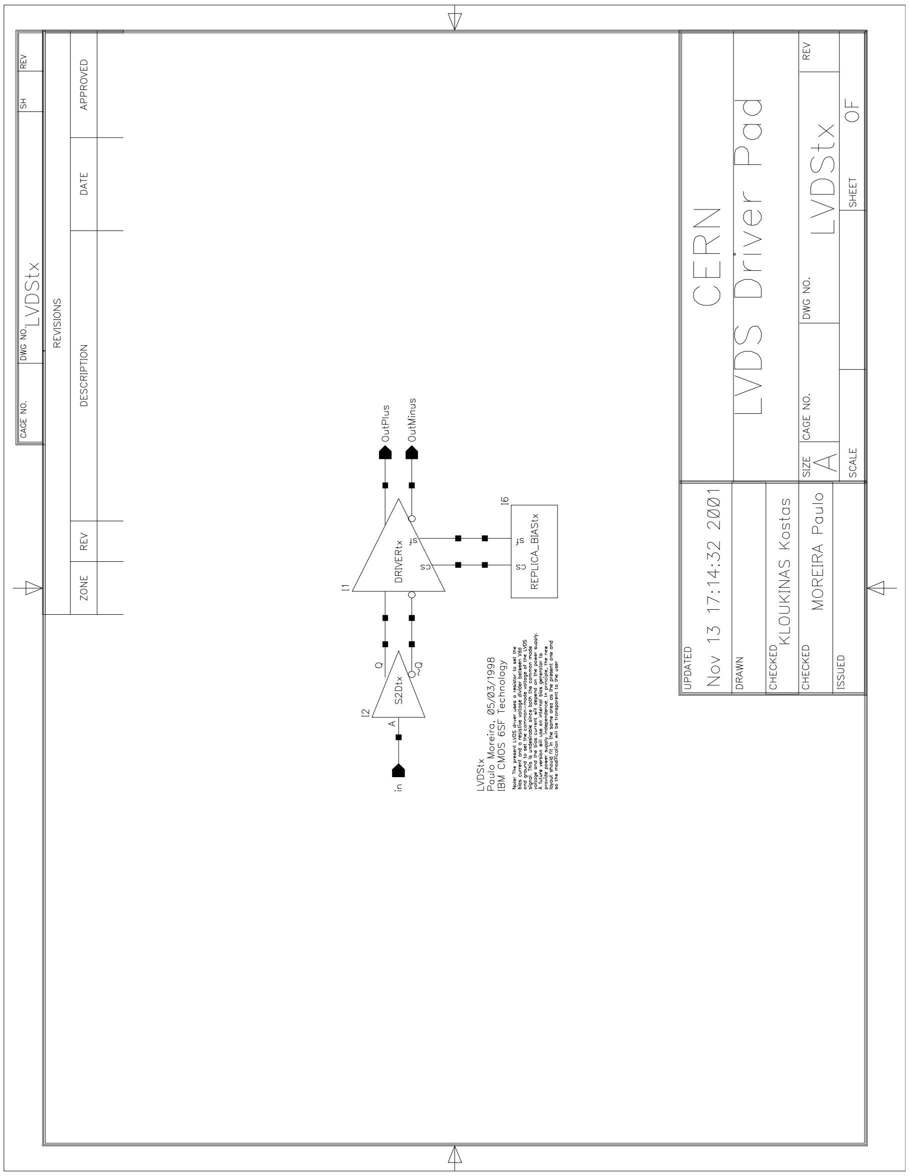


Figure B.17: Schematic of the CARIOCA LVDS driver.

Appendix C

CARIOCA Prototypes Photos

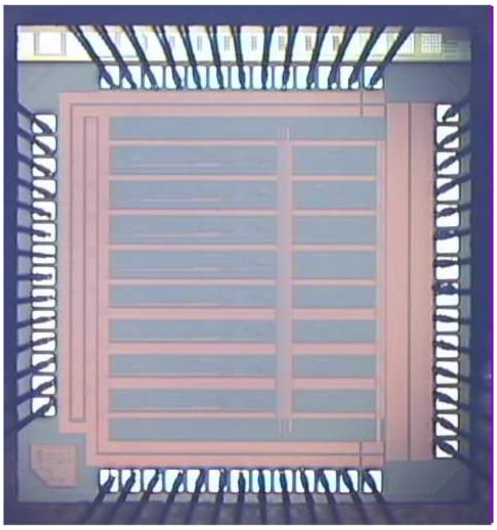


Figure C.1: Photo of the CARIOCA prototype I.

Figure C.2: Photo of the CARIOCA prototype II.

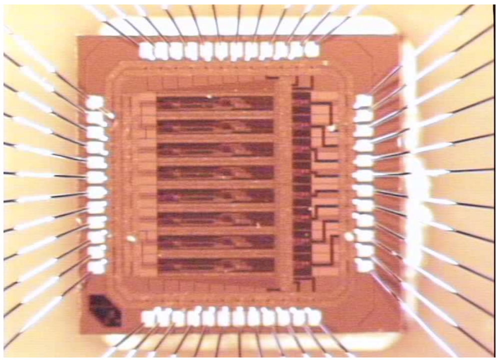


Figure C.3: Photo of the CARIOCA prototype III.

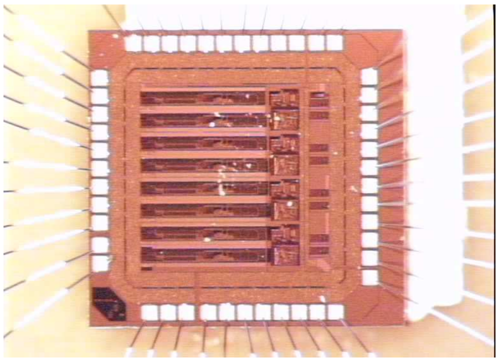


Figure C.4: Photo of the CARIOCA prototype IV.

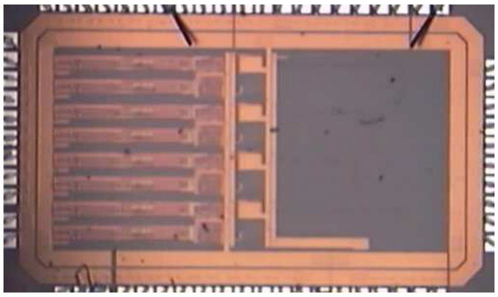


Figure C.5: Photo of the CARIOCA prototype V.

Bibliografia

[1] S. L. Glashow, Nucl. Phys. **B22** (1961) 579; S. Weinberg, Phys. Rev. Lett. **19** (1967) 1264; A. Salam in *Proceedings of the 8th Nobel Symposium*, p.367, ed. N. Svartholm, (Almquist and Wiksell) Stockholm (1968); F. J. Yndurain, "Quantum Chromodynamics: an Introduction to the Theory of Quarks and Gluons", New York (1983).

[2] M. E. Peskin, "Beyond the Standard Model", in *Proc. of 1996 European School of High-Energy Physics*, CERN 97-03 (1997) 52.

[3] http://cern.web.cern.ch/CERN/Divisions/SL/lep2page.html

[4] http://http://www.slac.stanford.edu/

[5] http://www-bd.fnal.gov/tevatron/

[6] G. Altarelli, "The Standard Model and beyond", hep-ph/9809532 (1998).

[7] N. Cabibbo, Phys. Rev. Lett. **10** (1963) 531; M. Kobayasi and K. Maskawa, Prog. Theor. Phys. **49** (1973) 652.

[8] H. P. Nilles, Phys. Reports **110** (1984) 1; H.E. Haber, Phys. Reports **117** (1985) 75.

[9] F. Vissani and A. Yu. Smirnov, Nucl. Phys. **B 460** (1996) 37; R. Hempfling, Nucl. Phys. **B 478** (1996) 3; H. P. Nilles and N. Plonsky, Nucl. Phys. **B 484**

(1997) 33; B. de Carlos and P. L. White, Phys. Rev. **D 55** (1997) 5772; S. Roy and B. Mukhopadhyaya, Phys. Rev. **D 55** (1997) 7020.

[10] A. Masiero and J. W. F. Valle, Phys. Lett. **B251** (1990) 273; J. C. Romão, C.A. Santos and J. W. F. Valle, Phys. Lett. **B288** (1992) 311.

[11] http://delphi.web.cern.ch/Delphi/

[12] http://lhcb.web.cern.ch/lhcb/

[13] http://lhc.web.cern.ch/lhc/

[14] P. Jarron *et al.*, "Study of Radiation Tolerance of ICs for the LHC", CERN/LHCC 2000-003 (2000).

[15] D. Moraes, "Estudo do Decaimento $\tau \rightarrow \pi(K)\nu_\tau$ no DELPHI/LEP", Master Thesis, Instituto de Física, Universidade Federal do Rio de Janeiro, 1998.

[16] A. Sopczak, "Limits on the Higgs Boson Masses from a MSSM Parameter Scan at $\sqrt{s} \leq 209\,\mathrm{GeV}$", in *Proc. of the European Physical Society International Europhysics Conference on High Energy Physics* (Budapest, Hungary, 2001) and in *Lepton Photon 2001 20th International Symposium on Lepton and Photon Interactions at High Energies* (Rome, Italy, 2001) DELPHI-2001-081 (2001).

[17] G. G. Ross, "Grand Unified Theories", Benjamin, New York, 1984; R. Mohapatra, Prog. Part. Nucl. Phys. 26 (1991) 1.

[18] P. C. W. Davies and J. Brown, "Superstrings: A Theory of Everything?", Cambridge University Press (1993) ISBN 0-521-45728-9.

[19] S. Weinberg, Phys. Rev. **D13** (1976) 974, Phys. Rev. **D19** (1979) 1277; L. Susskind, Phys. Rev. **D20** (1979) 2619.

[20] A. Bartl, H. Fraas and W. Majerotto, Z Phys. **C30** (1986) 441.

[21] A. Bartl, H. Fraas and W. Majerotto, Nucl. Phys. **B278** (1986) 1.

[22] C.S. Aulakh, R.N. Mohapatra, Phys. Lett. **B119** (1982) 136; A. Santamaria, J. W. F. Valle, Phys. Lett. **B195** (1987) 423; Phys. Rev. Lett. **60** (1988) 397; Phys. Rev. **D39** (1989) 1780.

[23] J. W. F. Valle, Phys. Lett. **B196** (1987) 157; M.C. Gonzalez-Garcia and J. W. F. Valle, Nucl. Phys. **B355** (1991) 330.

[24] F. de Campos, O.J.P. Éboli, M. A. García-Jareño, J. W. F. Valle, Nucl. Phys. **B546** (1999) 33.

[25] P. Nogueira, J. C. Romão, J. W. F. Valle, Phys. Lett. **B251** (1990) 142; R. Barbieri, D. E. Brahm, J. Hall, S.D.H. Hsu, Phys. Lett. **B238** (1990) 86.

[26] J. C. Romão, J. Rosiek and J. W. F. Valle, Phys. Lett. **B351** (1995) 497; J. C. Romão, N. Rius and J. W. F. Valle, Nucl. Phys. **B363** (1991) 369.

[27] R.N. Mohapatra and J. W. F. Valle, Phys. Rev. **D34** (1986) 1642; J. W. F. Valle, Nucl. Phys. **B11** (Proc. Suppl.) (1989) 118.

[28] R. Barbieri, S. Ferrara and C.A. Savoy, Phys. Lett. **B119** (1982) 343.

[29] J. C. Romão and J. W. F. Valle, Phys. Lett. **B272** (1991) 436, Nucl. Phys. **B381** (1992) 87.

[30] J. C. Romão, A. Ioannissyan and J. W. F. Valle, Phys. Rev. **D55** (1997) 427; M. A. Diaz, J. C. Romão and J. W. F. Valle, Nucl. Phys. **B524** (1998) 23.

[31] J. W. F. Valle, "Gauge Theories and the Physics of Neutrino Mass", Prog. Part. Nucl. Phys. **26** (1991) 91.

[32] DELPHI Collaboration, P.Aarnio *et al.*, Nucl. Instr. and Meth. **A303** (1991) 233; Nucl. Instr. and Meth. **A378** (1996) 57.

[33] P. Chochula *et al.*, Nucl. Instr. and Meth. **A412** (1998) 304.

[34] T. Sjöstrand, Computer Physics Communications **39** (1986) 347.

[35] S. Jadach, B.F.L. Ward and Z. Was, Computer Physics Communications **79** (1994) 503.

[36] J. Fujimoto *et al.*, Computer Physics Communications **100** (1997) 128.

[37] J.E. Campagne and R. Zitoun, Zeit. Phys. **C43** (1989) 469.

[38] F.A. Berends, R. Pittau, R. Kleiss, Computer Physics Communications **85** (1995) 437.

[39] M. Böhm, A. Denner and W. Hollik, Nucl. Phys. **B304** (1988) 687;
F.A. Berends, R. Kleiss and W. Hollik, Nucl. Phys. **B304** (1988) 712.

[40] F.A. Berends, P.H. Daverveldt, R. Kleiss, Computer Physics Communications **40** (1986) 271, 285, 309.

[41] T. Alderweirwld *et al.*, CERN-OPEN-2000-141.

[42] http://delphiwww.cern.ch/˜berggren/sgv.html.

[43] L. de Paula, M. Gandelman, D. Moraes, "Search for SUSY with spontaneously broken R-Parity at $\sqrt{s}$ = 183 GeV", in *Proc. of the 34th Rencontres de Moriond : Electroweak Interactions and Unified Theories* (Les Arcs, France) DELPHI-99-31 CONF 230, CERN-OPEN-99-467 (1999).

[44] L. de Paula, M. Gandelman, D. Moraes, "Search for Spontaneous R-Parity violation at $\sqrt{s}$ =183 GeV and 189 GeV", in *Proc. of the International Europhysics Conference on High-energy Physics* (Tampere, Finland) DELPHI-99-94 CONF 281, CERN-OPEN-99-417 (1999).

[45] DELPHI Collaboration, P.Abreu *et al.*, "Search for Spontaneous R-Parity violation at $\sqrt{s}$ = 183 GeV and 189 GeV", Phys. Lett. **B502** (2001) 24-38.

[46] DELPHI Collaboration, P.Abreu *et al.*, Phys. Lett. **B372** (1996) 172.

[47] L. de Paula, M. Gandelman, D. Moraes, "Search for Spontaneous R-parity violation at $\sqrt{s}$ = 189 GeV", in *Proc. of the 35th Rencontres de Moriond : Electroweak Interactions and Unified Theories* (Les Arcs, France) DELPHI-2000-021 CONF 342, CERN-OPEN-2000-342 (2000).

[48] L. de Paula, M. Gandelman, D. Moraes, "Search for Spontaneous R-Parity violation at center-of-mass energies=183 GeV and 189 GeV", in *Proc. of the 30th International Conference on High-energy Physics* (Osaka, Japan) DELPHI-2000-099 CONF 398, CERN-OPEN-2000-398 (2000).

[49] L. de Paula, M. Gandelman, D. Moraes, "Search for supersymmetry with R-parity violation at $\sqrt{s}$=192 to 208 GeV", in *Proc. of the European Physical Society International Europhysics Conference on High Energy Physics* (Budapest, Hungary, 2001) and in *Lepton Photon 2001 20th International Symposium on Lepton and Photon Interactions at High Energies* (Rome, Italy, 2001) DELPHI-2001-084, CERN-2001-512, (2001).

[50] L. de Paula, M. Gandelman, D. Moraes, "Update on the Search for Spontaneous R-parity Violation at centre-of-mass energies up to $\sqrt{s} \simeq 208$ GeV", DELPHI-2002-005 (2002).

[51] Particle Data Group, R.M. Barnett *et al.*, Phys. Rev. **D54** (1996).

[52] L3 Collaboration, M. Acciarri *et al.*, Phys. Lett. **B350** (1995) 109; OPAL Collaboration, G. Alexander *et al.*, Phys. Lett. **B377** (1996) 273.

[53] W. W. Armstrong *et al.*, ATLAS Collaboration, "ATLAS Technical Design Proposal", CERN-LHCC-94-43 (1994); "ATLAS Detector and Physics Performance: Technical Design Report, 2", CERN-LHCC-1999-015 (1999).

[54] G. L. Bayatian *et al.*, CMS Collaboration, "CMS Technical proposal", CERN-LHCC-94-38 (1994).

[55] ALICE Collaboration, "ALICE : a transition radiation detector for electron identification within the ALICE central detector", CERN-LHCC-99-013 (1999).

[56] S. Amato *et al.*, LHCb Collaboration, "LHCb : Technical Proposal", CERN-LHCC-98-004 (1998).

[57] J. H. Christenson *et al.*, Phys. Rev. Lett. **13** (1964) 795.

[58] http://www.slac.stanford.edu/BFROOT/

[59] http://bsunsrv1.kek.jp/

[60] http://www-cdf.fnal.gov/

[61] http://www.lns.cornell.edu/public/CLEO/

[62] http://www-d0.fnal.gov/

[63] http://www-hera-b.desy.de/

[64] B. Aubert *et al.*, "Improved Measurement of CP-violating Asymmetry Amplitude $\sin 2\beta$, BABAR-CONF-02/01, hep-ex/0203007 (2002).

[65] K. Hanagaki, "Recent results on CP violation from BELLE", in *Proc. of the 36th Rencontres de Moriond : Electroweak Interactions and Unified Theories* (Les Arcs, France) (2001).

[66] O. Schneider, "Future B physics prospects at hadron colliders", in *Proceedings of the 5th KEK topical conference "Frontiers in Flavour Physics"* (Tsukuba , Japan, 2001).

[67] A. F. Falk, "Flavor Physics and the CKM Matrix: an overview", in *Proceedings of the 5th KEK topical conference "Frontiers i n Flavour Physics"* (Tsukuba , Japan, 2001).

[68] A. Bornheim, “CLEO - recent results and future prospects”, in *Proceedings of the 5th KEK topical conference ”Frontiers in Flavour Physics”* (Tsukuba , Japan, 2001).

[69] F. Palla, “Recent B physics results from LEP and SLC”, in *Proceedings of the 5th KEK topical conference ”Frontiers in Flavour Physics”* (Tsukuba , Japan, 2001).

[70] V. Papadimitriou, “Tevatron B physics: recent results and prospects”, in *Proceedings of the 5th KEK topical conference ”Frontiers in Flavour Physics”* (Tsukuba , Japan, 2001).

[71] A. I. Sanda, Z. Z. Xing, **D56** (1997) 6866; M. Gronau and D. London, Phys. Rev, **D55** (1997) 2845.

[72] L. Wolfenstein, Phys. Rev. Lett. **51** (1983) 1945.

[73] LHCb Collaboration, “LHCb Magnet: Technical Design Report”, CERN-LHCC-2000-007, LHCb-TDR-1 (1999).

[74] LHCb Collaboration, “LHCb VELO (Vertex Locator): Technical Design Report”, CERN-LHCC-2001-011, LHCb-TDR-5 (2001).

[75] LHCb Collaboration, “LHCb Outer Tracker: Technical Design Report”, CERN-LHCC-2001-024, LHCb-TDR-6 (2001).

[76] LHCb Collaboration, “LHCb RICH: Technical Design Report”, CERN-LHCC-2000-037, LHCb-TDR-3 (2000).

[77] LHCb Collaboration, “LHCb Calorimeters: Technical Design Report”, CERN-LHCC-2000-036, LHCb-TDR-2 (2000).

[78] LHCb Collaboration, “LHCb Muon System: Technical Design Report”, CERN-LHCC-2001-010, LHCb-TDR-4 (2001).

[79] LHCb Collaboration, "LHCb Data Acquisition and Experiment Control: Technical Design Report", CERN-LHCC-2001-040, LHCb-TDR-7 (2001).

[80] "Requirements for the L0 front-end electronics", LHCb-1999-029 (1999).

[81] A. Lai *et al.*, "Muon Detector Front-end Architecture: an update", LHCb-2001-030 (2001); A. Lai *et al.*, "Muon Detector Front-end Architecture", LHCb-2000-017 (2000).

[82] E. Aslanides *et al.*, "A synchronous architecture for the L0 muon trigger", LHCb-2001-010; E. Aslanides *et al.*, "The L0(μ processor", LHCb-1999-008.

[83] E. Polycarpo and J. R. T. de Mello Neto, "Update on muon identification", LHCb-2001-061; E. Polycarpo and J. R. T. de Mello Neto, "Muon Identification in LHCb", LHCb-2001-009.

[84] B. Botchine *et al.*, "Wire pad chambers and cathode pad chambers for the LHCb muon system", LHCb-2000-114 (2000).

[85] M. Adinolfi *et al.*, "Proposal for the RPC Muon Detector of LHCb", LHCb-2000-053 (2000).

[86] G. Bencivenni *et al.*, " A triple-GEM detector with pad readout for the inner region of the first LHCb muon station", LHCb-2001-051 (2001).

[87] W. Riegler, "RPC Simulations", LHCb-2000-112 (2000).

[88] M. Adinolfi *et al.*, "Performance of low-resistivity single and dual-gap RPCs for LHCb", Nucl. Instr. and Meth. **A456** (2000) 95.

[89] W. Riegler, "Detector Physics and performance Simulations of the MWPCs for the LHCb Muon System", LHCb-2000-060 (2000).

[90] B. Bochin *et al.*, "Wire Pad chambers for the LHCb Muon System", LHCb-2000-003 (2000).

[91] A. Kashchuk *et al.*, “Performance study of a MWPC prototype for the LHCb Muon System with the ASDQ chip”, LHCb-2000-062 (2000).

[92] B. Bochin *et al.*, “Wire Pad chambers and Cathode Pad Chambers for the LHCb Muon System”, LHCb-2000-114 (2000).

[93] D. Hutchcroft *et al.*, “Performance study of a MWPC prototype for the LHCb Muon System with the ASDQ chip”, LHCb-2000-062 (2000).

[94] B. Bochin *et al.*, “Beam tests of WPC-7 prototype of the wire pad chambers for the LHCb Muon System”, LHCb-2000-112 (2000).

[95] B. Bochin *et al.*, “Beam tests of WPC-8 and WPC-9 prototypes of the wire pad chambers”, LHCb-2001-024 (2001).

[96] W. Riegler, “Crosstalk, cathode structure and electrical parameters of the MWPCs for the LHCb muon system”, LHCb-2000-061.

[97] W. Bokhari *et al.*, “The ASDQ ASIC for the Front End electronics of the COT”, CDF/DOC/Tracking/CDFR/4515 (1999).

[98] O. Sasaki and M. Yoshida, “ASD IC for the thin gap chambers in the LHC ATLAS Experiment”, IEEE Trans. Nucl. Sci. **46** (1999) no.3 1871.

[99] F. Anghinolfi *et al.*, “CARIOCA - A Fast Binary Front-End Implemented in 0.25um CMOS using a Novel Current-Mode Technique for the LHCb Muon detector”, LHCb-200-093 (2000).

[100] P. R. Gray and R. G. Meyer, “Analysis and Design of Integrated Circuits”, University of California, Berkeley (1984) ISBN 0-471-87493-0.

[101] Bashir Al-Hashimi, “The Art of Analog and Digital Simulation using PSPICE”, CRC Press (1995) ISBN 0-8493-7895-8.

[102] D. Moraes, W. Bonivento, P. Jarron, W. Riegler, F. dos Santos, "Status of the CARIOCA Project", in *Proceedings of the VII Workshop on Electronics for LHC Experiments* (Stockholm, Sweden, 2001) CERN 2001-005, CERN/LHCC/2001-034.

[103] R.A.Boie *et al.*, Nucl. Instr. and Meth. **192** (1982) 365.

[104] M. Newcomer *et al.*, Progress in development of the ASDBLR ASIC for the ATLAS TRT, in *Proceedings of the V Workshop on Electronics for LHC Experiments* (Colorado, USA, 1999) CERN/LHCC/99-33.

[105] Behzad Razavi, Design of Analog CMOS Integrated Circuits, (2001).

[106] C. Posch *et al.*, CMOS front-end for the MDT sub-detector in the ATLAS Muon Spectrometer, development and performance, in *Proceedings of the VII Workshop on Electronics for LHC Experiments* (Stockholm, Sweden, 2001) CERN 2001-005, CERN/LHCC/2001-034.

[107] Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), IEEE P1596.3-1995, IEEE Standard Document (1995).

[108] P. Jarron *et al.*, Nucl. Phys. **B78** (1999) 625-634.

[109] D. Moraes, W. Bonivento, P. Jarron, W. Riegler, F. dos Santos, "Development of the CARIOCA front-end chip for the LHCb muon detector", *submitted to Elsevier Science in January of 2002.*

[110] D. Moraes, F. Anghinolfi, P. Deval, P. Jarron, W. Riegler, A. Rivetti, B. Schmidt, 2001 IEEE International Conference on Circuits and Systems, Volume I, 360-363.

[111] D.Moraes, W.Bonivento, N.Pelloux, "Measurement results of the First CARIOCA Front-end Version for Cathode Readout", LHCb-Muon 2001-064 (2001).

[112] D. Moraes, F. Anghinolfi, P. Deval, P. Jarron, W. Riegler, A. Rivetti, B. Schmidt, "CARIOCA - A Fast Binary Front-End Implemented in 0.25um CMOS using a Novel Current-Mode Technique for the LHCb Muon detector", in *Proceedings of the VI Workshop on Electronics for LHC Experiments* (Cracow, Poland, 2000) CERN-2000-010, CERN/LHCC/2000-041.

[113] Y. Sugimoto, M. Sekiya and T. Lida, " A Study if the Signal-to-Noise Ratio of a High-Speed Current-mode CMOS Sample-and-Hold Circuit", IEIEC Trans. Fund. **E48**, 10 (1997).

[114] V.Radeka, "Low Noise techniques in Detectors", Ann. Rev. Nucl. Part. Sci. 1988, 217-277.

[115] G. Anelli, F. Faccio, S. Florian, P. Jarron, "Noise characterization of 0.25 μm CMOS technology for the LHC experiments", Nucl. Instr. Meth. in Physics Research **A457**, issues 1-2, 361-368(2001) .

[116] http:www.ni.com

[117] A. Kachtchouk, W. Riegler, B. Schmidt, T. Schneider, L. de Paula, "Performance study of a MWPC prototype for the LHCb Muon System with the ASDQ chip", A. Kachtchouk, LHCb-Muon 2000-062 (2000).

[118] G. Anelli *et al.*, " Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS technologies for the LHC experiments", IEEE Trans Nucl. Science 46, 6 (1999).

[119] E. A. Vittoz, "Notes of the Advanced Engineering Course on CMOS & BiCMOS IC Design", Lausanne, Switzerland, 1996.

[120] R. H. Dennard *et al.*, " Design of ion-implanted MOSFET's with very small physical dimension", IEEE Journal of Solid-State Circuits 9, 256-268 (1974).

[121] http://notes.sematech.org/ntrs/Rdmpmen.nsf, “The technology Roadmap for Semiconductors”, 1999 Edition.

[122] G. Anelli, “Design and characterization of radiation tolerant integrated circuits in deep submicron CMOS technologies for the LHC experiments”, PhD Thesis, Institut National Polytechnique de Grenoble, 2000.

List of Figures

List of Tables