

## Why IEEE 1355?



- The restrictions of backplane interconnects are widely recognised to be a limiting factor in high performance distributed system applications.
- Serial technology offers a way out.
- The requirement is for a Standard, Low Cost, Low Latency,
  Physical Interconnection Layer
- O This layer must:
  - ✓ Deliver reliable raw performance
  - ✓ Support higher level protocols( ATM, Fiberchannel, SCI, etc)
- O Application areas:

✓ Silicon to Silicon Physical layer only

✓ Chip to Chip
 Physical layer only

✓ Board to Board Physical or higher layer protocol





### What is IEEE 1355?



- Olt is a Standard for a:
  - ✓ Low Cost, Low Latency, Physical Interconnection Layer
- O There are two serial link protocols defined:
  - ✓ DS Links for the range 100 to 200 Mbaud
  - ✓ HS Links for the range 1 to 3 Gbaud
- The DS link protocol is a four wire bidirectional protocol.
  - ✓ Two wires in each direction. Self clocking code.
  - ✓ The Strobe line moves when the Data line does not.
- The HS link is a two wire bidirectional protocol
  - ✓ One wire in each direction, 8B/12B DC balanced code
  - ✓ Delay Locked Loop
- ODS macrocell dimensions
  - √ 0.2 mm² 0.1 W @ 0.5micron CMOS
- OHS macrocell dimensions
  - √ 1 mm² 0.3 W @ 0.5micron CMOS





## What components support IEEE 1355?



#### ODS LINKS

#### o STC101:

- ✓ Parallel to DS link serial interface chip.
- ✓ 32 or 16 bit data bus
- ✓ Synchronous or Asynchronous parallel transfer
- √ 64 byte Fifo buffering
- √ variable packet size (limit 4 Kbyte)
- ✓ 100 Mbit/sec

#### o STC104:

- √ 32 way non blocking cross bar switch
- √ >300 Mbytes/s cross sectional bandwidth
- ✓ ~1µs packet latency
- ✓ Grouped Adaptive Routing
- ✓ Universal Routing





## What components support IEEE 1355?



#### **OHS LINKS**

#### O BULLIT:

- ✓ Parallel to HS link serial interface chip.
- ✓ Technology evaluation device
- ✓ Full or reduced protocol options
- √ Fifo buffering
- ✓ ~800 Mbit/sec

#### O RCUBE:

- √ 8 way non blocking cross bar switch
- √ >600 Mbytes/s cross sectional bandwidth
- √ ~150 nS packet latency
- ✓ Grouped Adaptive Routing
- ✓ Parallel access to the routing core





## Who developed IEEE 1355?



#### O The ESPRIT framework

- ✓ Macrocell development under the OMI / HIC program.
- ✓ System Design and Application work under OMI / MACRAME
- ✓ Networking Analysis under PUMA
- ✓ Embedded product development under GPMIMD
- Industrial Partners
  - ✓ Technology providers: BULL SGS-THOMSON,
  - ✓ Technology exploiters: DOLPHIN, PARSYS, PARSYTEC,

TELMAT, THOMSON

- ✓ R & D & Applications: CERN, PACT, PARSYTEC, SINTEF
- ✓ University Groups: OSLO, UPMC, SOUTHAMPTON
- Standards Working Group: >70 Organisations
  Represented





## Where are the first applications of IEEE 1355?

- The GPMIMD project delivered
  - √ a 64 processor node machine
  - ✓ interconnected through four folded CLOS networks
  - √ 56 STC104 switches.
  - √ measured cross-sectional bandwidth ~1Gbyte/sec.
- This DS link technology is repackaged and marketed by Parsys, and Telmat
- O At CERN the L3 experiment adopted the technology for the level 2 trigger in the data acquisition system.
- Parsytec is bringing a HS link based technology to market.





# What IEEE 1355 products can be seen at HPCN?



- O PARSYS is showing:
  - ✓ PCI to DS link interface
  - ✓ Ethernet to DS link interface
  - ✓ SCSI to DS link interface
- O PARSYTEC is showing:
  - ✓ PCI to HS link interface
  - √ 8\*8 discrete HS link routing module
  - ✓ Processor motherboard with HS link connectivity
  - ✓ Application example of steel quality control





## **Summary**



- IEEE1355 is a European technology for high performance serial connectivity.
- The standard passed ballot in 1995.
- Application of IEEE1355 to emerging standards is being actively pursued.
- Silicon solutions are here now to enable exploitation.
- Embedding the technology into user silicon is a simple procedure.
- Demanding real time applications are proving the technology.
- Commercial products exploiting the technology are available now.

