Nov. 21, 1999

Neutron Irradiation Tests of an S-LINK-over-G-link System

K. Anderson, J. Pilcher, H. Wu
Enrico Fermi Institute, University of Chicago, Chicago, IL

E. van der Bij, Z. Meggyesi
EP/ATE Division, CERN, Geneva, Switzerland

J. Adams
National Institute of Standards and Technology, Gaithersberg, MD

1. Objective

This note describes neutron irradiation tests of an S-LINK [1] source card (LSC) which incorporates the Hewlett Packard G-link chip set [2]. The test was designed to evaluate the use of this technology in the ATLAS Tile Calorimeter. At the position of this card the nominal neutron flux is 10^{10} 1-MeV-equivalent-n/cm^2/year and the expected dose from ionizing radiation is 0.02 Krad/yr. Based on 10 years operation at design luminosity and a safety factor of 5, the card must withstand a neutron fluence of 5×10^{11} n/cm^2 and a dose from of ionizing radiation of 1 Krad. Single event upset is also an important consideration and was carefully monitored.

2. Neutron Source Characteristics

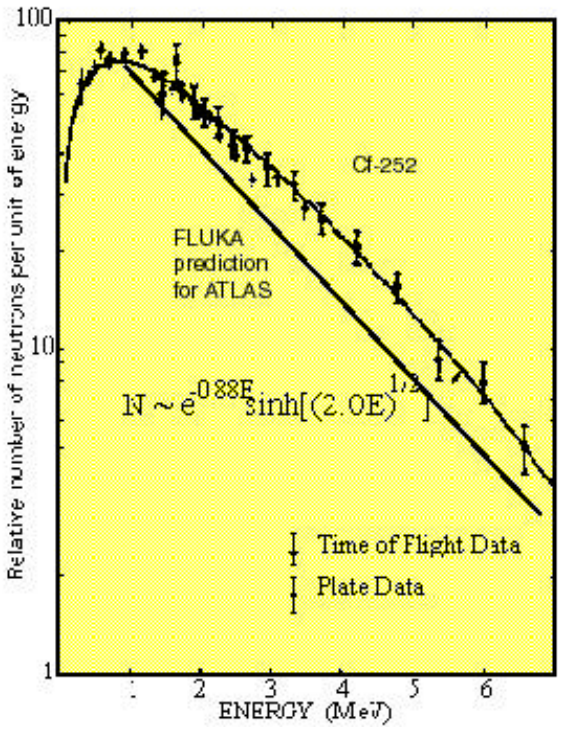

Figure 1: Neutron energy spectrum from Cf–252 together with expected spectrum in ATLAS.

The test was performed at the National Institute of Standards and Technology (NIST) in Gaithersburg Maryland using a Californium–252 fission source which produced 5.0×10^9 n/s. The test exposure lasted for 3 weeks; a period short compared to the 2.65 year half-life of Cf–252.

The neutron energy spectrum of Cf–252 is shown in Fig. 1. It has a peak at ~ 0.7 MeV and a mean energy of 2.14 MeV. Approximately 7% of the neutrons have an energy above 5 MeV. A prediction of the neutron spectrum in the ATLAS gap region using the FLUKA Monte Carlo program is also shown in Fig. 1. The variation with energy is a good match to

the Cf-252 spectrum [3].

A convolution of the spectrum with the energy dependent displacement damage function for neutrons in silicon indicates that the neutrons from Cf–252 cause 1.06 times the damage of 1 MeV monochromatic neutrons [4]. In the analysis below this factor is treated as a safety margin and has not been applied.

The source also produces a modest flux of photons. The dose from ionizing radiation from an unshielded Cf-252 source is 2.9 Krad for 10^{12} n/cm^2 [5].

3. S-LINK System

The test used an S-LINK-over-G-link combination of source and destination cards specially prepared for the study of link errors [6]. The cards used Hewlett Packard HDMP-1022/1024 transmitter/receiver chips operated in 20-bit, single frame mode with a 40 MHz clock. The optical transmitter on the LSC was a Methode MDX-19-4-1-S and an Actel A54SX16 FPGA was used for logic control. The 40 MHz oscillator was a Temex QEN 47-CH.

The data pattern sent by the LSC was set by switches on card and the setting was downloaded to the LDC card through its computer connection. The pattern used for this test had alternate bits set. The LSC generated the test data at the full link speed of 640 Mb/s. The data were compared in the LDC to the expected pattern and only transmitted to the monitoring computer in case of a discrepancy. Errors related to link protocol were also transmitted. We note that in the TileCal application the data rate over the optical link is 346 Mb/s for the maximum LVL1 trigger rate of 75 KHz.

4. Test Configuration

The source was placed ~10 cm from the face of the LSC with the card normal to a line from the source. To reduce the photon dose, 6 mm of lead shielding was placed between the source and the card. This is estimated to reduce the neutron flux by ~12% and the photon dose by >40%. For this configuration the neutron flux at the center of the card was 3.0×10^{11} n/cm^2/day.

The LDC card was placed in a low radiation environment and connected to the LSC by a 30-m-long simplex optical fiber**.** Data errors detected by the S-LINK LDC were transferred to a PC via a PCI interface card [7] and were logged to disk using a simple data acquisition program. The clock time of each error was logged with the data.

5. Test Results

The test began September 1, 1999 and ended September 19 with a fatal failure of the LSC because of the voltage regulator transistor. During this period the card received a total neutron fluence of 5.7×10^{12} n/cm^2, or approximately 10 times the required level.

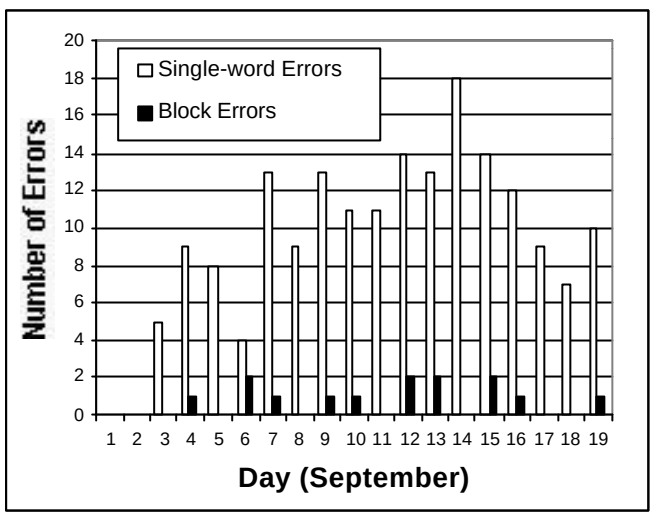

Figure 2: Time distribution of errors.

The errors fall into two categories; single-word errors, and blocks of errors lasting more than 10 microseconds. The latter are likely associated with loss of synchronization of the link. The distribution of these errors over the duration of the test is shown in Fig. 2. The average rate of single-word errors was 9.5 per day and the rate of block errors 0.74 per day. For the neutron flux of this test these figures correspond to one single-word error per 3.2×10^{10} n/cm^2 and one block-error per 4.1×10^{11} n/cm^2. For the ATLAS TileCal system with 256 links, and at the nominal neutron flux for the design luminosity of the LHC given in Section 1, they correspond to 6.7 single-word errors and 0.53 block errors per month anywhere in the system.

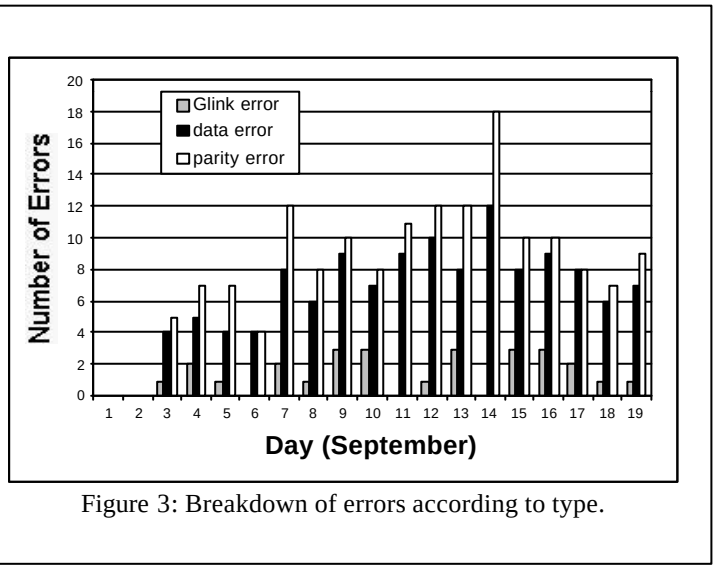

Figure 3: Breakdown of errors according to type.

Errors were classified as G-link internal errors, data mismatch, parity mismatch, and frame-length mismatch. These errors can arise from single event upset of any of the components on the LSC. An analysis of the data showed no frame length mismatch errors. The rate of other types of errors is shown in Fig. 3. Most error events involved more than one type of error and correspond to several entries in Fig. 3. Note that most errors are flagged by the parity bit.

6. Conclusions

1. The survivability of the S-LINK-over-G-link system under neutron irradiation has been satisfactorily demonstrated. The system continued to operate at 10 times the required neutron fluence.

2. The observed rate of single-word errors would correspond to 6.7 per month from the entire ATLAS TileCal system for the nominal neutron fluence indicated in Section 1. Since these errors are detectable from parity information, and since the data itself has considerable redundancy, this error rate should not pose a problem; nevertheless, the ROD modules which receive the data must test for these errors and take appropriate action. The actual error rate in ATLAS should be lower because the link will only be used with a duty factor of ~50% of that used here.

3. The observed rate of block errors would correspond to 0.53 per month from the entire TileCal system. Such errors would result in the loss of all data from one electronics drawer ($1/256^{th}$ of the system) for a number of consecutive events. If these errors correspond to loss of link synchronization the recovery time is estimated to be ~ 0.5 ms [8]. At the maximum LVL1 trigger rate this would correspond to a block of ~ 40 events. The fraction of LVL1 triggers affected by such an error would be $\sim 10^{-10}$. Such a loss appears entirely acceptable but an ATLAS-wide policy would be helpful for reaching a conclusion. These block errors correspond to a bit error rate on a single link in the nominal TileCal neutron environment of 4×10^{-13}.

4. These results correspond to the Cf-252 neutron spectrum given Fig. 1 which closely approximates 1 MeV neutrons. A more detailed calculation of the neutron spectrum in the TileCal electronics drawers would be desirable, particularly the region above 5 MeV.

5. During this test the LSC was exposed to 9.9 Krad of ionizing radiation. Separate studies have indicated that the system remains fully functional to over 20 Krad [9].

References:

1. Details on the S-LINK system can be found at: http://www.cern.ch/HSI/s-link/.

2. The G-link system is described at:
http://www.semiconductor.agilent.com/io/hdmp1022.html.

3. The FLUKA calculation was done by P. Sala and applies to the gap region of the detector where the LAr electronics is located. The spectrum inside the TileCal electronics drawers could be somewhat softer.

4. S. Reucroft et al., Nucl. Instr. & Meth. A394, 199 (1997) and J. Swain, private communication.

5. R. Martin, Oak Ridge National Laboratory, private communication.
6. Further details on this system are available at: http://www.cern.ch/HSI/s-link/devices/g-lsc/.

7. The S-LINK to PCI interface card is described at: http://www.cern.ch/HSI/s-link/devices/slink-pci/.

8. This is believed to be an upper limit since preliminary measurements reported by Mark Pearce give 0.3 ms.

9. Zoltán Meggyesi et al., FPGA Design in the Presence of Single Event Upsets, poster session paper presented at the LEB Workshop, Snowmass, Colorado, Sept. 20-24, 1999.