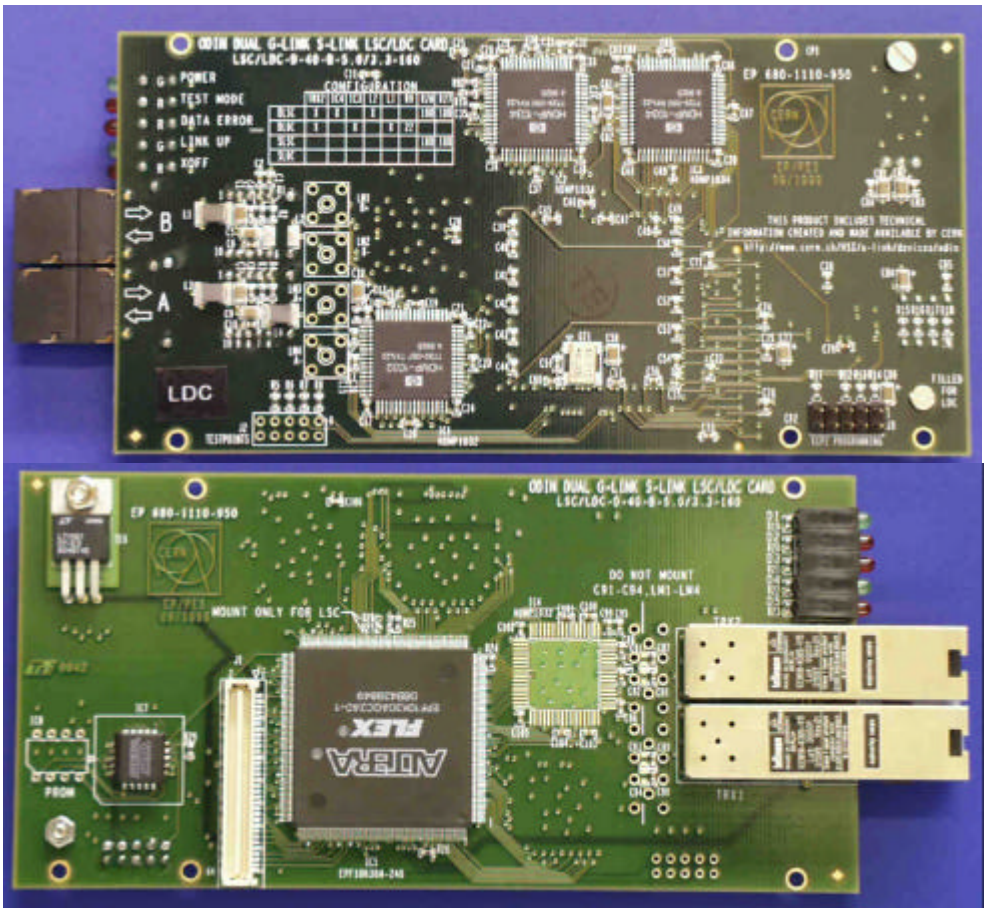
ODIN S-LINK

INTERFACE

DATA SHEET

LSC / LDC-D-40-B-5.0 / 3.3-160

VERSION 1.0



1. INTRODUCTION

The ODIN S-LINK is a standard duplex S-LINK that uses the low power G-Link chip-set (HDMP-1032/34) as physical layer. Its components are the Link Source Card (LSC), the Link Destination Card (LDC) cards and a fiber optic cable with Volition duplex connectors. More information, including this document, about the ODIN Interface can be found on the World Wide Web at:

`http://www.cern.ch/HSI/s-link/devices/odin/`

This document is intended as a user guide as it contains all ODIN-specific information needed to use the link. The reader of this document should know the basics of the S-LINK specification as this data sheet only point out a few important features of ODIN and makes a few clarifications. The S-Link specification can be downloaded from the World-Wide-Web at:

`http://www.cern.ch/HSI/s-link/spec/`

2. MAIN FEATURES

ODIN exists in two different operation versions, single and double channel, where one or two G-Link chip sets are used in the forward channel. These two versions cannot be mixed; i.e. a single channel LSC will not work with a double channel LDC and vice versa. ODIN also exists in two different voltage versions, 3.3V and 5V. See Figure 2-1 for block diagram of the double channel version and the usage of the two optical fibers.

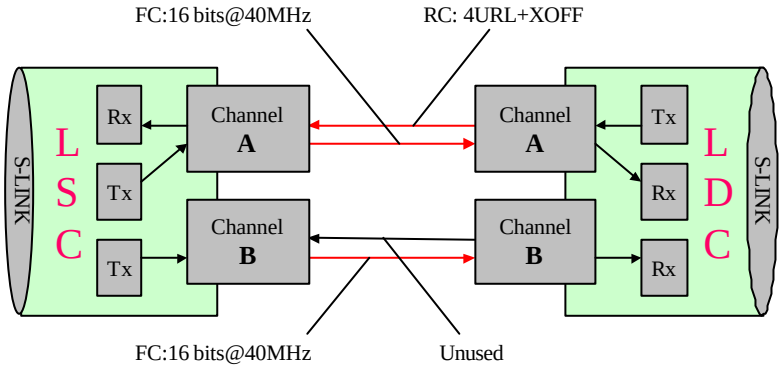


Figure 2-1 Double channel ODIN

The S-LINK code for the ODIN cards is:

LSC/LDC-D-40-B-5.0/3.3-160

The main features of the ODIN S-LINK implementation are:

General features

- Duplex S-Link
- 32 bit data width
- UCLK up to 40Mhz
- Block basis error reporting on data words
- Word-by-word error reporting on control words
- 5V tolerant input signal levels
- Option of 3.3V or 5.0V power input PCB versions
- Power consumption per board typically 5.5W, max. 7W at 5.0V, 3.6W, max 4.5W at 3.3V
- Autonomous link synchronization and maintenance of physical link
- Improved S-LINK Reset protocol
- Flow control is provided both in data mode and self-test modes
- Optical output, max. cable length with 50µm multimode cables: 550m

Double channel version

- 40 MHz LCLK
- 160 Mbytes/s maximum data transfer rate
- 80 Mbytes/s transmission rate for control information (UCTRL# low)
- 5 MHz sampling rate for the return lines
- Maximum 1m fiber length difference

Single channel version

- 32 MHz LCLK
- 128 Mbytes/s maximum data transfer rate
- 64 Mbytes/s transmission rate for control information (UCTRL# low)
- 8 MHz sampling rate for the return lines

3. INSTALLATION

Fix the ODIN S-LINK cards with screws to standoff pillars and front panel mounting holes to avoid mechanical stress and contact problems. For proper operation the board should be fixed by all four screws. Avoid mechanical stress on the cards during mounting. Do not plug in and out the cards on the motherboard when this is powered on.

Before powering up, check that the voltage version of the ODIN is the same as the motherboard. 5V motherboard should have a voltage keying pin described in S-LINK specification [1] and the 3.3V ODIN should not have a voltage hole to eliminate the chance of mounting 3.3V S-LINK on a 5V motherboard. Mounting 5V ODIN on a 3.3V motherboard is physically possible, but will not work.

Double Odin features two optical connectors, marked A and B, and cables must not be switched. Maximum length difference is 1 meter. If cables are different in length channel B should have the shorter cable for better word alignment tolerance.

Connect the optical fiber(s) and after powering up the cards and the link goes up immediately and Power and Link up leds go on. There is no need for a reset at power up as the cards go up when powered on and fibers are connected.

4. OPERATING CONDITIONS

Table 4-1 shows current drawn by the different versions and the recommended operating conditions to guarantee good performance.

Symbol	Description	Min	Typical	Max	Units
$I_{cc,d}$	Current drawn, Single ODIN	700	1000	1200	mA
$I_{cc,d}$	Current drawn, Double ODIN	1000	1200	1400	mA
V_{cc} (3.3V board)	Voltage	3.1	3.3	3.5	V
V_{cc} (5V board)	Voltage	4.5	5.0	6.0	V
T_{op}	Temperature	0	25	70	°C

Table 4-1 ODIN operating conditions

5. TIMING CHARACTERISTICS

Table 5-1 gives the required timing parameter for LSC for proper operation. See [1] for explanation of the parameters.

Symbol	**Description**	**Min**	**Max**	**Units**
t_{DS}	Data Set-up time	10		ns
t_{DH}	Data Hold time	1		ns
t_{ENS}	Enable Set-up time	10		ns
t_{ENH}	Enable Hold time	1		ns
t_{WFF}	Write Clock to Full Flag		12	ns
t_{CLK}	Clock Cycle time	25		ns
t_{CH}	Clock High time	11		ns
t_{cl}	Clock Low time	11		ns

Table 5-1 LSC timing parameters

Table 5-2 gives the guaranteed timing parameters for LDC. Suffix –single relates to single channel ODIN with 64 MHz transmission frequency and 32 MHz LCKL. Suffix –double relates to double channel ODIN with 40 MHz transmission frequency and 40 MHz LCLK.

Symbol	**Description**	**Min**	**Max**	**Units**
t_{DS}	Data Set-up time	10		ns
t_{DH}	Data Hold time	1		ns
t_{ENS}	Enable Set-up time	10		ns
t_{ENH}	Enable Hold time	1		ns
$t_{CLK\text{-}single}$	Clock Cycle time	31		ns
$t_{CH\text{-}single}$	Clock High time	13		ns
$t_{cl\text{-}single}$	Clock Low time	13		ns
$t_{CLK\text{-}double}$	Clock Cycle time	25		ns
$t_{CH\text{-}double}$	Clock High time	11		ns
$t_{cl\text{-}double}$	Clock Low time	11		ns

Table 5-2 LDC timing parameters

6. OPTICAL CHARACTERISTICS

Symbol	Description	Min	Typical	Max	Units
	Link length (50/125 m)	2		550	m
	Link length (62.5/125 m)	2		260	m
BER	Bit Error Rate			10^{-12}	
$ë_c$	Center wavelength	830	850	860	nm

Table 6-1 ODIN optical characteristics

7. LED INDICATORS

LED symbol	Colour	Function at LSC	Function at LDC
PWR	green	Power On	Power On
TST	red	Self test Mode	Self test Mode
ERR	red	-	Data Error
UP	green	Not Link Down	Not Link Down
XOF	red	Link Full Flag	UXOFF active

Table 7-1 LSC and LDC LED indicators

8. USER DATA WIDTH LINES

The UDW input lines are unused. If ODIN is set to 16 or 8-bit mode the effective transmission rate will go down accordingly since all 32 bits always are transferred.

9. DATA TRANSFER

The ODIN S-LINK will transfer all input data when up, Power and Link Up leds are on and LDOWN# line is high on both sides. If data is written to single channel LSC faster than 32 MHz the LFF# will go low and the XOFF led goes on at the LSC, even if there is no flow control sent from LDC. This is because maximum data transmission rate is 128 Mbytes/s. For maximum transfer rate, 2 more words should be written to LSC after LFF# goes low.

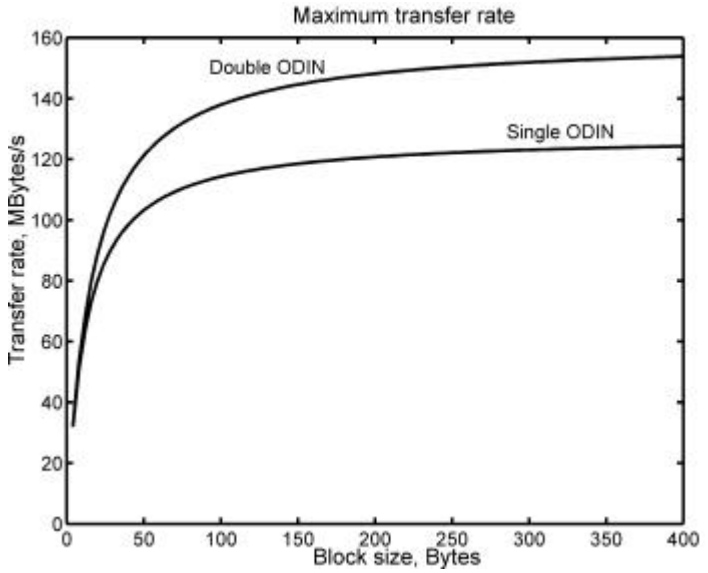


Figure 9-1 Maximum transfer rate at different data block sizes with 40 MHz UCLK

For small data block sizes the LFF# line will also become active as error detection and S-LINK control words take up bandwidth. Figure 9-1 gives maximum average transfer rate for small block sizes. The block size refers to the ATLAS event data format where one Begin of Fragment control word and one End of Fragment control word frames the data words. These transfer rates given are maximum values and to reach the maximum value 2 more words must be written to LSC after LFF# goes low. Also note that the graph shows the average values while the nominal value inside a block is the maximum transfer rate.

10. S-LINK RESET

ODIN S-LINK features an improved reset protocol, which is backward compatible. The user may reset the whole link from either side, or even both sides. The card reset is changed into a link reset to make the reset an easy and reliable operation regardless of usage.

If the link is down prior to the reset cycle, LDC will come up before LSC, regardless of which side the reset is performed. This eliminates the chance of data written to LSC being lost because of LDC being down.

If the link is up prior to the reset cycle, the card where URESET# line is asserted will go down according to [1]. The other side will be reset without going down.

It is not recommended to perform a reset while writing data to the LSC, as this will cause data loss.

11. TEST MODE

Test mode fully complies with S-LINK specification. UTDO# line is sampled at link reset.

12. FLOW CONTROL

The Read out buffer size can be calculated from the formula given in [1]:

$$RBS = \left(\frac{LDC_{rt} + [L \times UFD \times 2] + LSC_{rt}}{DTR} \right)$$

where:

RBS= Read out Buffer size (words)
LDC_{rt}=LDC reaction time to transmit XOFF after UXOFF# goes low (ns)
LSC_{rt}=LSC reaction time to stop transmitting data after XOFF received (ns)
L= Length of S-LINK fiber (m)
UFD=Unit Fiber Delay-time for light to travel 1m in fiber (~6ns/m)
DTR=Data Transfer Time (ns/word)

Data words in LSC and LDC pipelines are included in LSC_{rt} and LDC_{rt} respectively.

Symbol	Single ODIN	Double ODIN
LDC_{rt}	350	550
LSC_{rt}	200	300
UFD	6	6
DTR	31.25	25

Table 12-1 Flow control parameters

The values for the ODIN boards are given in Table 12-1, which yields the formulas:

$$RBS_d = 20 + \frac{5L}{13} \qquad \text{(Single ODIN)}$$

$$RBS_d = 40 + \frac{L}{2} \qquad \text{(Double ODIN)}$$

13. RETURN LINES

Return Lines are functional during data transfer and in test mode. LRL[3..0] lines will stay unaltered when the link is down. An internal parity checking logic ensures proper operation of the Return Lines. The sampling rate of the return lines is 8 MHz for the single channel version and 5 MHz for the double channel version.

14. ERROR DETECTION

ODIN features a CRC-based block error detection and errors are reported in the following control word, as specified in [1]. There is also a weak word-by-word error detection, but this only looks at the internal data format and G-Link error bit, and does not look at the actual data

S-LINK control words uses parity bits as error detection in order to separate data errors from control word errors.

15. LINK DOWN FUNCTION

The following events may result the link down signal to be asserted:

1. Reset cycle
2. Self-test mode
3. Local reset, i.e. the LDOWN# is asserted only on the card where URESET# is set low.
4. LSC or LDC is not powered up
5. Broken optical link
6. Fatal error occurred

The three first cases are covered by the S-LINK specifications. In the other cases the link down should be latched until a reset cycle. This is true except on LSC power down as the LSC is powered up in a reset state. On LDC power down, LSC will go down caused by the return channel loosing synchronization. This link down state will be latched until cleared by a reset at either side.

16. KNOWN BUGS

For UCLK in low MHz range, <10 MHz, flow control does not work in Test Mode, as this sometimes will cause a link down. Going out of test mode and perform a link reset clears this state.

REFERENCES

[1] O. Boyle, R. McLaren, E. van der Bij, “The S-LINK Interface Specification”, http://www.cern.ch/HSI/s-link/spec/spec/ CERN, 1997.