Development and Test Results of a Digital Data Transmission System for Liquid Krypton Calorimeter Level 0 Trigger System for the NA62 Experiment at CERN

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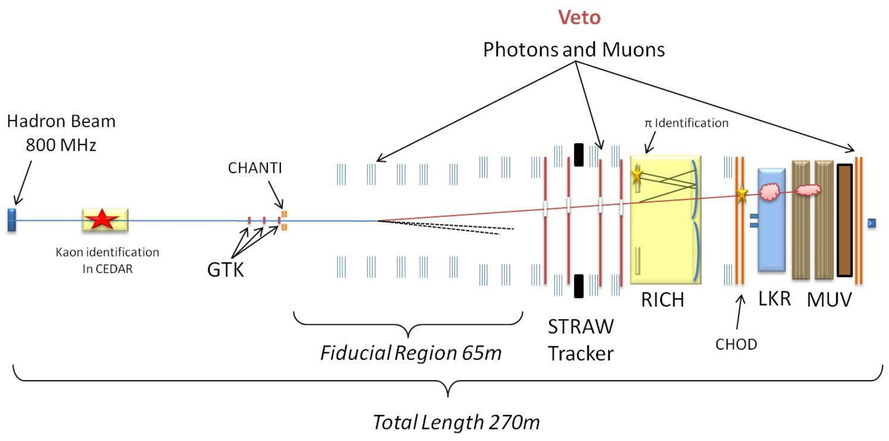
I. NA62 experiment

The NA62 experiment currently being installed at the SPS North Area High-Intensity is composed of several detectors: a differential Cerenkov counter (KTAG), a beam tracker (GTK), a charged particle detector (CHANTI), a STRAW chambers magnetic spectrometer, a photon veto system composed of different detectors (LAV, IRC/SAC, Liquid-Krypton Calorimeter) in the various angular decay regions, a RICH, a charged particle hodoscope (CHOD) and a muon detector (MUV).

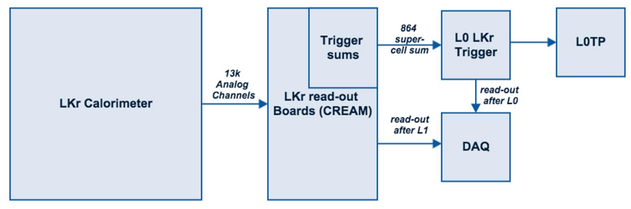


The NA62 detectors at CERN SPS

The Modern high-energy physics experiments, such as the NA62 experiment, require sophisticated trigger systems. A board named "Calorimeter REAdout Module" (CREAM) has been developed by CAEN under the CERN responsibility; **furthermore, mezzanine boards named: "TEL62 DESerializer" (TELDES), TX and RX mezzanines have been developed respectively by the Perugia and Roma Tor Vergata INFN Groups**.

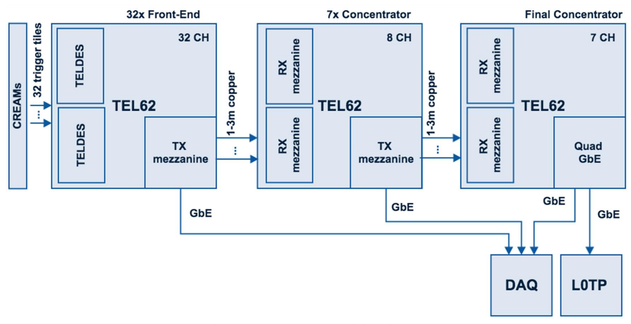
II. Trigger Level 0 Architecture

The LKr L0 trigger continuously receives from the CREAMs 864 Trigger Level Sums (TLS), each one corresponding to a tile of 16 calorimeter cells. The 864 TLSs are transmitted between CREAMs and TELDESs as LVDS signals over shielded high-performance copper twisted-pairs. Besides programmable TLSs, CREAMs provide data buffering, optional zero suppression and 40-MHz 14-bit sampling for all the 13248 calorimeter readout channels.



Block diagram of the LKr L0 trigger

The LKr Calorimeter data are read from the CREAMs, providing TLSs to the LKr L0 trigger, which generates the L0 trigger; furthermore the Data AcQuisition (DAQ) system processes the data, respectively from LKr L0 trigger and CREAMs, after the L0 and L1 triggers are received.

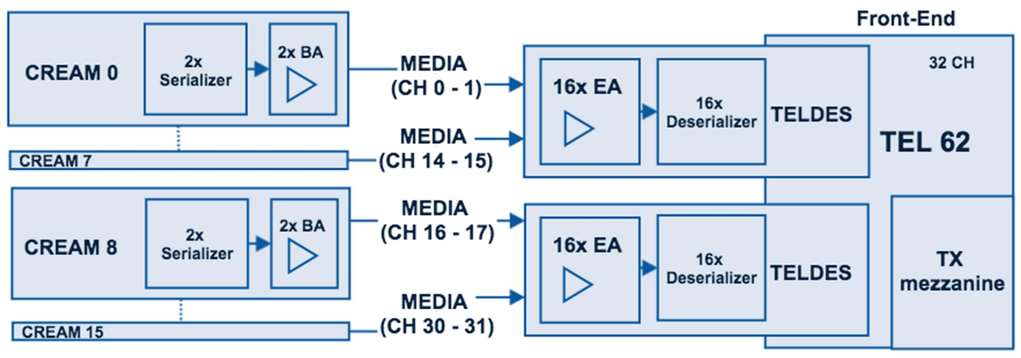


LKr trigger processor block diagram

The LKr trigger processor is a three-layer parallel system, composed of Front-End (FE) and Concentrator boards, both based on the TEL62 boards, equipped with custom dedicated mezzanines (TELDES, TX mezzanine, RX mezzanine), see scheme on left side. Two TELDESs are plugged in each FE board in order to receive 32 TLSs from 16 CREAMs. Data received by the CREAM have to be serialized before the transmission to the TELDES, where are deserialized and, together with the proper sampling clock, delivered to the TEL62 FPGAs.

III. CREAM - TELDES DIGITAL DATA TRANSMISSION DESCRIPTION

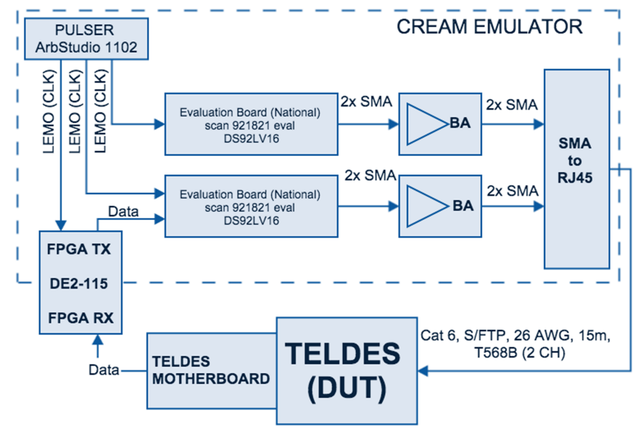
In order to evaluate the link as well as the TELDES characteristics, the INFN groups have developed a fully dedicated test set-up, including electronic test boards for CREAM and TEL62 interface emulators. A specific test protocol has been so developed to investigate the reliability and the performance of both data-link and TELDES.



CREAM-TELDES LVDS Link

To guarantee the performance needed, whereas saving in term of system cost, COTS (Commercial Off-The-Shelf) chips have been used for the data link-between CREAM and TELDES. **Serializer/deserializer** (SER/DES) DS92LV16 chip has been chosen, in conjunction with DS15**BA**101 and DS15**EA**101, a cable extender chipset. Each TELDES, as shown in the upper scheme, receives LVDS signals from 8 CREAMs, equalizes them by means of DS15EA101, and deserializes them using the DS92LV16. The resulting 32 calorimeter tiles are then delivered to the FE FPGAs in order to extrapolate the peak information.
The serial data-stream is organized in 18-bit words, containing the digitized data from the calorimeter readout channels. Each word includes a start bit and a stop bit appended by the serializer, framing sixteen data bits. In our case since the *TCLK* is 40 MHz, the serial rate is 720 Mbps whereas the data throughput is 640 Mbps for each link between CREAM and TELDES. The deserializer monitors the incoming embedded clock to determine lock status and will indicate loss of lock by lowering the negative *LOCK* output.
Experimental tests done in the DAQ room at NA62 CERN SPS North Area show that the behaviour of the *LOCK* signal of the deserializer is strongly dependent on EMI. A significant reduction of the phenomenon is obtained only by using a particular type of Cat. 6 cable (S/FTP, 26AWG). A test to monitor the losses of the deserializer *LOCK* and the PER over a period of at least 20 hours has been developed and executed.

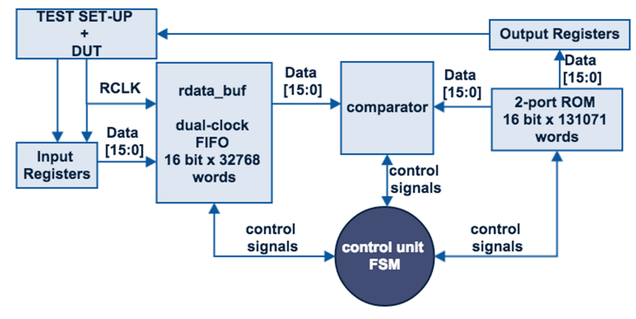
IV. TEST SET-UP



Schematic Test Set-up

Schematic Test Set-up is shown on the left: data generated inside the FPGA, are sent to the Evaluation Board; they are then buffered and sent over a 15 m Cat.6 cable complying with TIA/EIA T568B. The data are received from the DUT and sent back to the FPGA, which carries out the comparisons needed to estimate the PER.

In order to carry out the desired measurements, which include PER, deserializer lock losses, and long-term test, a firmware has been developed. The block diagram is shown in the lower scheme.

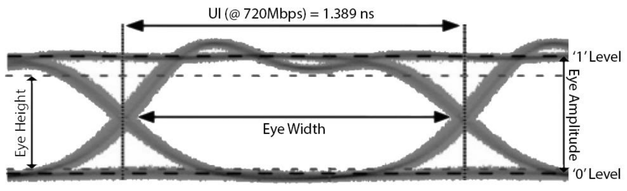


Block diagram of the DE2-115 FPGA Firmware

In addition to sending PRBS words, the firmware also receives words from the TELDES motherboard; data passes through a dual-clock FIFO, which synchronizes the recovered clock domain to the internal one. Every bit of the received words is compared to the related bit of the sent words, and if this is different, a counter is increased. Once the comparison ends, the PER is shown together to the BER obtained by summing all the values of the counters.

Eye diagram measurements are also taken by means of an active differential probe. A pass-fail mask, based on the deserializer acceptance window has been defined as shown in the first figure in the test results.

V. TEST RESULTS



Measured parameters on the eye diagram

The PER of the CREAM-TELDES data-link is an essential parameter to validate the system performance since it could invalidate the LKr L0 trigger accuracy. **The maximum acceptable trigger error rate is 10^{-2} .**

Considering all the 864 channels as independent, and that one wrong word invalidates the trigger, the trigger error rate is a binomial random variable. The maximal acceptable PER for a single channel is therefore $1.16 \cdot 10^{-5}$.
Due to the relevant number of channels to be validated, the channel test time has to be as short as possible. The number of words to be evaluated are calculated considering each word independent from the others and received with a certain, unknown, PER: under such hypothesis the received words can be considered as a sum of binomial random variables. When the number of sent words is high and the PER is small enough, a binomial random variable can be approximated with a Poisson's one.
The probability to observe zero errors when receiving n words is then:

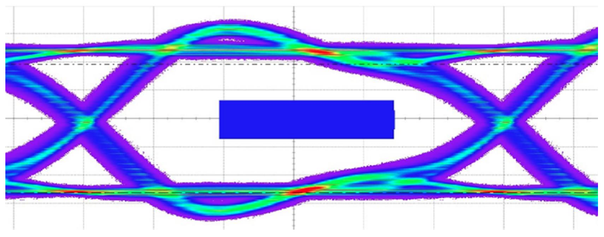
$$prob\,(\varepsilon = 0) = p_n(0) = \binom{n}{0} p^0 (1-p)^{n-0} = (1-p)^n$$

The confidence level (CL), defined as the probability that the PER is lower than γ, given n, can be then calculated as:

$$CL = 1 - prob(\varepsilon = 0) = 1 - (1-p)^n.$$

From that equation the number n can be now calculated from CL = 0.99 and $\gamma = 6 \cdot 10^{-9}$. Note that the γ value is smaller than the needed one: such value has been chosen because the testing time (40 seconds per channel) is reasonable and yet reaches an acceptable confidence level for the PER.

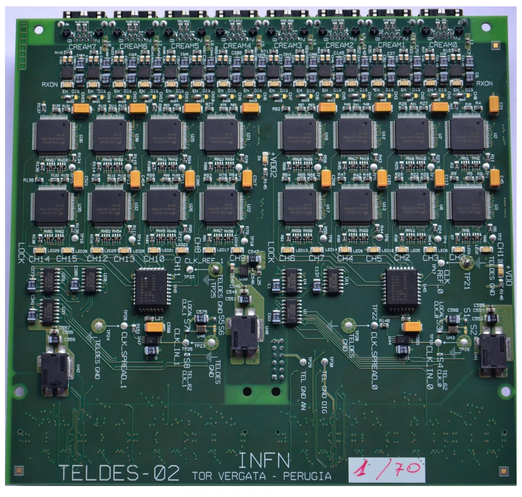
Among the 70 TELDESs tested for PER it has been calculated that all the board results are within the limit.
Moreover also a long-term test, lasting 20 hours, has been performed on all the channels of two TELDESs.
The average number of errors is 14, which achieves a PER lower than $8.42 \cdot 10^{-12}$ with a CL of 0.99.
The values measured from one of the typical eye diagrams are shown in the right side picture :



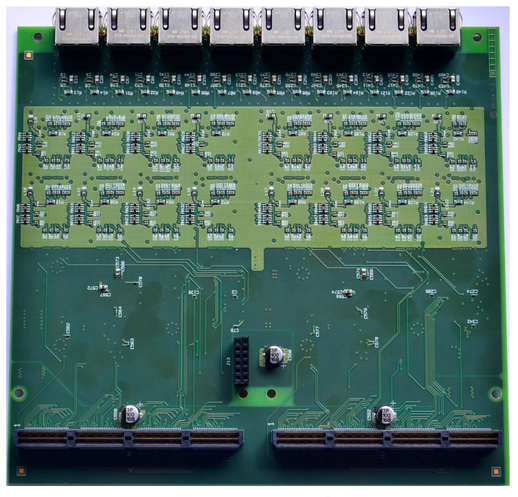
Eye Diagram obtained on the deserializer input. Note that the blue pattern is the mask, which has not been crossed by the waveform.

VI. CONCLUSION

The LVDS digital data-link used inside the Level 0 Trigger system for the Liquid Krypton Electromagnetic Calorimeter of the NA62 experiment has been developed. The TELDES production boards have been tested as well as the integration phase inside the experiment has been concluded.
A test set-up has been realized and used to extensively test the 70 TELDES boards.



TELDES Top View



TELDES Bottom View

The performance of the boards is tested and data have successfully transferred in the experimental area at 40 Mhz clock rate.

All results indicate that the performance satisfies the requirements of the NA62 experiment.

The novelty is in that the proposed digital data transmission, even if is operative in a harsh high-energy physics experiment, is fine. If one were to transfer LVDS digital data between 2 systems tens of meters away, using the selected COTS (in the environment cited above) the guarantee of a robustness of the high-speed link should become possible.