The Trigger System for $K^0 \to \pi^0\pi^0$ Decays of the NA48 Experiment at CERN

Ivan Mikulec
Institut für Hochenergiephysik,
Vienna, Austria

CERN - PISA - VIENNA

Objective of the NA48 experiment

To measure the direct CP-violation parameter

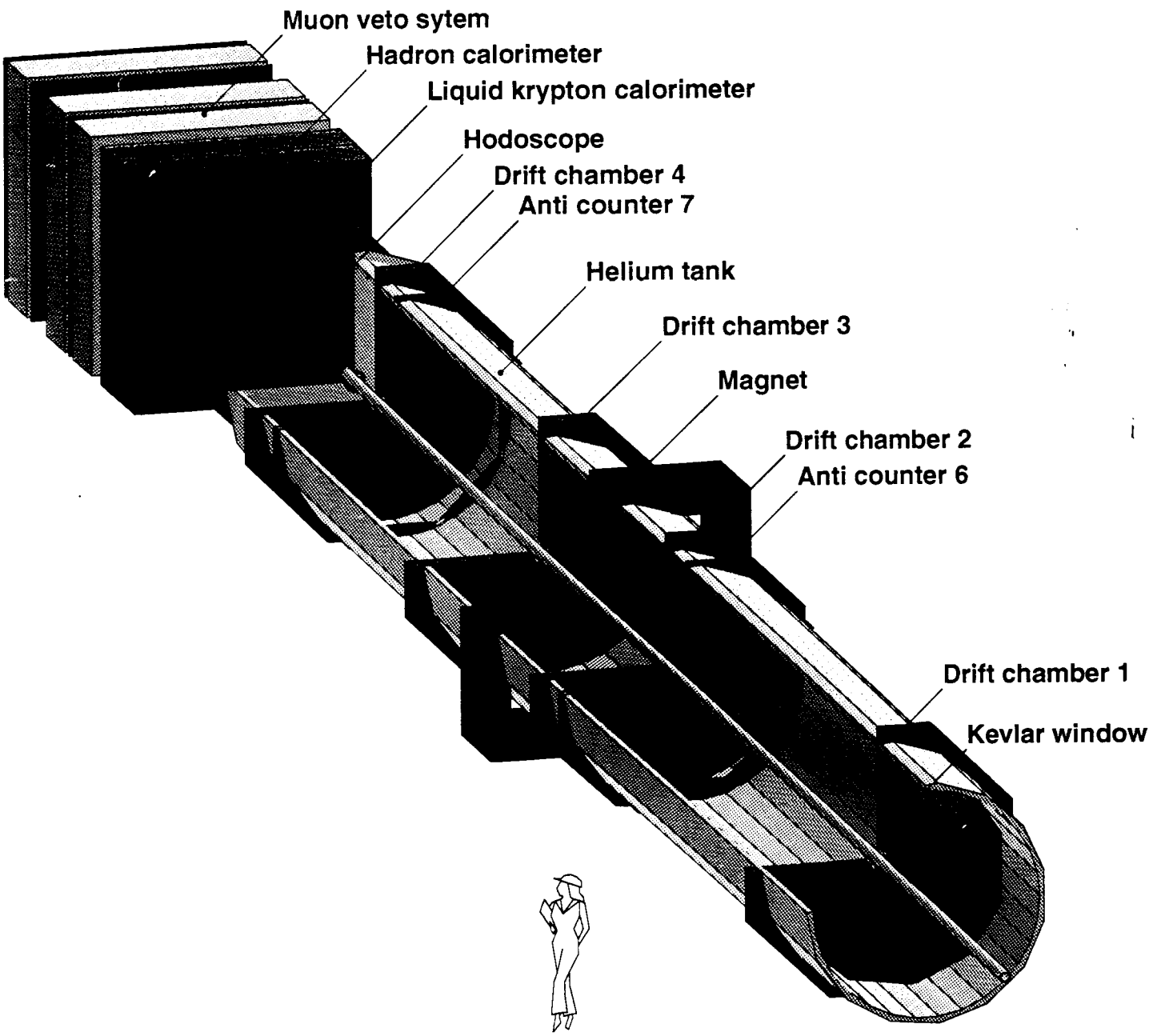
$$Re\frac{\varepsilon'}{\varepsilon} \approx \frac{1}{6}\left\{1 - \frac{K_L \to \pi^0\pi^0}{K_S \to \pi^0\pi^0} \Big/ \frac{K_L \to \pi^+\pi^-}{K_S \to \pi^+\pi^-}\right\}$$

with accuracy $2\text{x}10^{-4}$

☛ Low systematic error:
simultaneous K_L and K_S beam

☛ Low statistical error:
high beam intensity $1.5\text{x}10^{12}$ ppp of SPS

challenge for the trigger


Muon veto sytem
Hadron calorimeter
Liquid krypton calorimeter
Hodoscope
Drift chamber 4
Anti counter 7
Helium tank
Drift chamber 3
Magnet
Drift chamber 2
Anti counter 6
Drift chamber 1
Kevlar window

NA48 Trigger System

Hardware Trigger

Neutral ($\pi^0\pi^0$) - LKr calorimeter

Charged($\pi^+\pi^-$) - Spectrometer
Hodoscope
Hadron calorimeter

Software Trigger

Neutral ($\pi^0\pi^0$) Trigger

Objective:

> 99% efficiency

~ 1 kHz rate

Background:

$K_L \to \pi^0\pi^0\pi^0$	$\sim 220 \times K_L \to \pi^0\pi^0$
$K_L \to \pi e \nu$	$\sim 340 \times K_L \to \pi^0\pi^0$
$K_L \to \pi^+\pi^-\pi^0$	$\sim 125 \times K_L \to \pi^0\pi^0$

Accidental activity

Decision based on reconstruction of

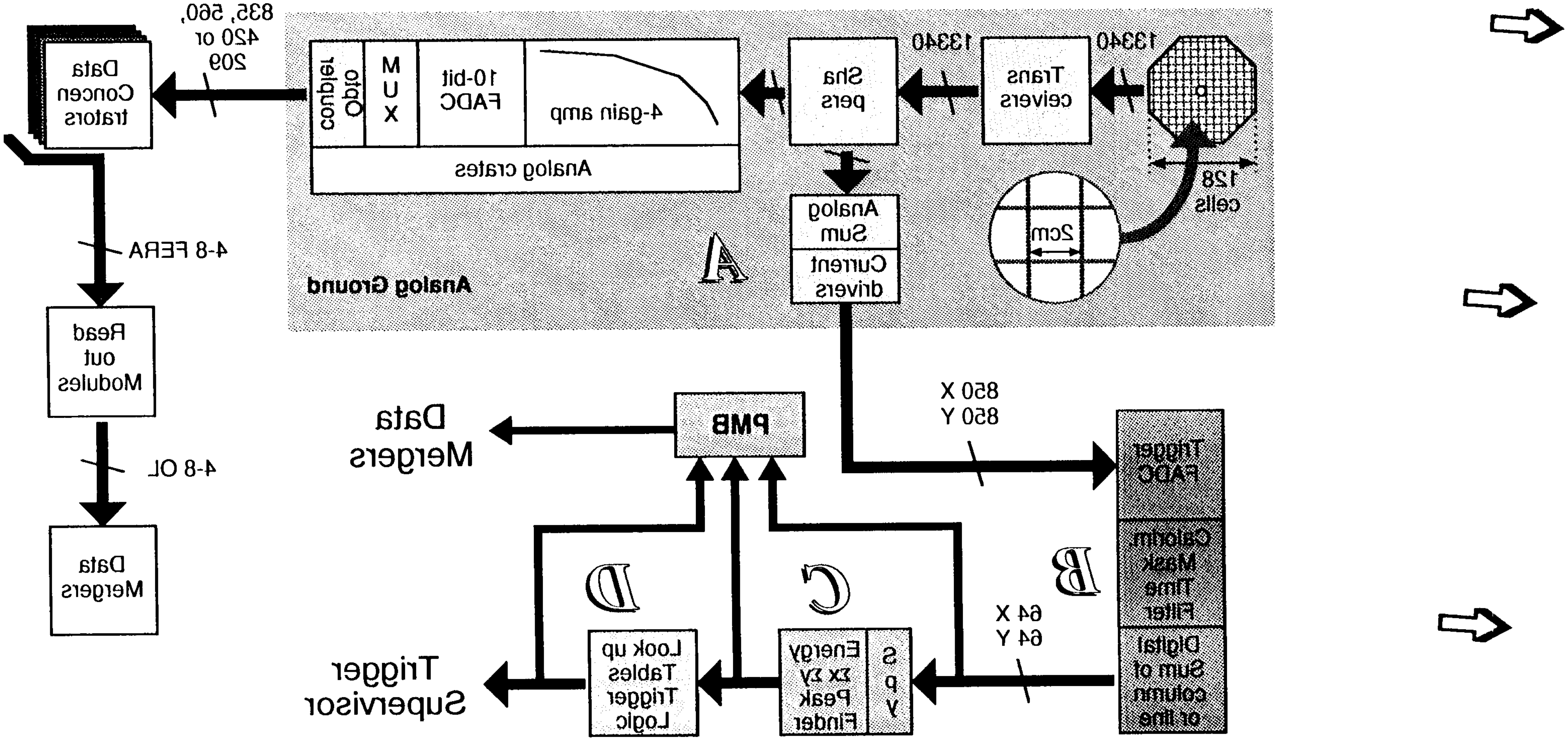
Total energy

Energy center of gravity

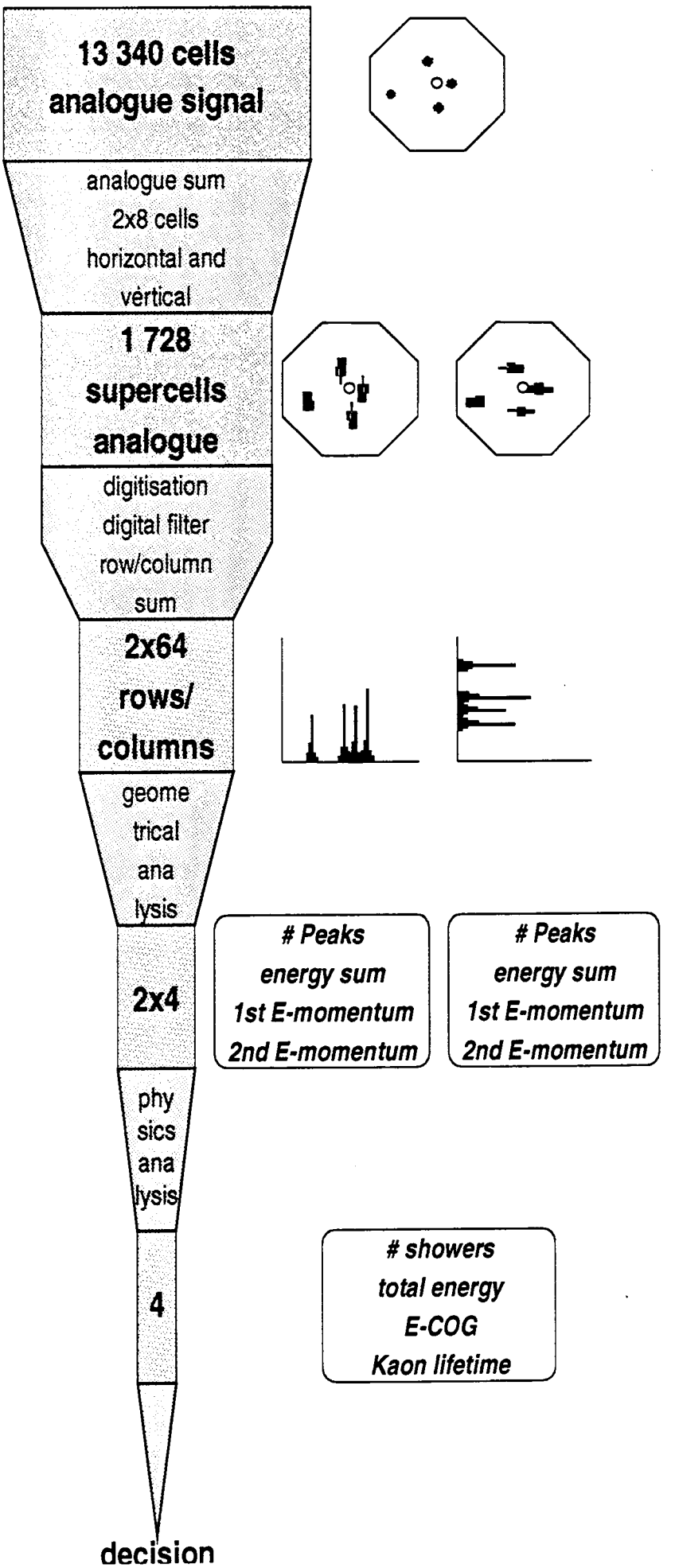
Kaon lifetime

Number of showers

in <100 μs every 25 ns in pipeline



Trans ceivers
Sha pers
13340
13340
128 cells
2cm
Analog Sum
Current drivers
4-gain amp
10-bit FADC
M U X
Opto coupler
Analog crates
Analog Ground
A
835, 560, 420 or 209
Data Concen trators
4-8 FERA
Read out Modules
4-8 OL
Data Mergers
850 X
850 Y
Trigger FADC
Calorim. Mask Time Filter
Digital Sum of column or line
B
64 X
64 Y
PMB
Data Mergers
S p Y
Energy Σx Σy Peak Finder
C
Look up Tables Trigger Logic
D
Trigger Supervisor


13 340 cells
analogue signal
analogue sum
2x8 cells
horizontal and
vertical
1 728
supercells
analogue
digitisation
digital filter
row/column
sum
2x64
rows/
columns
geome
trical
ana
lysis
2x4
phy
sics
ana
lysis
4
decision
Peaks
energy sum
1st E-momentum
2nd E-momentum
Peaks
energy sum
1st E-momentum
2nd E-momentum
showers
total energy
E-COG
Kaon lifetime

CPD
(Calorimeter Pipelined Digitizer)

216 FASTBUS modules
> 13.10^3 channels

Main task

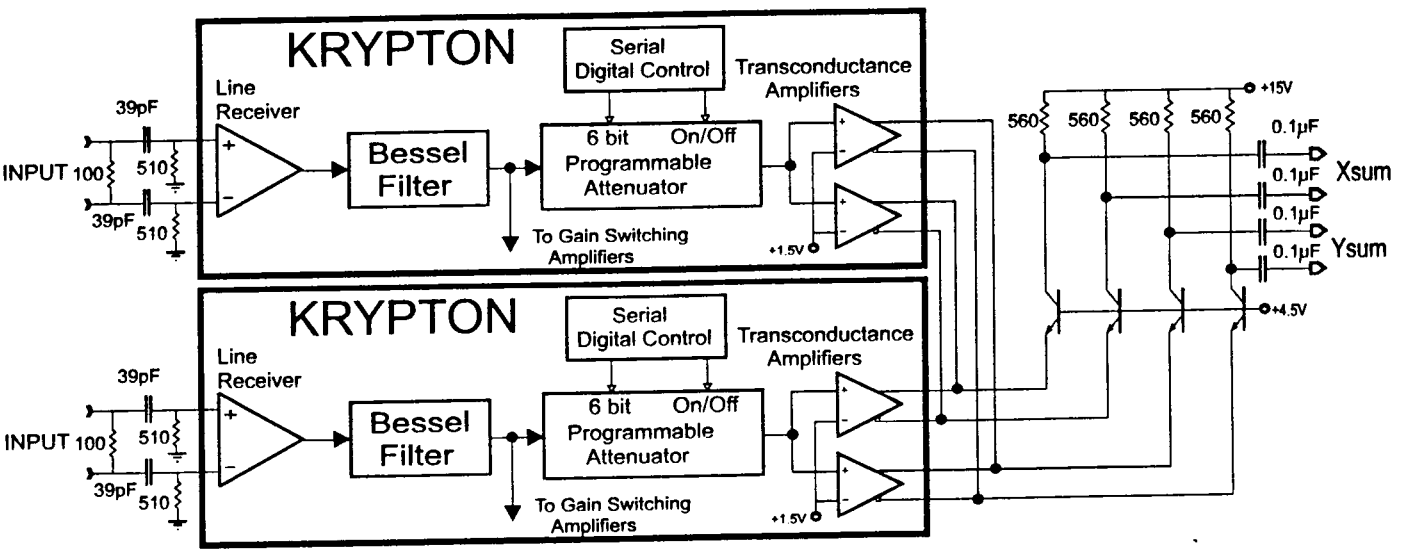
- LKr calorimeter read out

But also

- Build 2x8 cells analogue sums for the trigger
- Transmit this signal to the trigger electronics

Trigger output signal

- Differential [redacted] V_{pp}=1V (~100 GeV)
- Customized auxiliary FASTBUS backplane reorders signals such way that no additional patch panel is needed



VFM
(Vienna Filter Module)

64 VME modules 9U
> 1700 channels

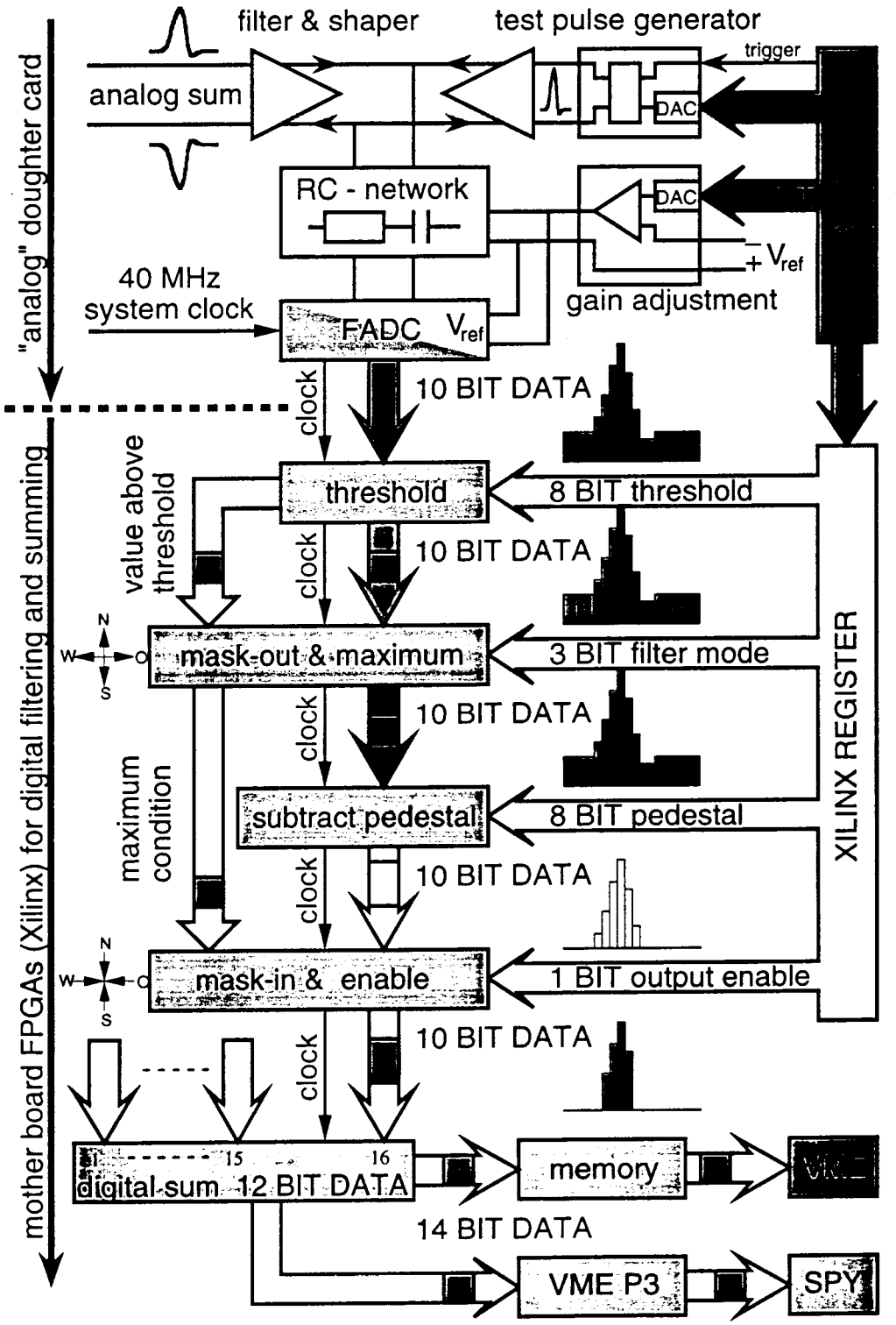
3 tasks

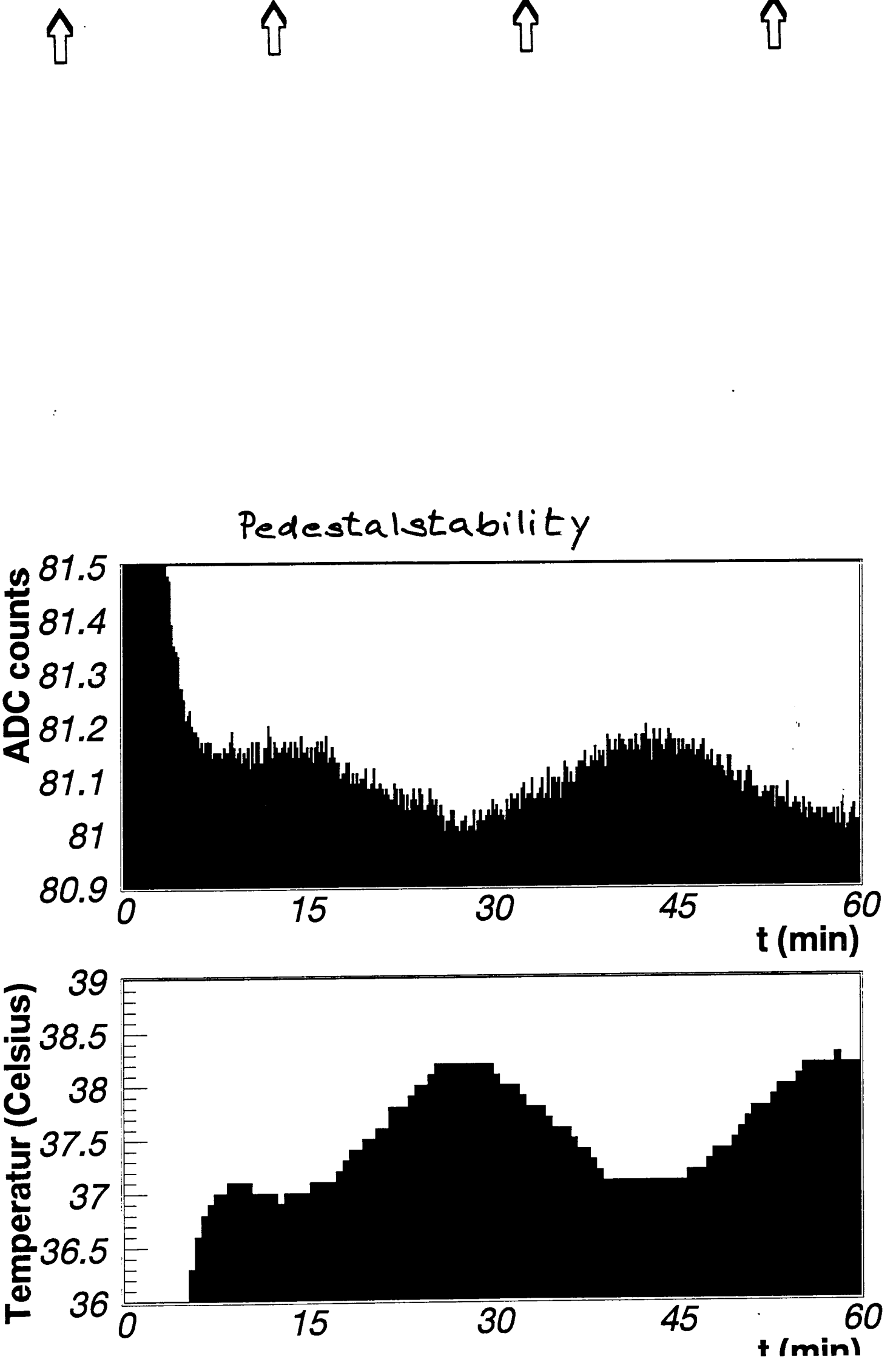
1	Digitizing	10-Bit FADC (32/module)
2	Filtering	8 Xilinx chips/module
3	Summing	2 Xilinx chips/module

Features

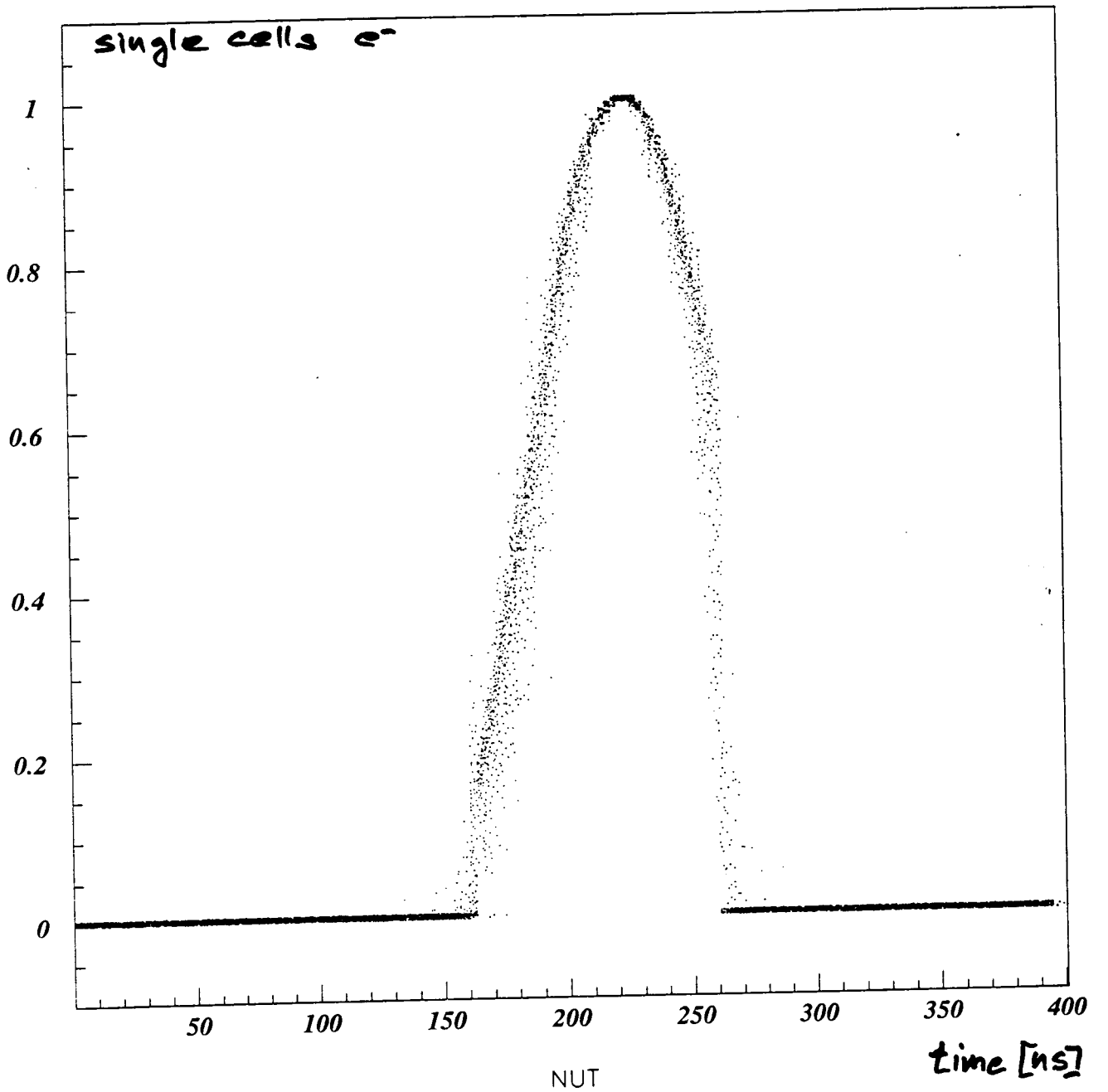
- ☛ Fully configurable over VME
- ☛ Analogue and digital part fully separated
- ☛ Stand-alone testing facilities
- ☛ Highly synchronous clock distribution
- ☛ Components on both sides of the board
- ☛ Optional algorithm to compensate for energy loss
- ☛ Small temperature dependence ~0.1 LSB/K

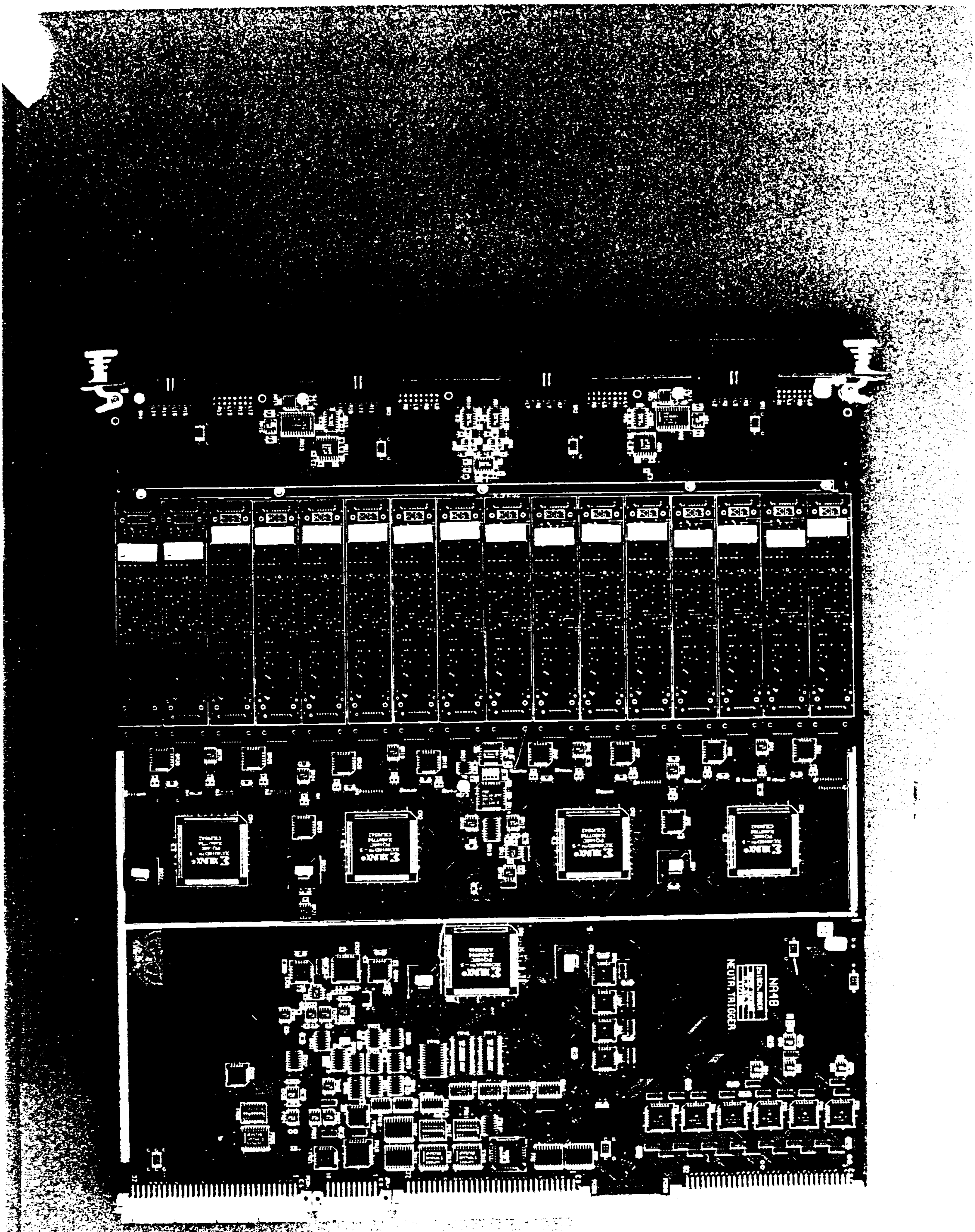
noise $\lesssim 1$ LSB/2×8 cells


filter & shaper
test pulse generator
trigger
analog sum
DAC
RC - network
DAC
V_{ref}
40 MHz
system clock
FADC V_{ref}
gain adjustment
"analog" doughter card
clock
10 BIT DATA
threshold
8 BIT threshold
value above
threshold
clock
10 BIT DATA
mask-out & maximum
3 BIT filter mode
clock
10 BIT DATA
maximum
condition
subtract pedestal
8 BIT pedestal
clock
10 BIT DATA
mask-in & enable
1 BIT output enable
XILINX REGISTER
clock
10 BIT DATA
digital-sum 12 BIT DATA
memory
14 BIT DATA
VME P3
SPY
mother board FPGAs (Xilinx) for digital filtering and summing


Pedestalstability
ADC counts
81.5
81.4
81.3
81.2
81.1
81
80.9
0
15
30
45
60
t (min)
Temperatur (Celsius)
39
38.5
38
37.5
37
36.5
36
0
15
30
45
60
t (min)

Pulse shape seen by NUT after Filter





PSS
(Peak Sum System)

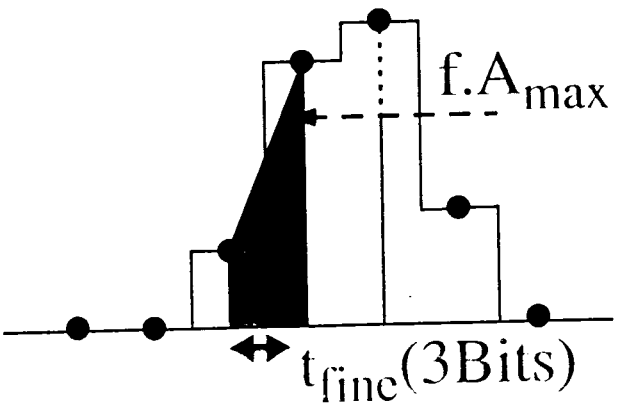
9U VME:
32 Spy modules
16 Peak Sum modules
2 Final Recombinator modules

Tasks

- Monitoring (Spy)
- Build ΣE, ΣEx, ΣEx^2 in 2 views
- Find peaks in space and time

Features

- Fine time (3ns) peak counting using a leading edge interpolation



LUT
(Look-Up Table System)

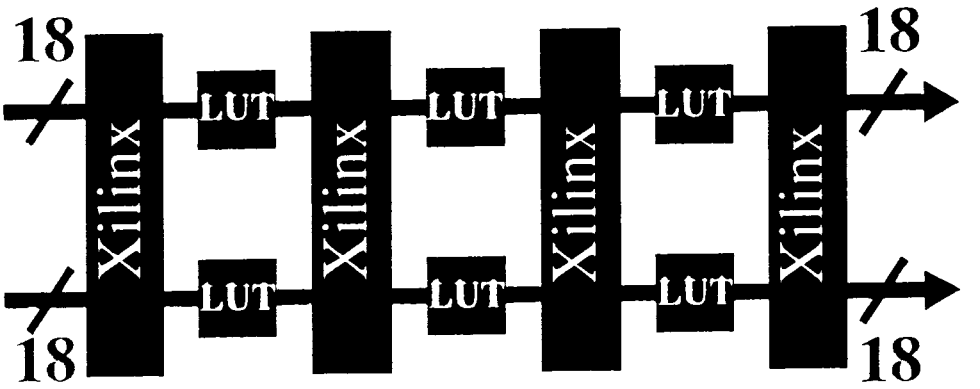
8 FASTBUS modules

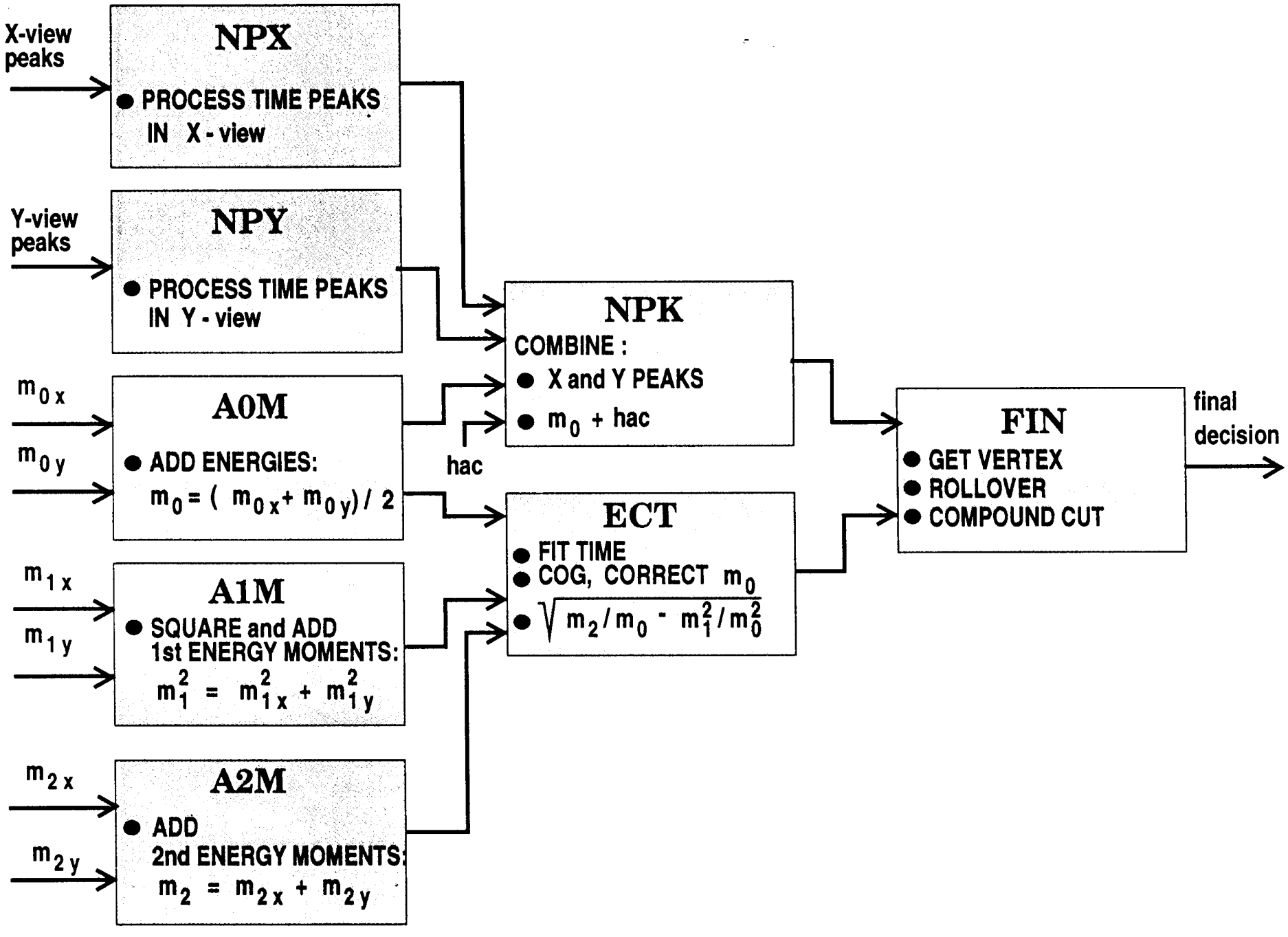
Tasks

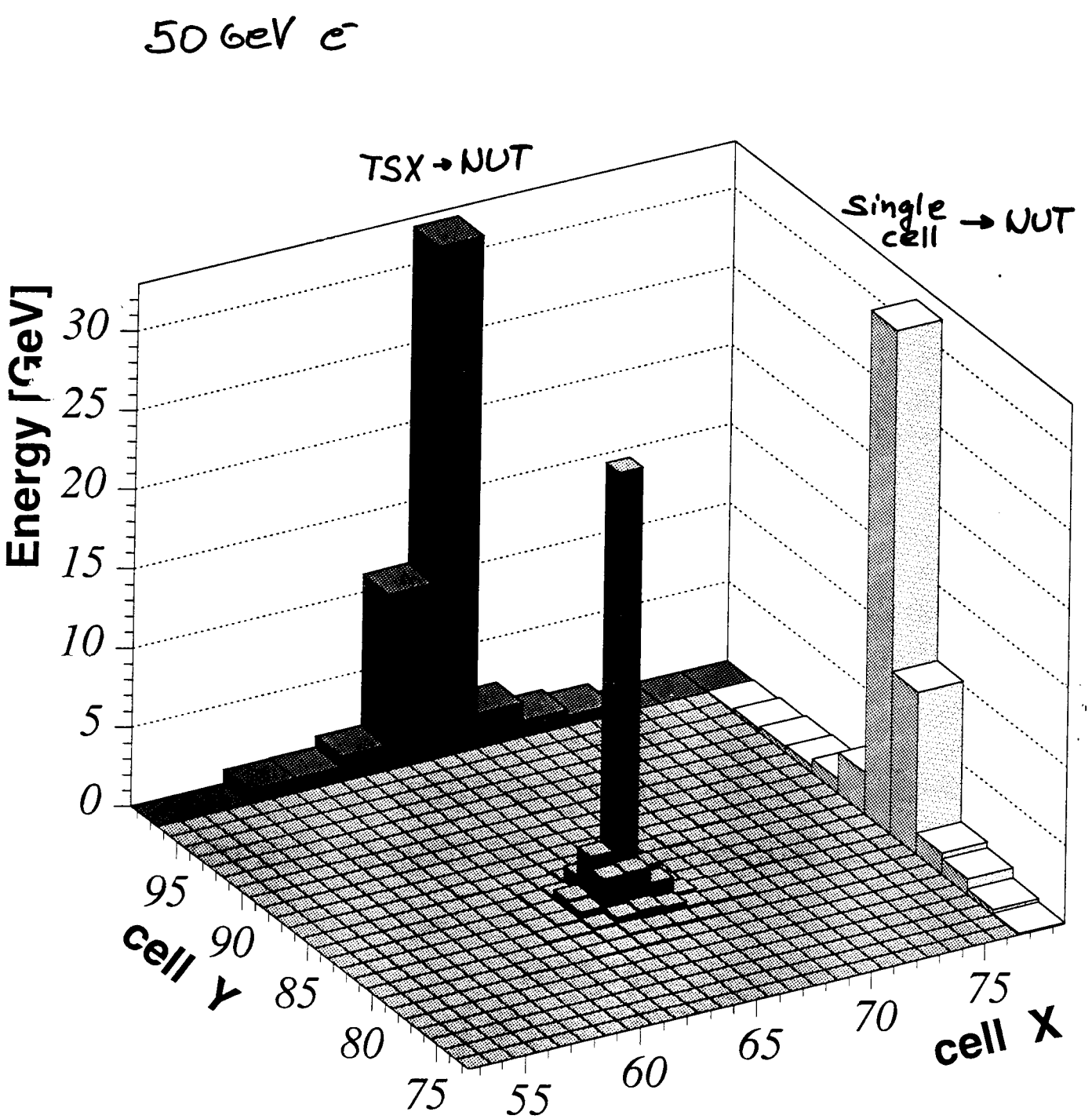
- Compute observable quantities
- Apply thresholds

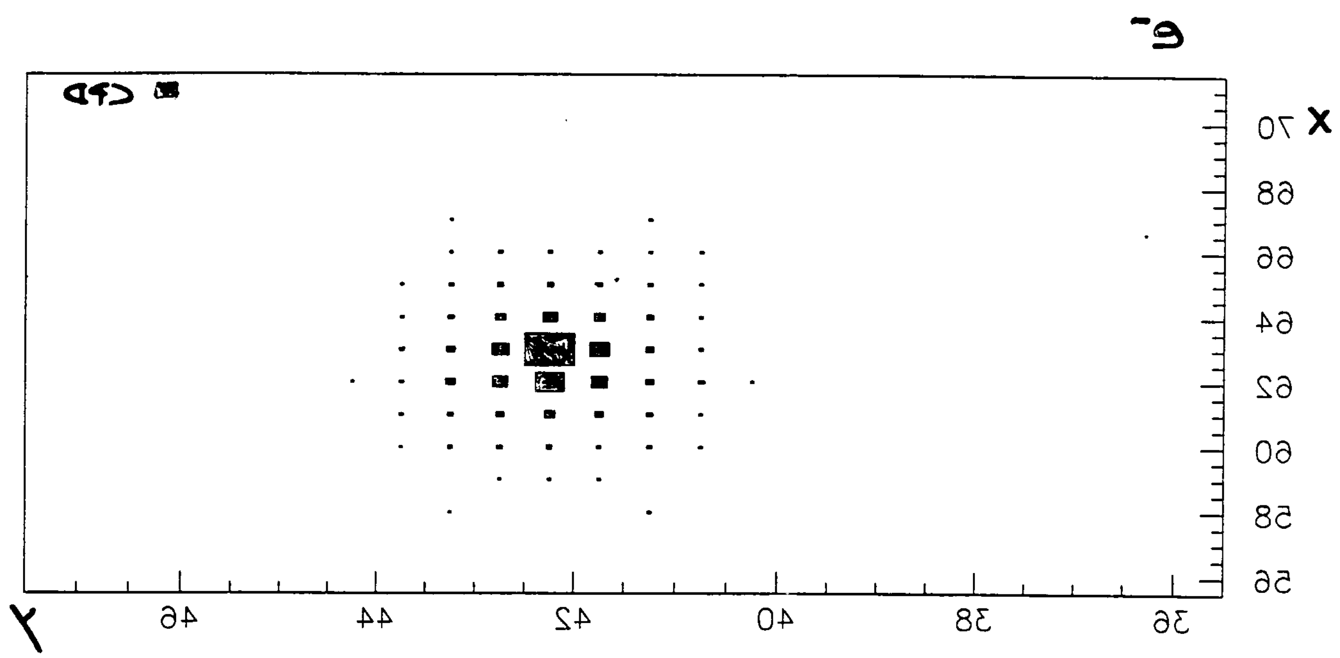
Features

- High flexibility achieved using a system of LUT memories and FPGA chips

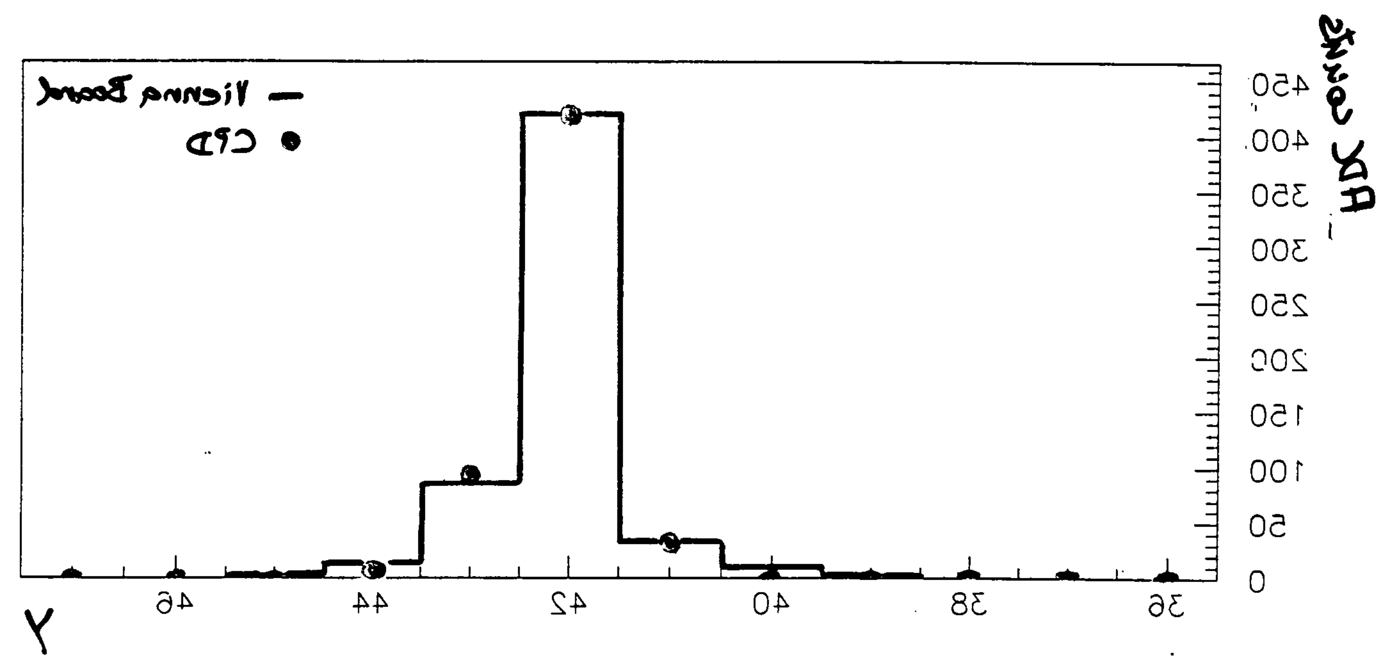



X-view peaks
NPX
PROCESS TIME PEAKS IN X - view
Y-view peaks
NPY
PROCESS TIME PEAKS IN Y - view
m_{0x}
m_{0y}
A0M
ADD ENERGIES:
$m_0 = (m_{0x} + m_{0y}) / 2$
hac
m_{1x}
m_{1y}
A1M
SQUARE and ADD 1st ENERGY MOMENTS:
$m_1^2 = m_{1x}^2 + m_{1y}^2$
m_{2x}
m_{2y}
A2M
ADD 2nd ENERGY MOMENTS:
$m_2 = m_{2x} + m_{2y}$
NPK
COMBINE :
X and Y PEAKS
m_0 + hac
ECT
FIT TIME
COG, CORRECT m_0
$\sqrt{m_2/m_0 - m_1^2/m_0^2}$
FIN
GET VERTEX
ROLLOVER
COMPOUND CUT
final decision


50 GeV e⁻
TSX → NUT
Single cell → NUT
Energy [GeV]
30
25
20
15
10
5
0
95
90
85
80
75
cell Y
55
60
65
70
75
cell X



e⁻
CPD
X
70
68
66
64
62
60
58
56
Y
46
44
42
40
38
36



Vienna Board
CPD
ADC counts
450
400
350
300
250
200
150
100
50
0
Y
46
44
42
40
38
36

2π° candidate