The TDCPix ASIC: Tracking for the NA62 GigaTracker

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5th June 2014

Introduction to NA62 and the GigaTracker

The TDCPix Chip Architecture

Measured Performance
- Pixel Jitter
- TDC Performance
- Full Chain Performance

Summary

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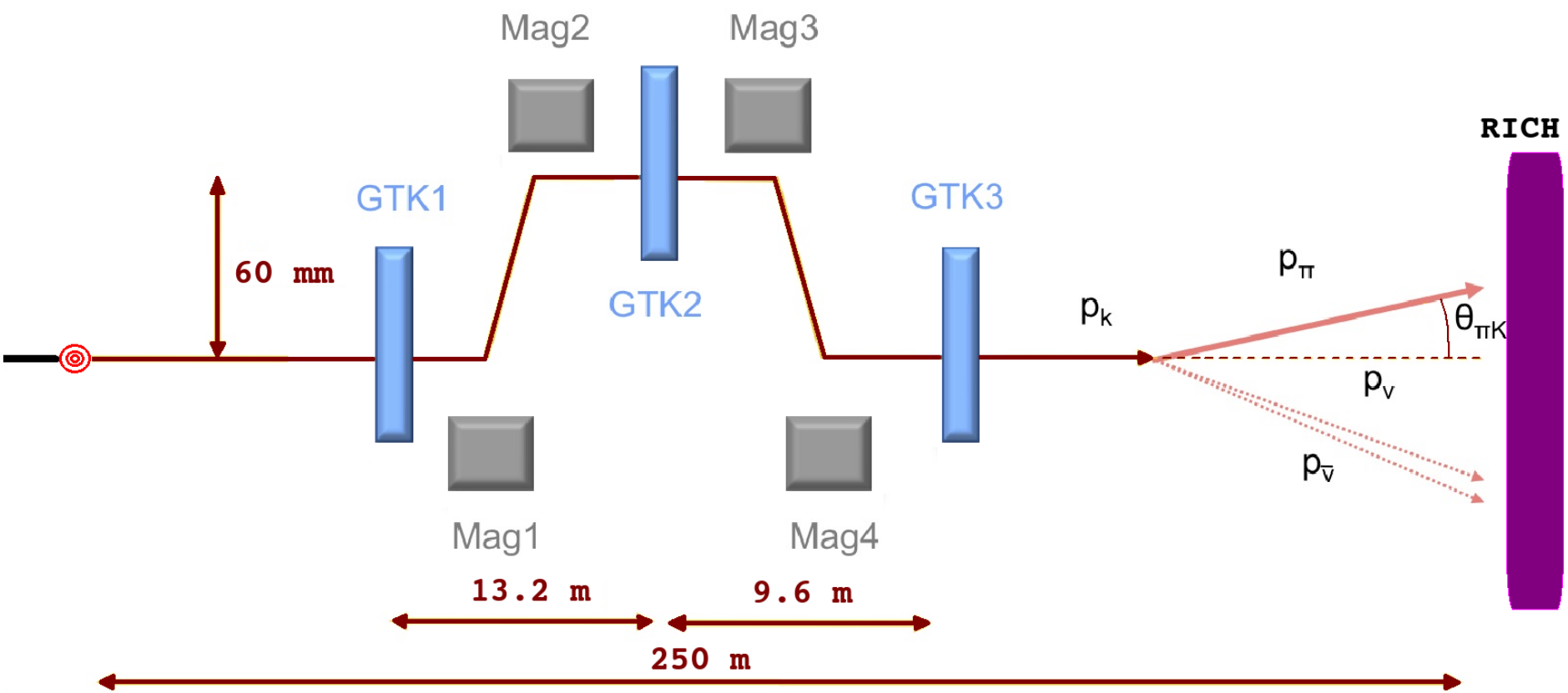
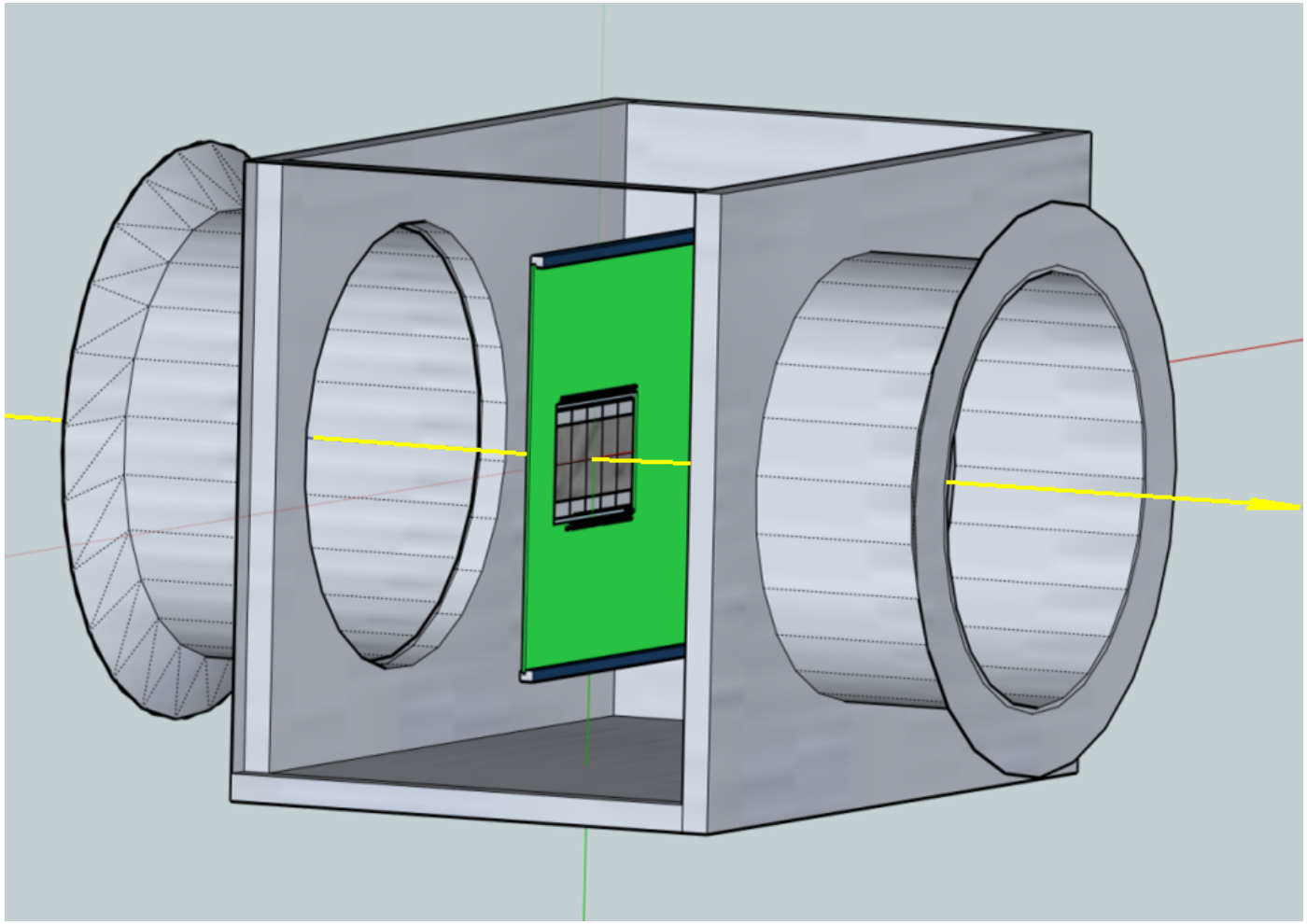
The NA62 Experiment



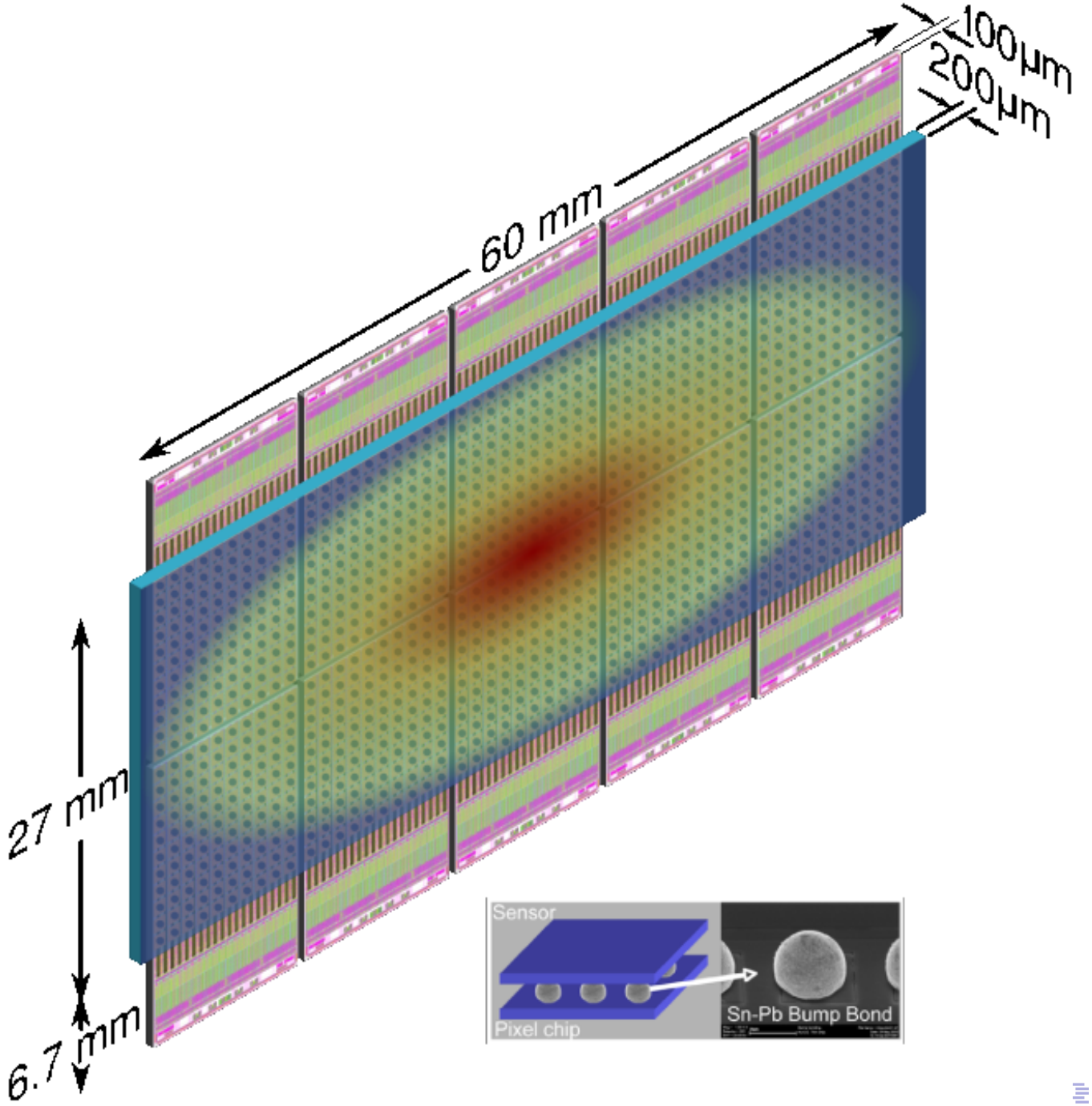
- Trajectory
  - momentum
  - angle
- Time
  - correlate hits with RICH
  - $\leq 200\,ps(RMS)$ per station

GTK Station in the Beam Line

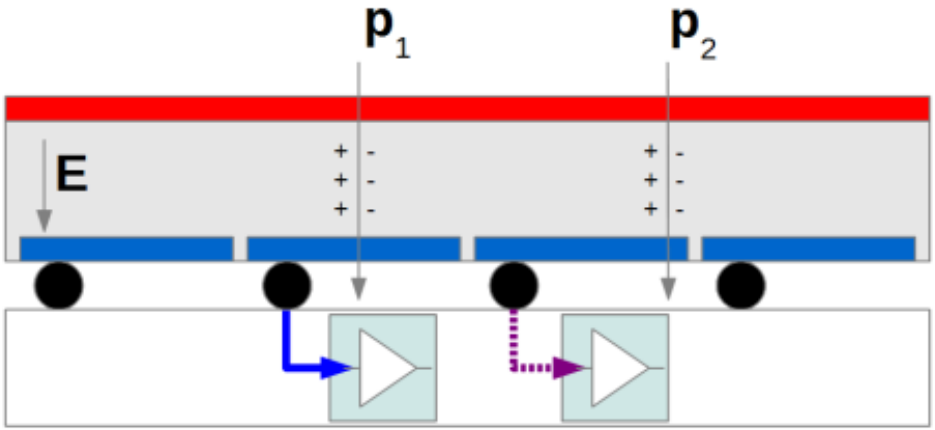


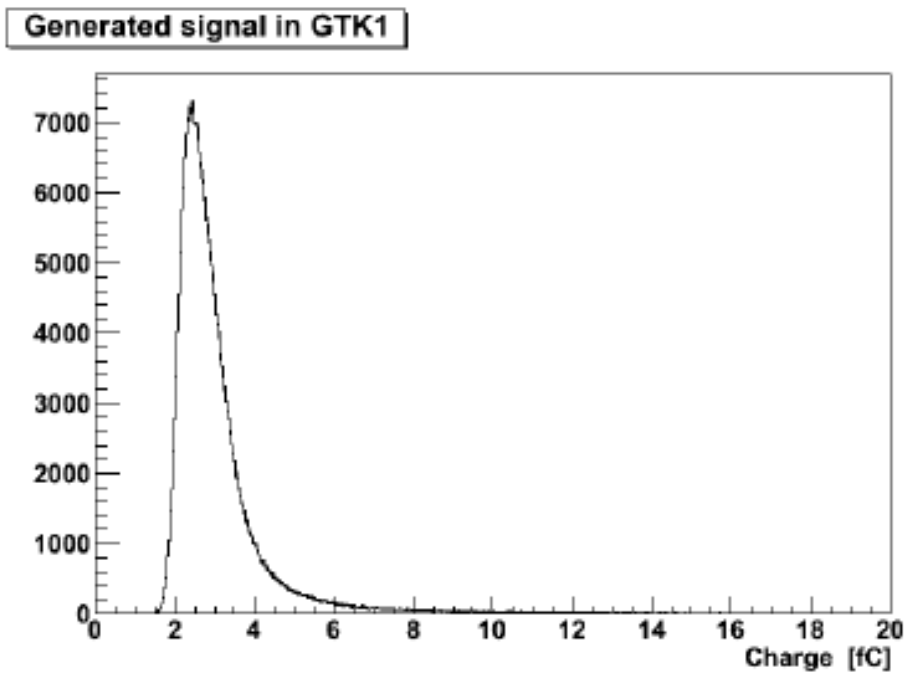
- in vacuum
- centred on the beam
- 0.8→1 GHz beam rate

GigaTracker: Hybrid Pixel Detector



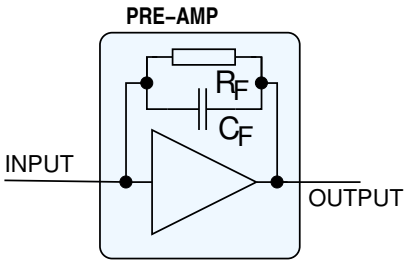
Principle Of Sensor Operation

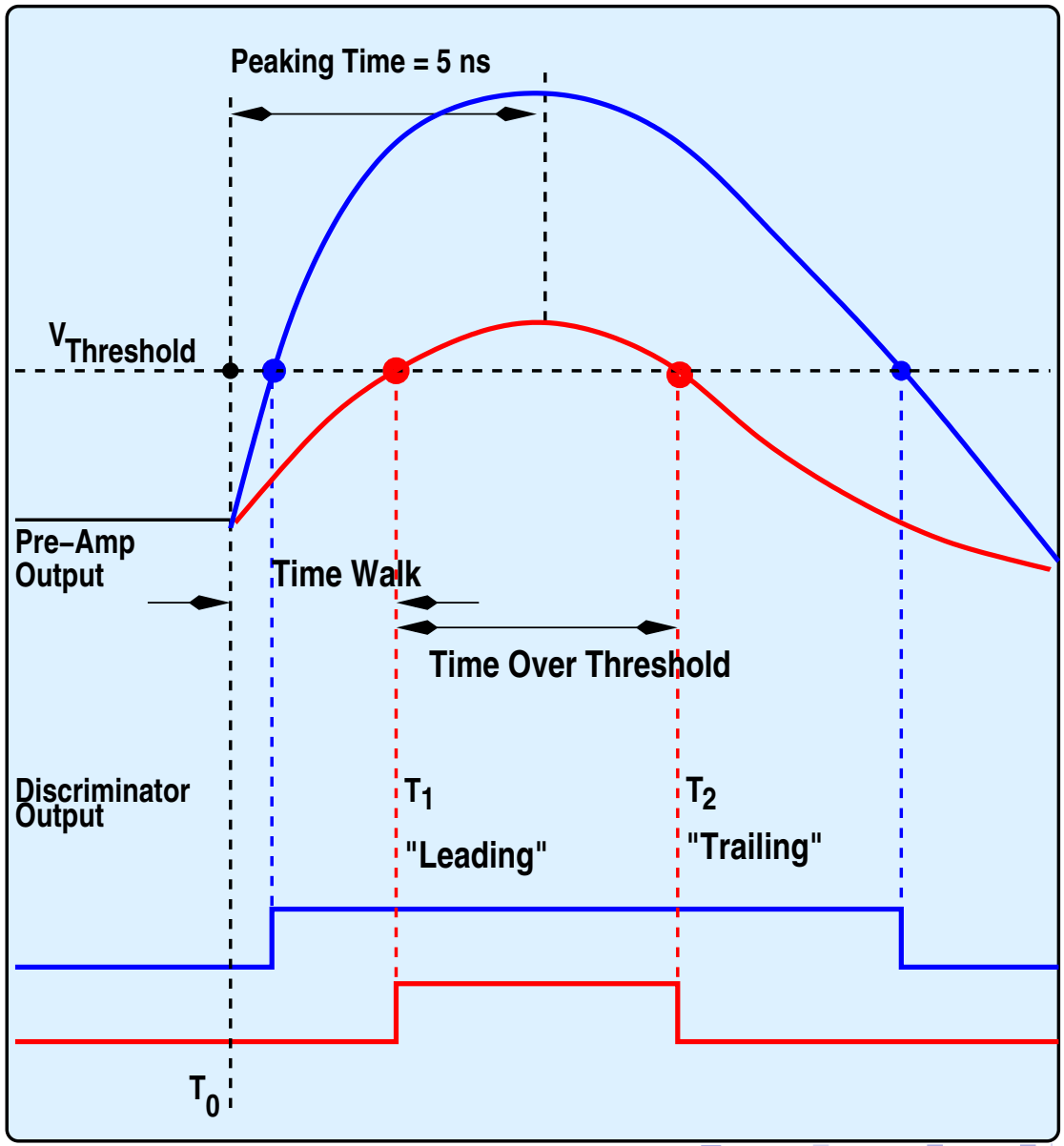




- $V_{bias} \sim$ 300-600V
- charge release mechanism is stochastic
- Landau distribution
  - $Q_{MP} = 2.4\,fC$
- $1\,fC \leq Q \leq 10\,fC$
- Segmented electrodes give spatial information
- Thickness: $200\mu m$

Pre-Amplifier & Discriminator Signals





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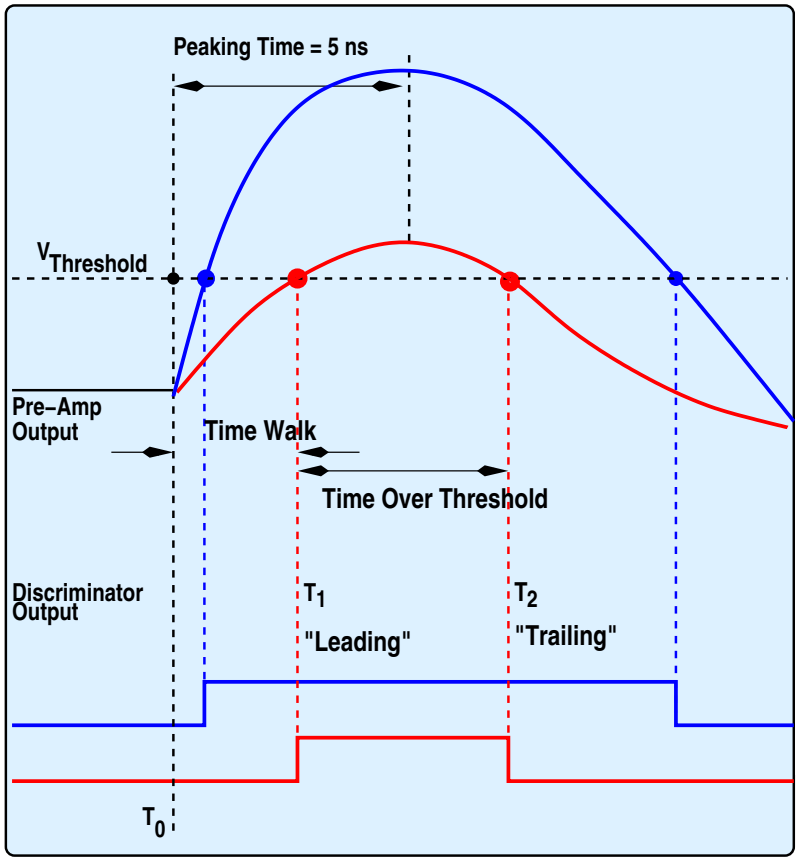

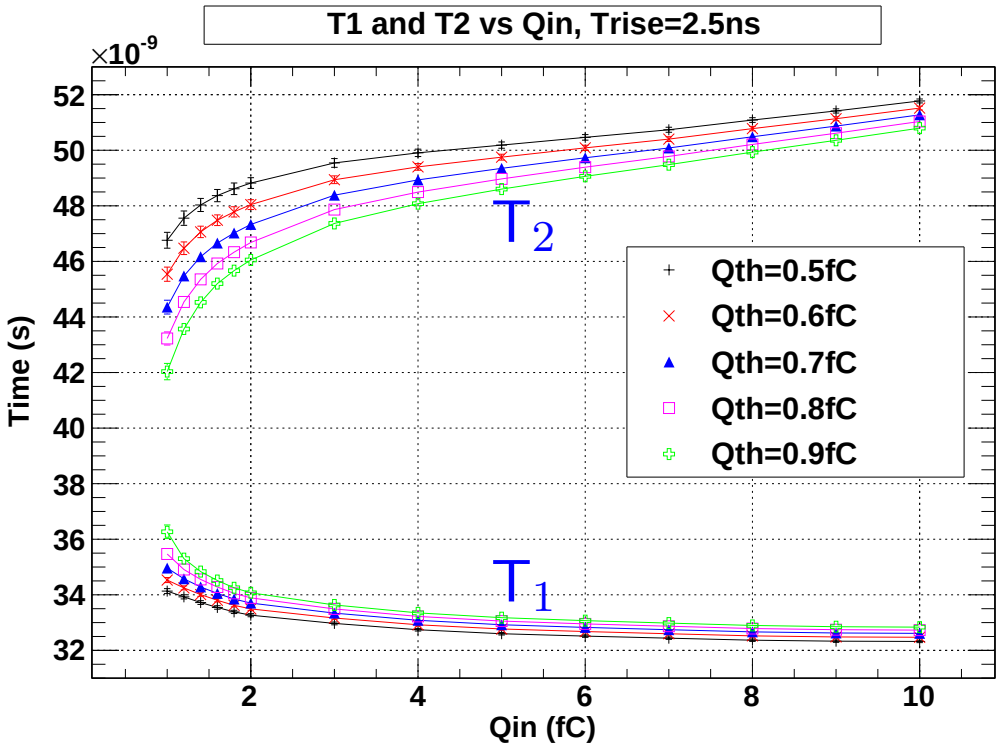

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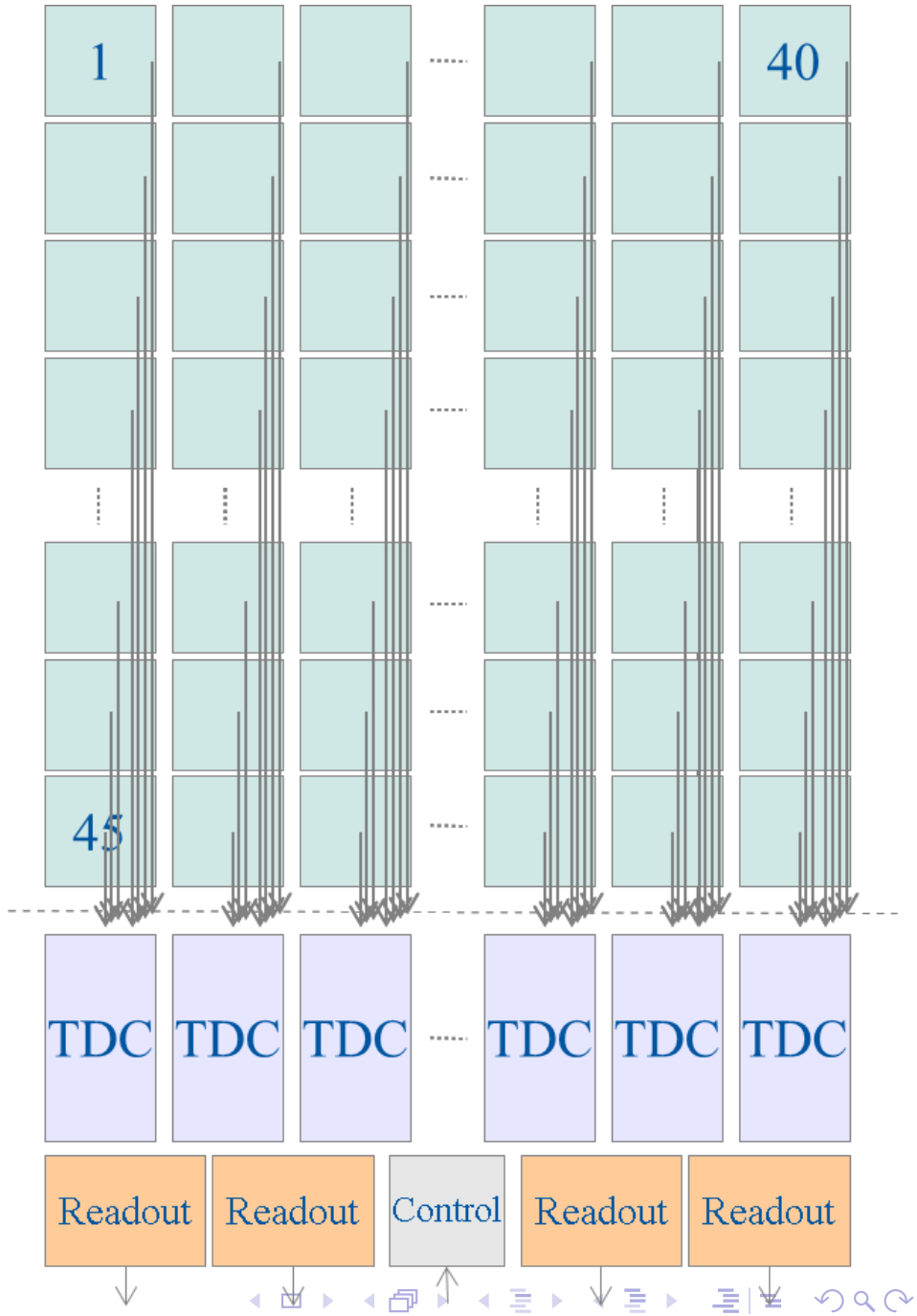
TDCPix Architectural Overview

- 40 x 45 pixels
  - 300x300 μm^2
  - asynchronous



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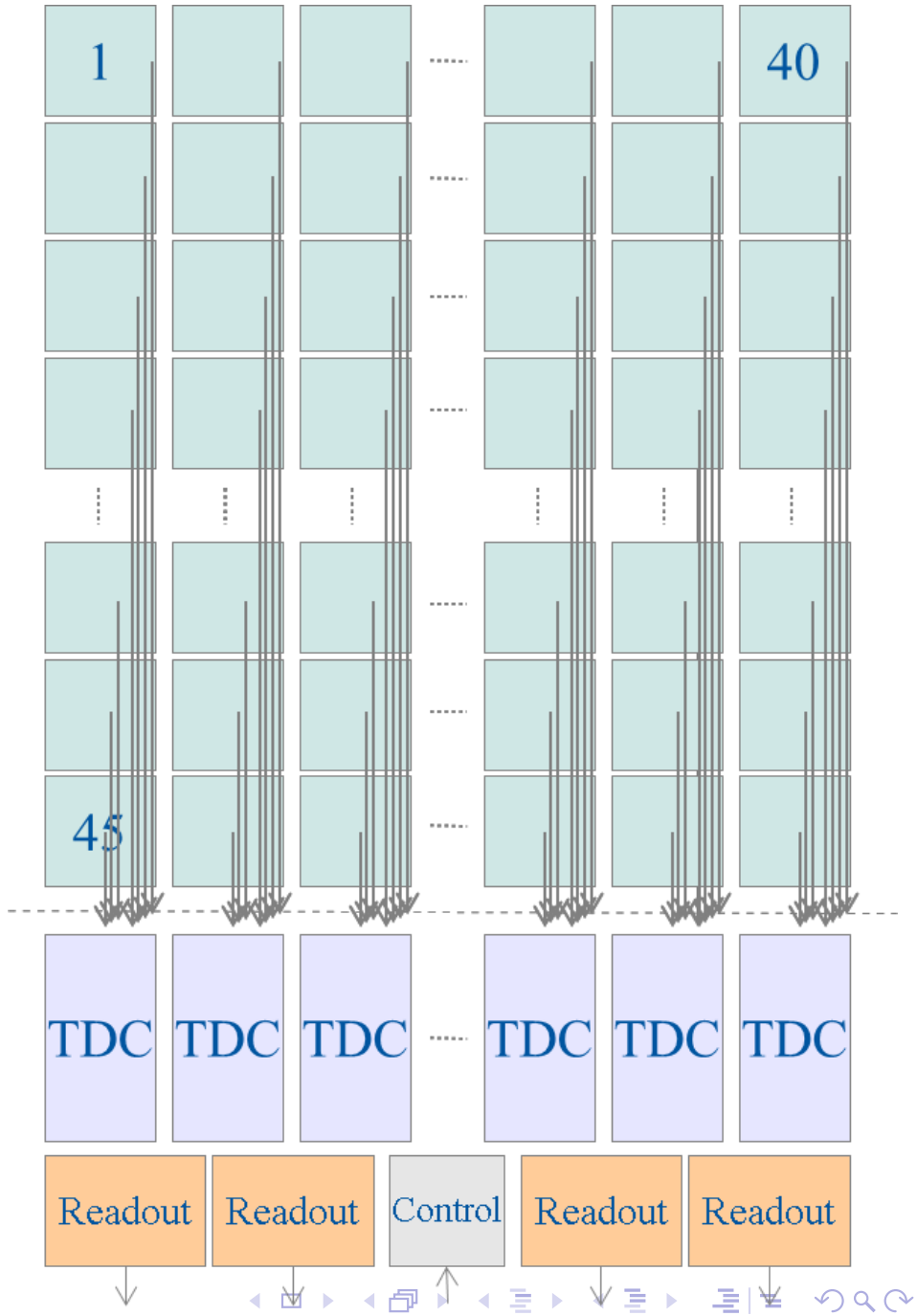
  - per-pixel hit signal to EOC



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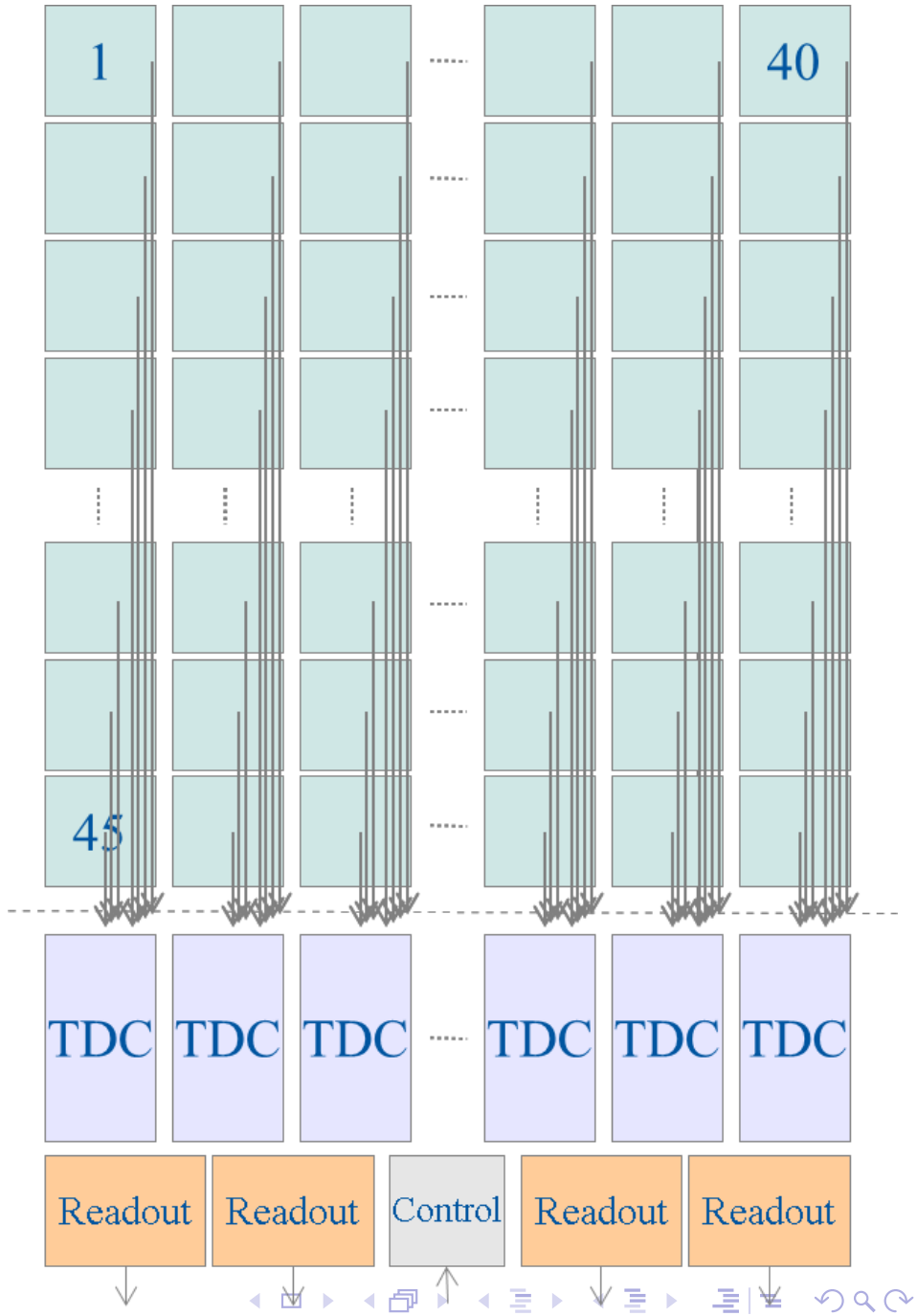
- 360 dual TDC channels
  - TDC Bin size $\sim 97\,ps$



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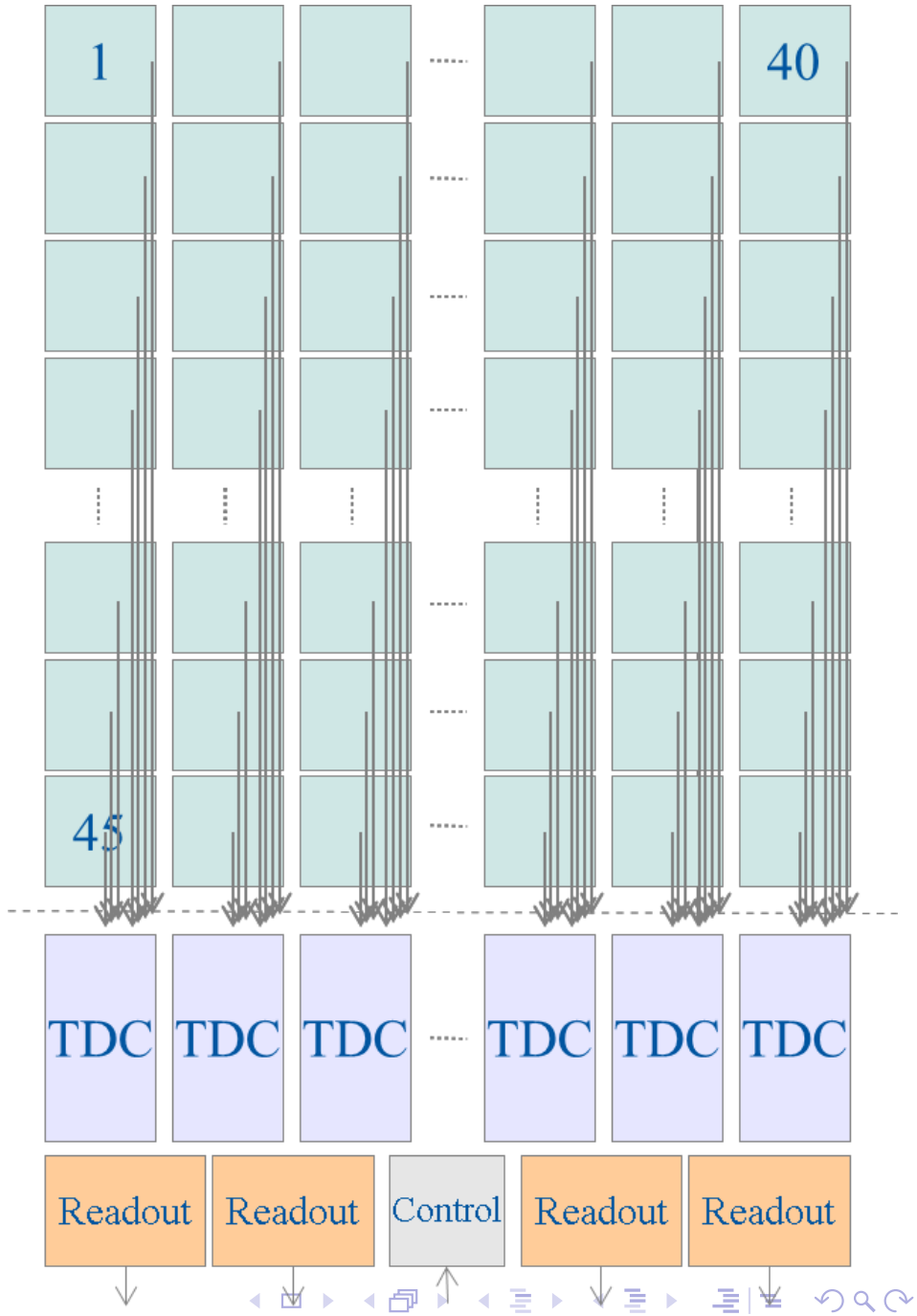
- self-triggered operation
  - Rate:210MHits/s
  - 4 x $3.2\,Gb/s$ serialisers



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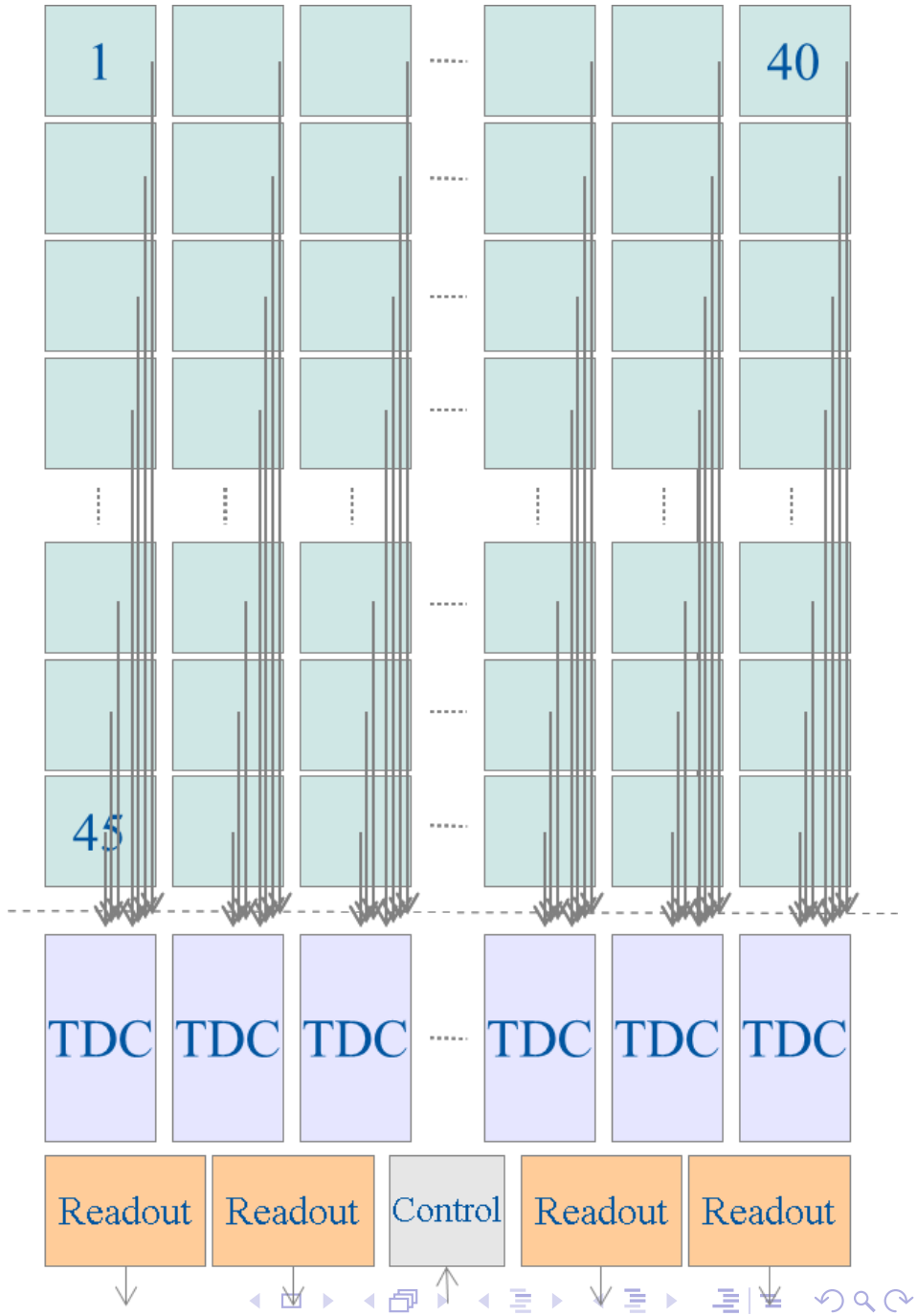
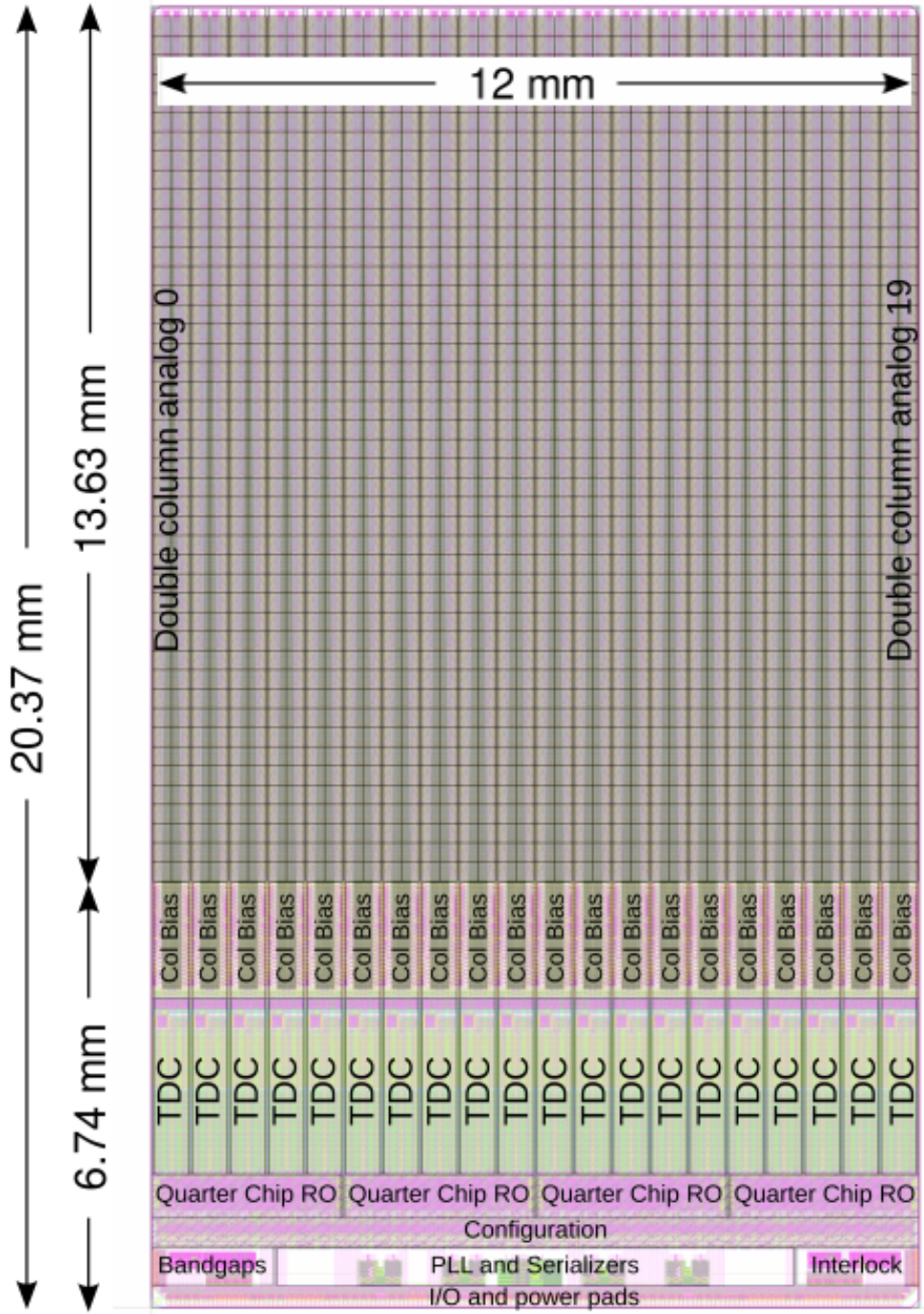
  - state/config.



TDCPix Top Level



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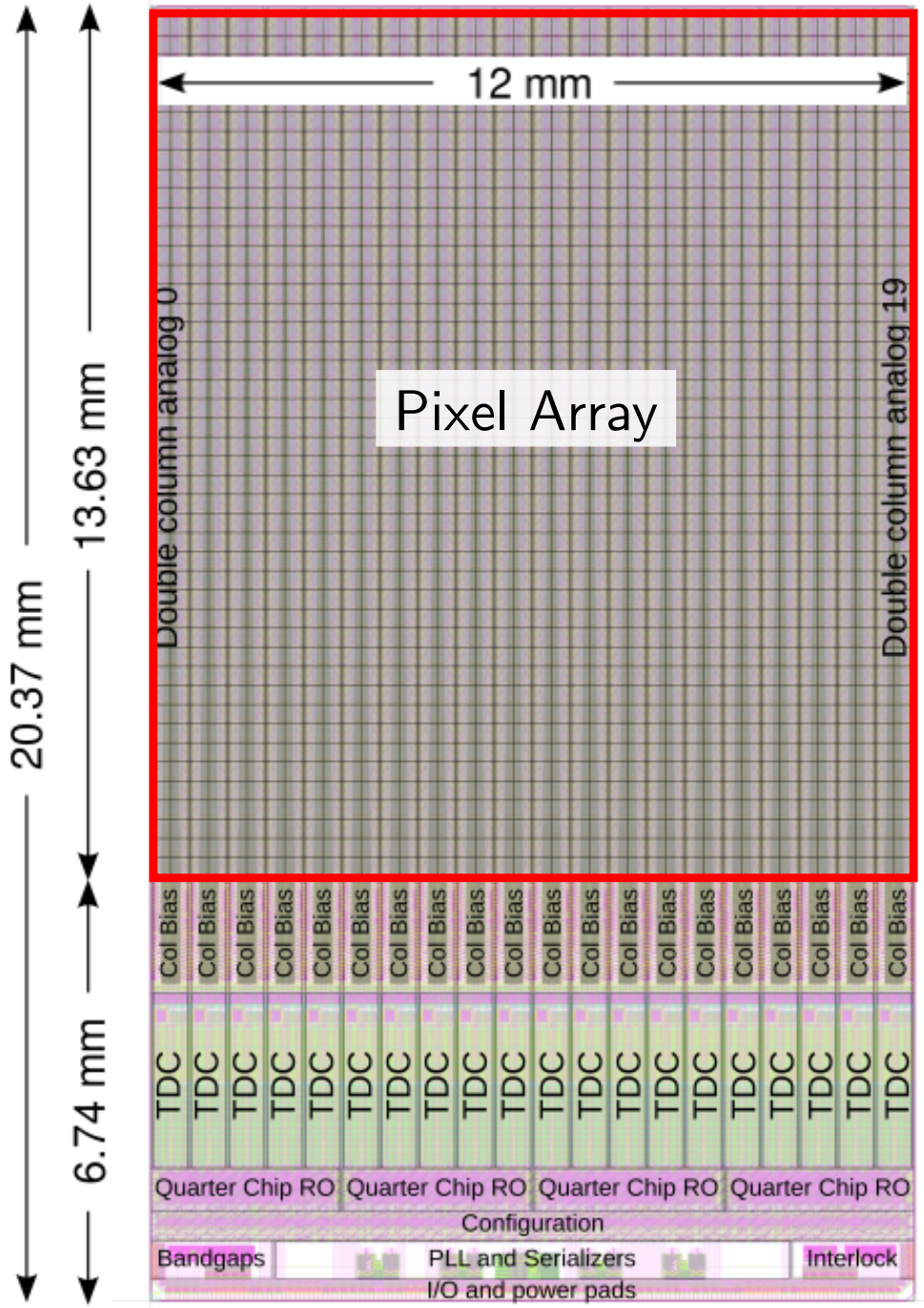

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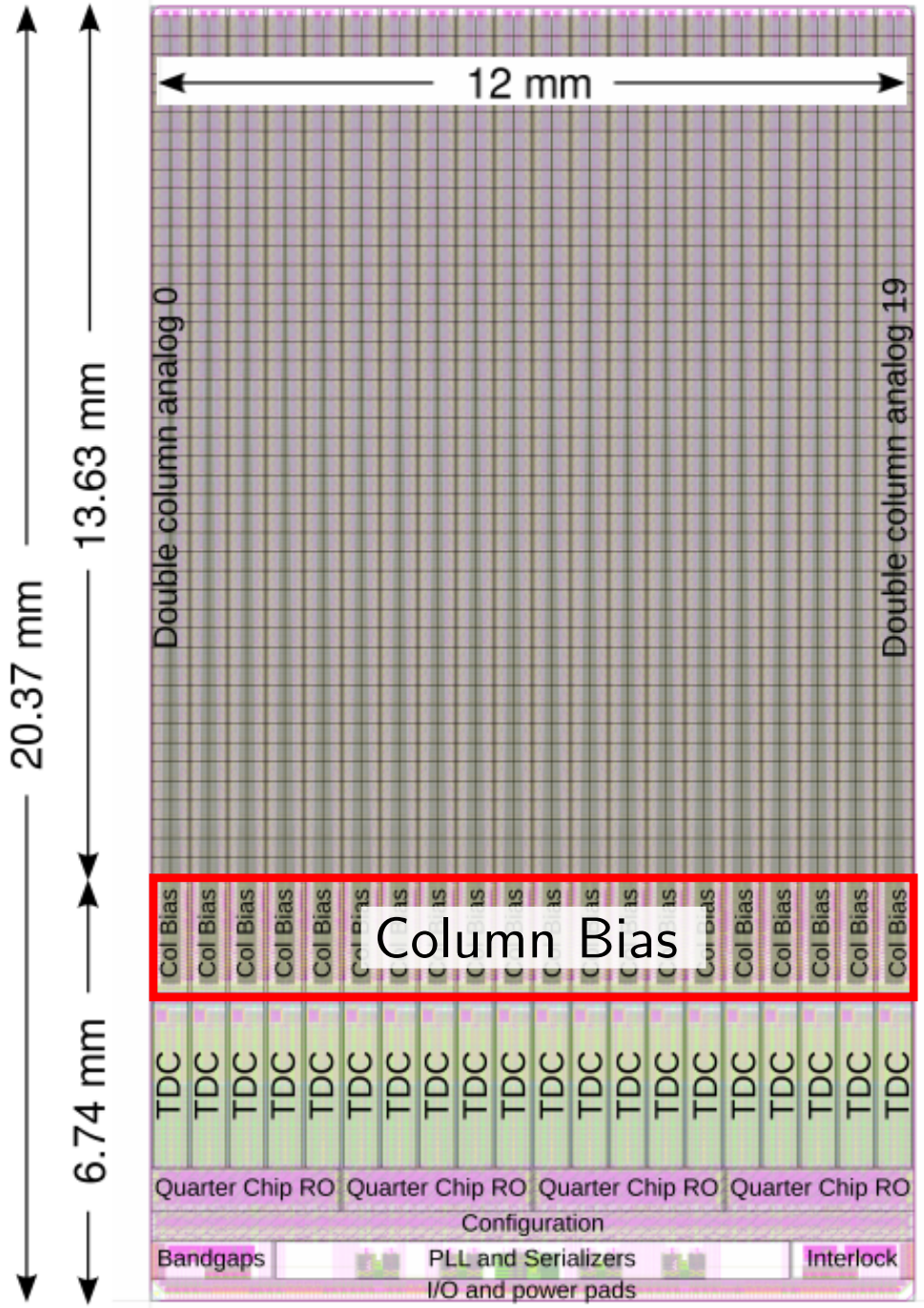

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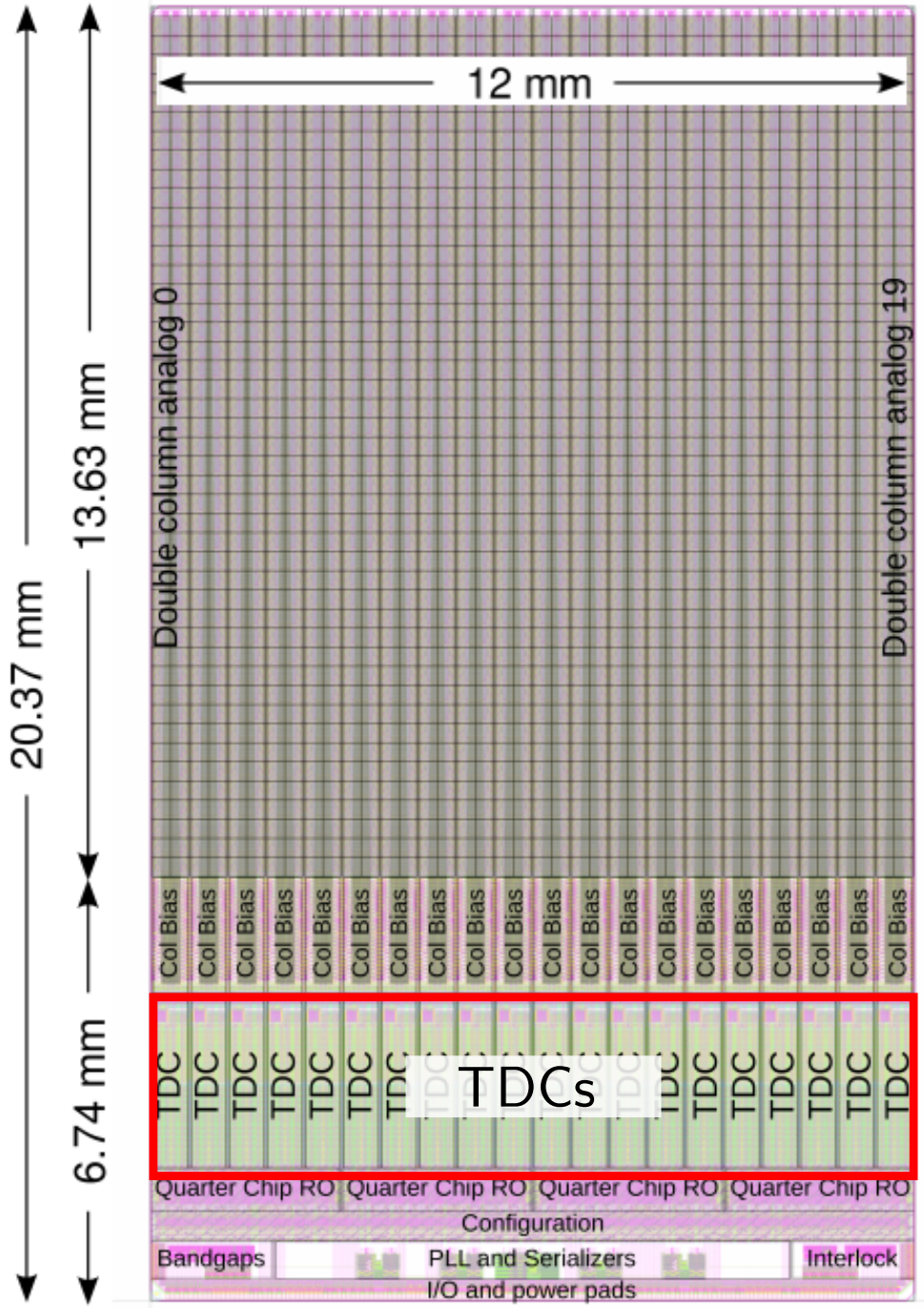

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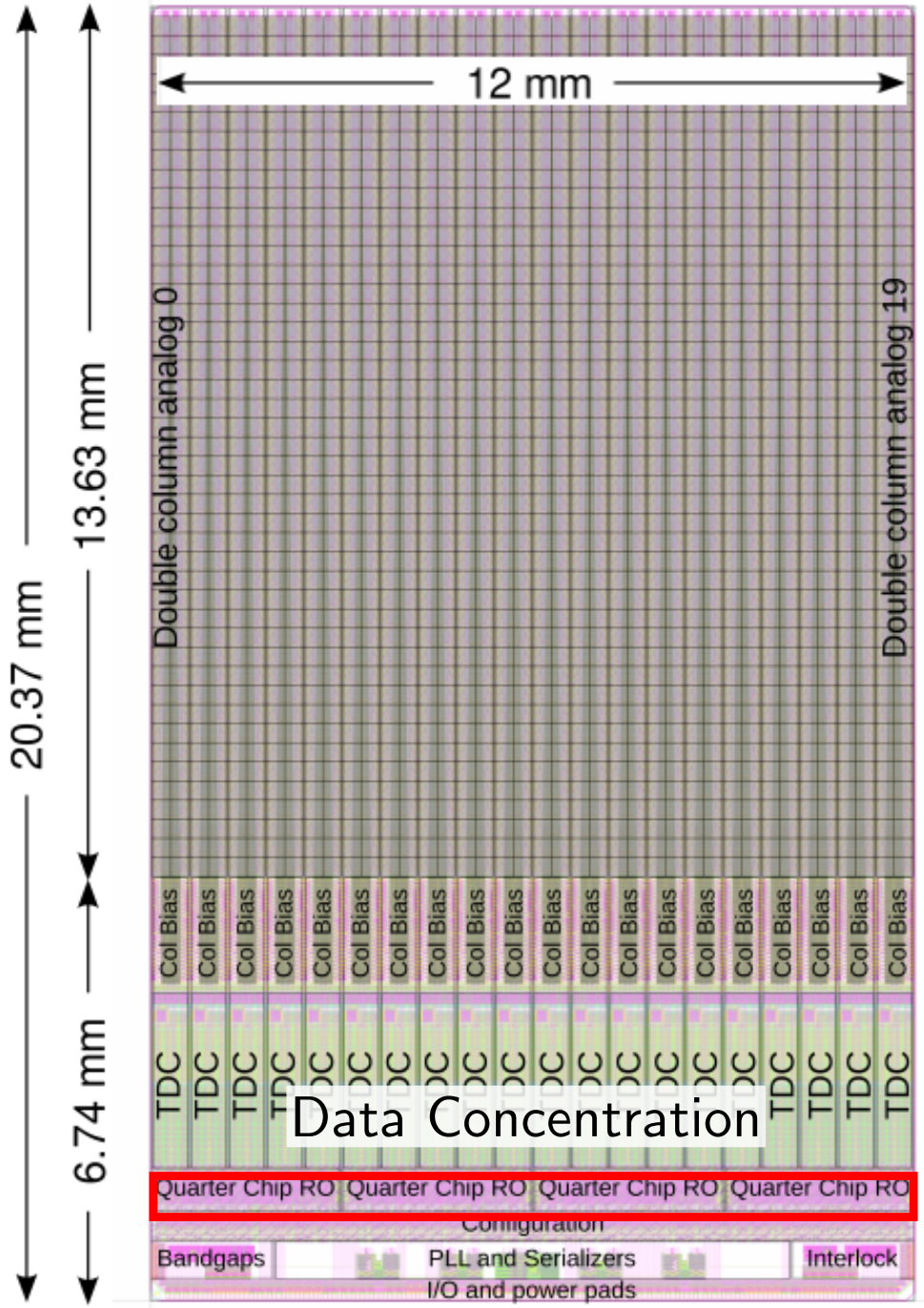

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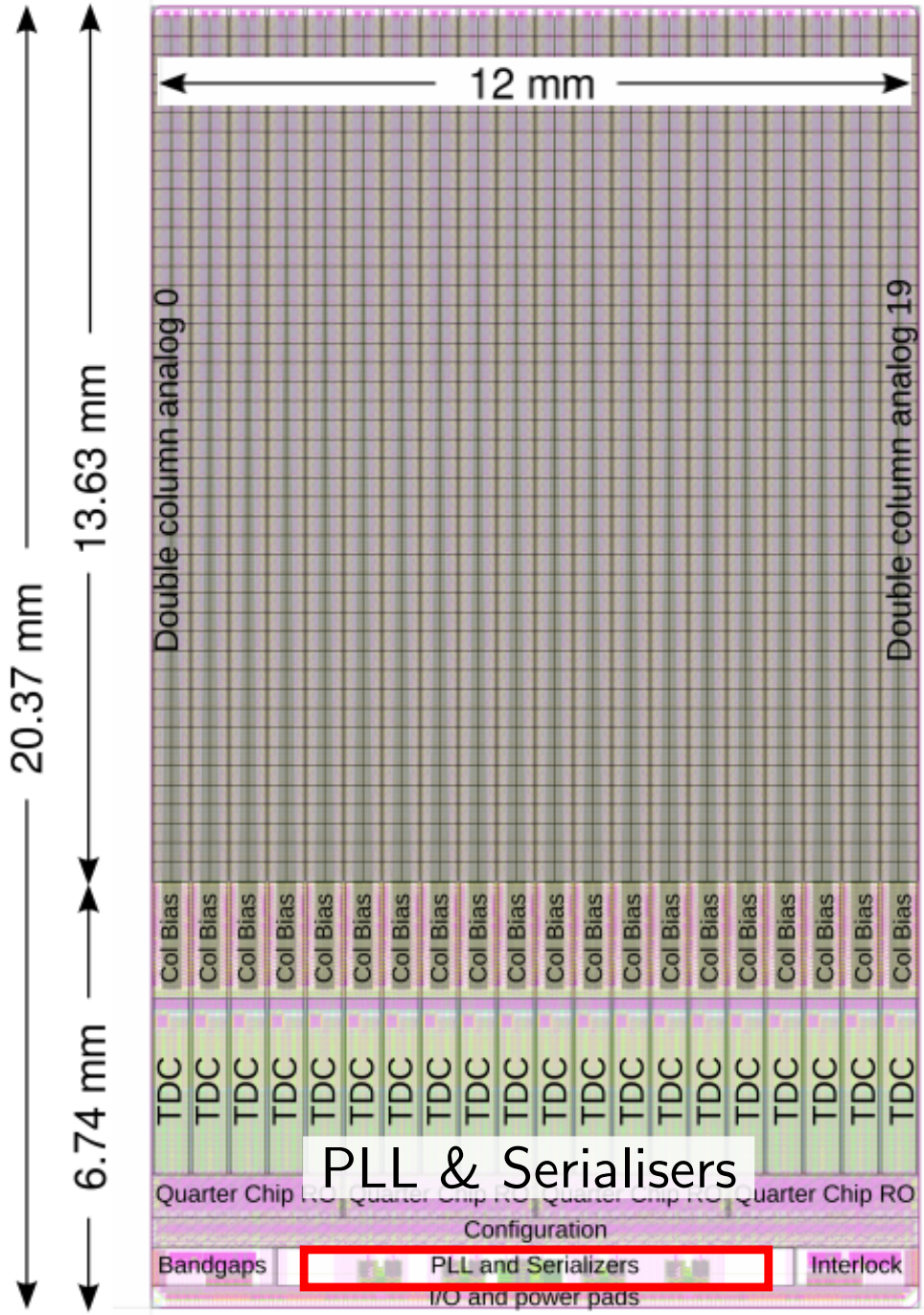

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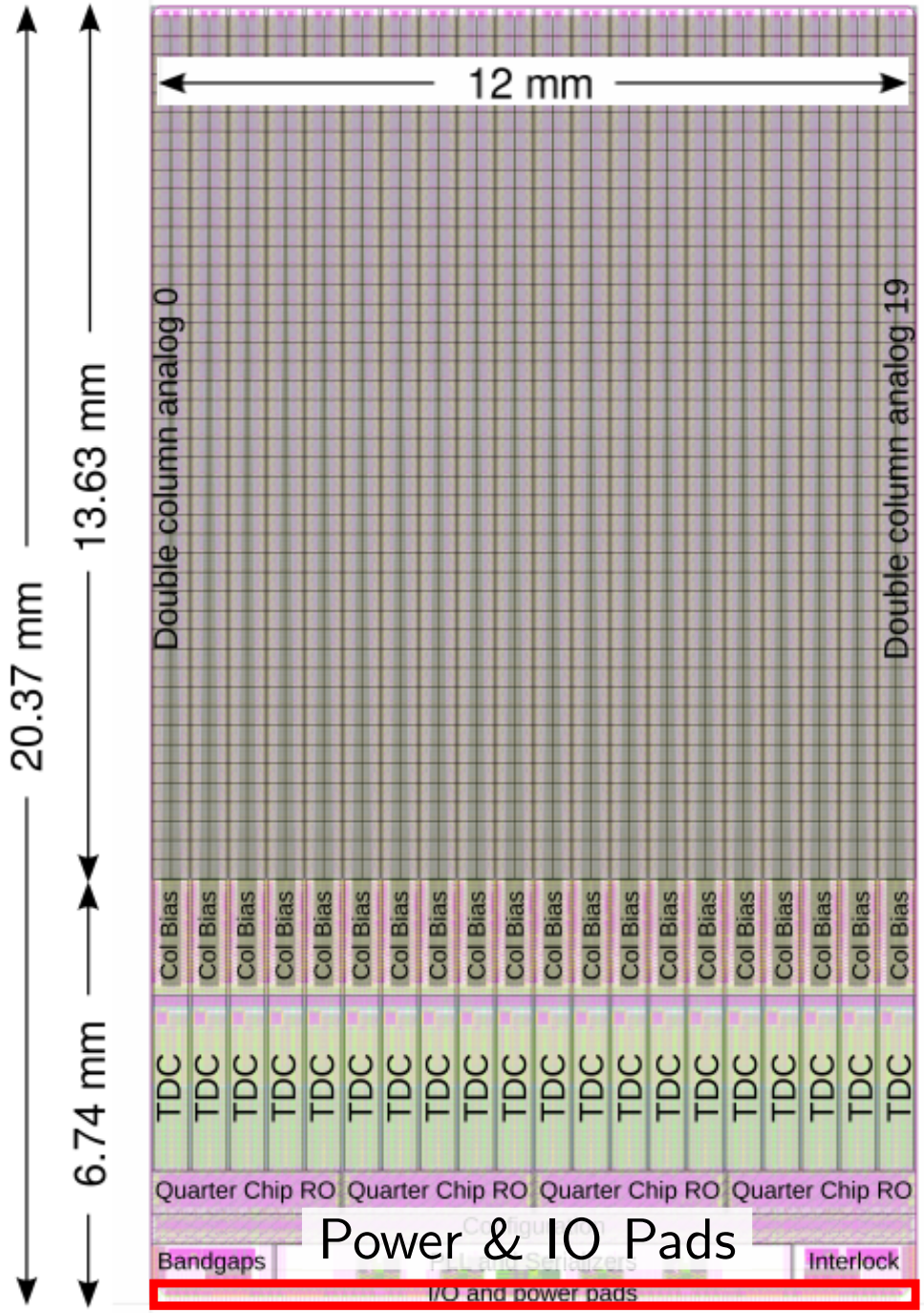
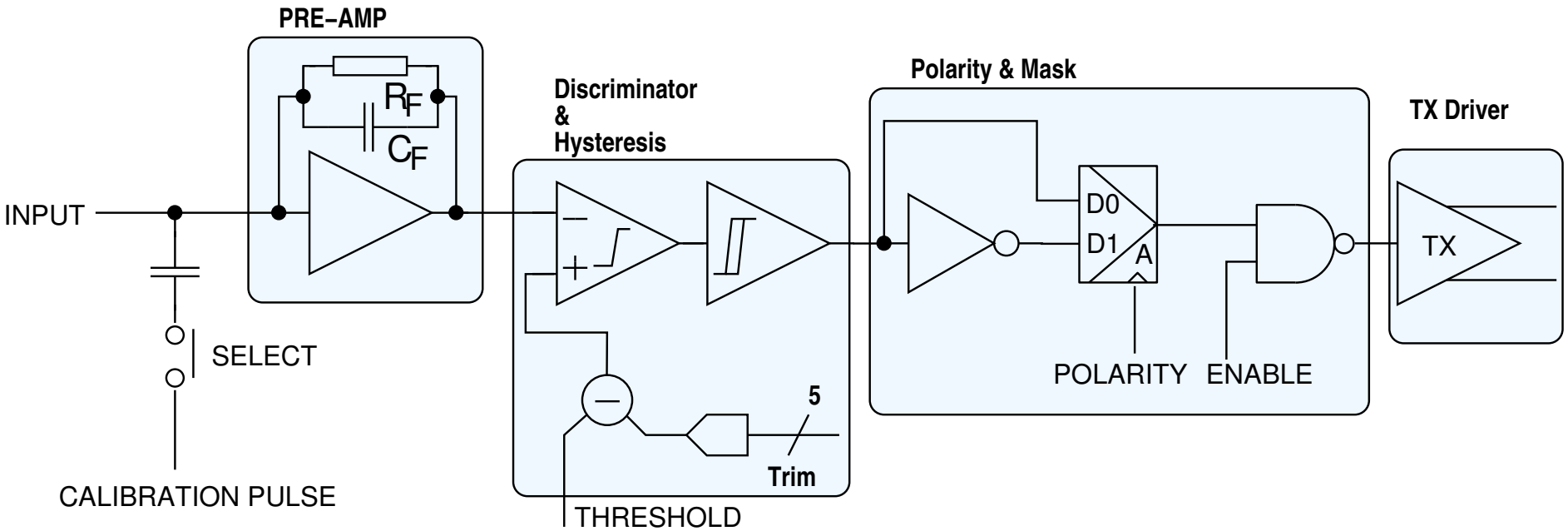
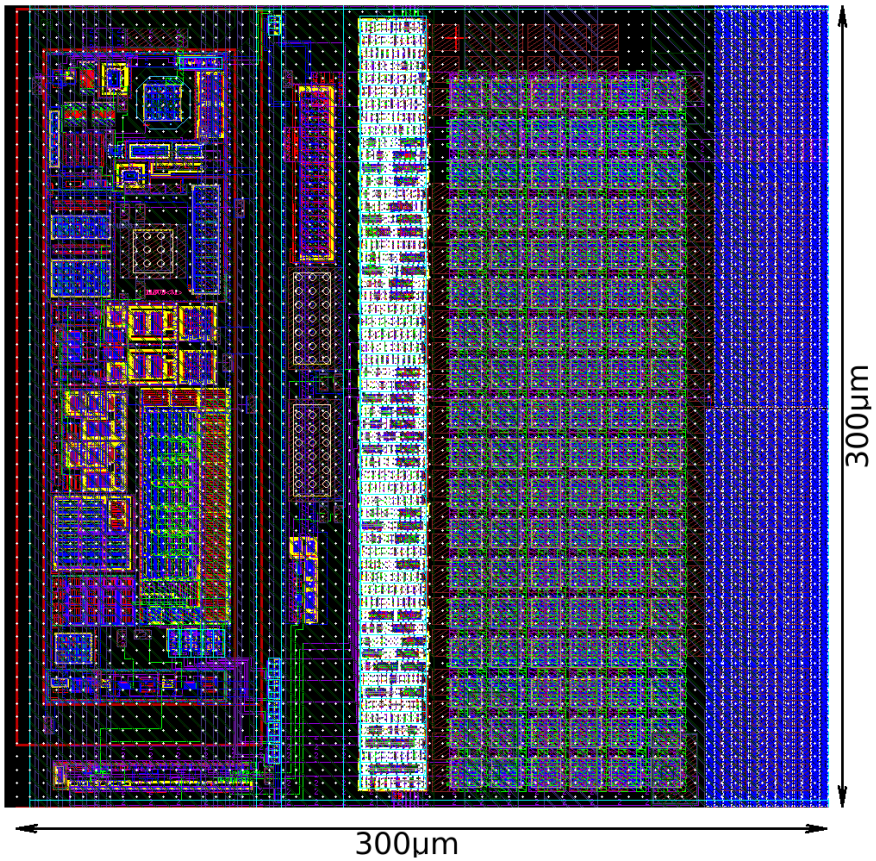


Simplified Pixel Architecture



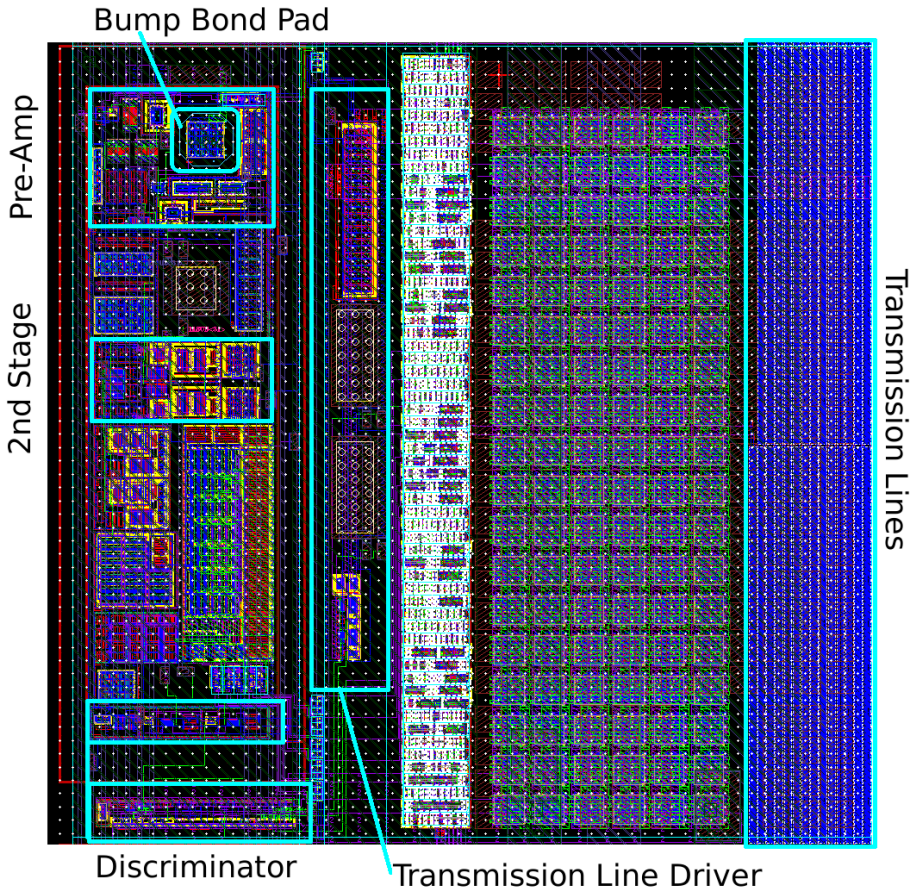
- Gain $\sim 65\,mV/fC$
- peaking time $\sim 5\,ns$
- Polarity control
- Pixel mask

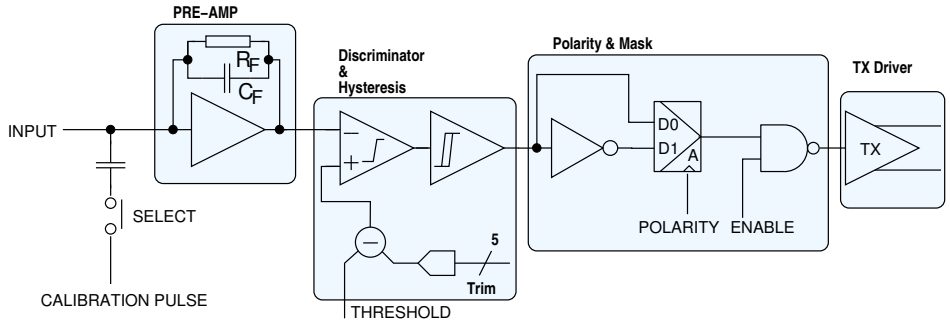
Pixel Layout:



300x300μm^2 cell

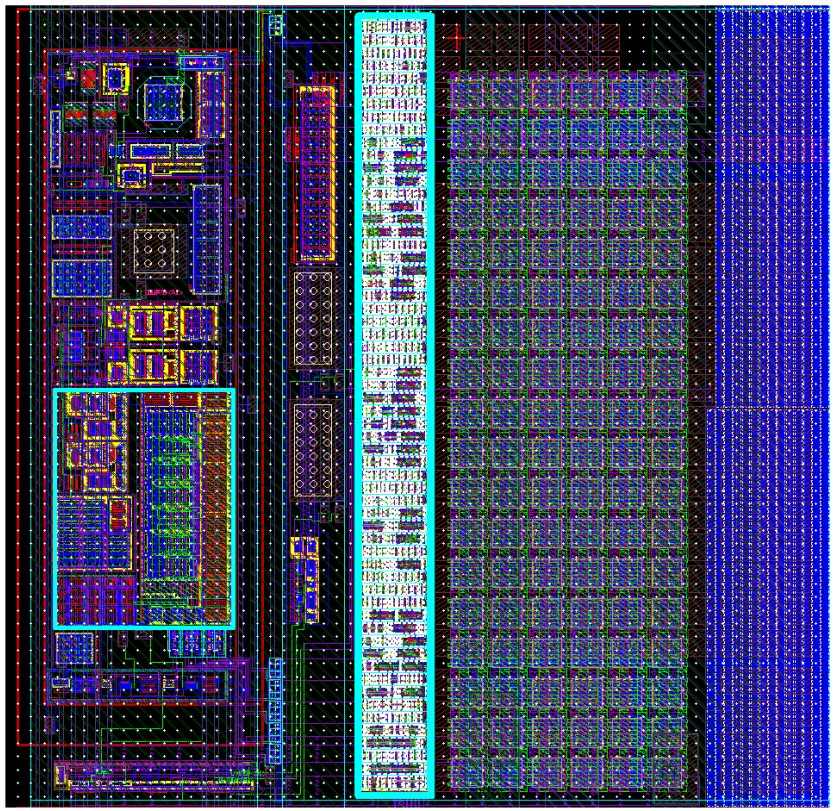
Pixel Layout: Signal Path

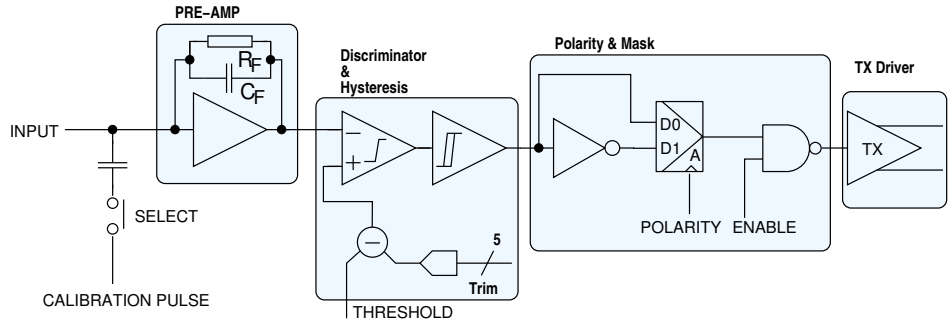




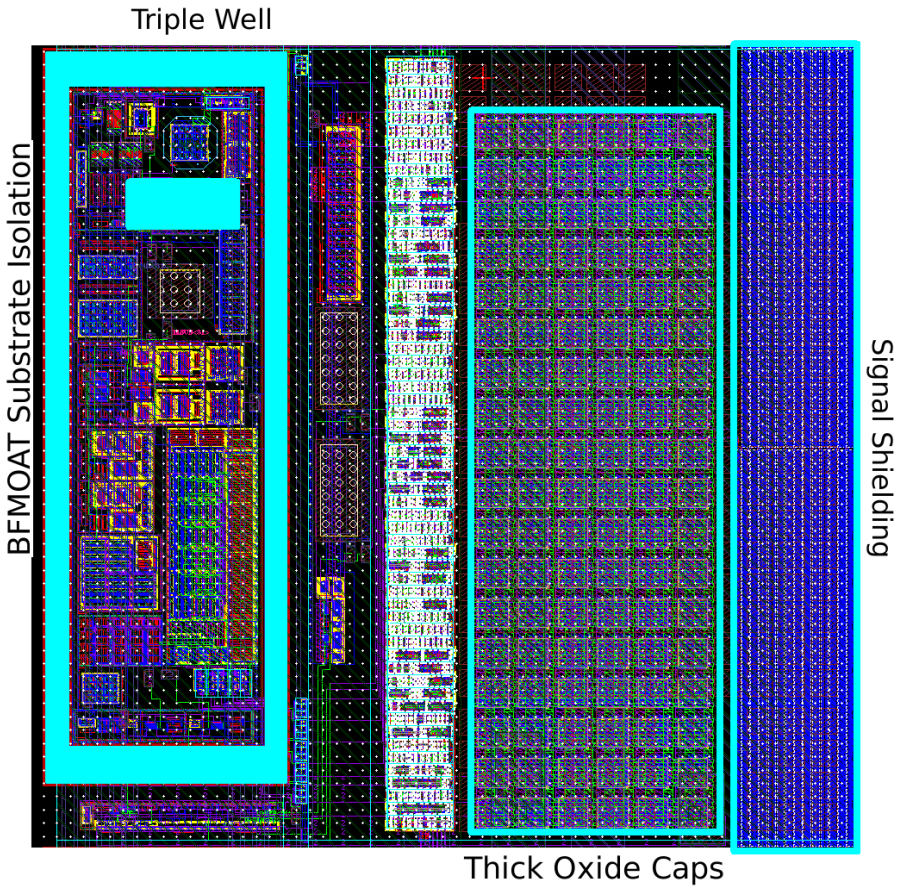
Pixel Layout: Trimming & Configuration

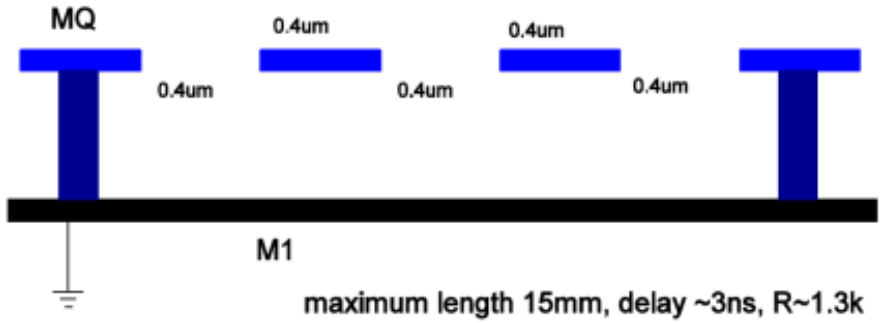
In-Pixel Configuration





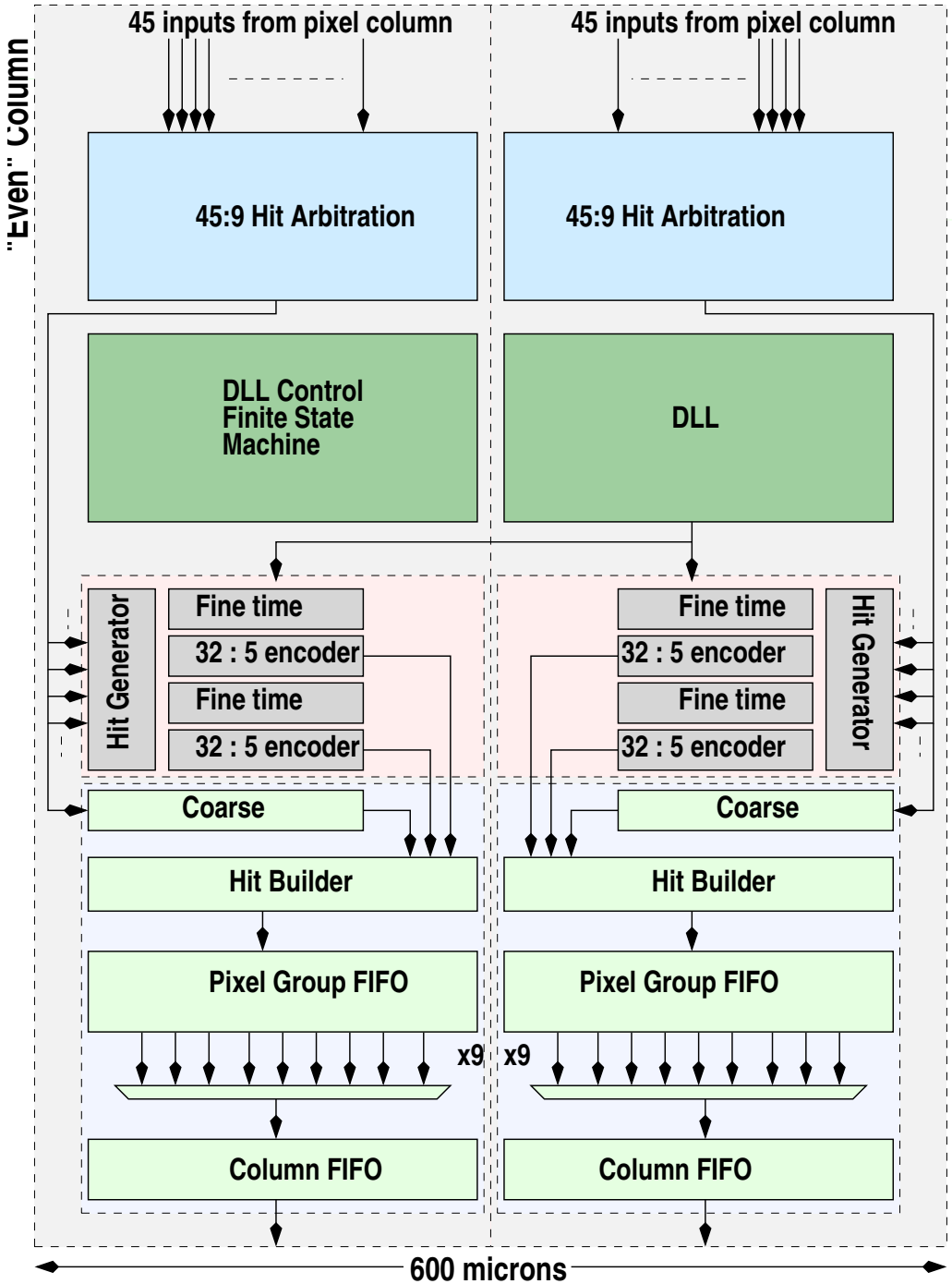
Pixel Layout: Noise Mitigation

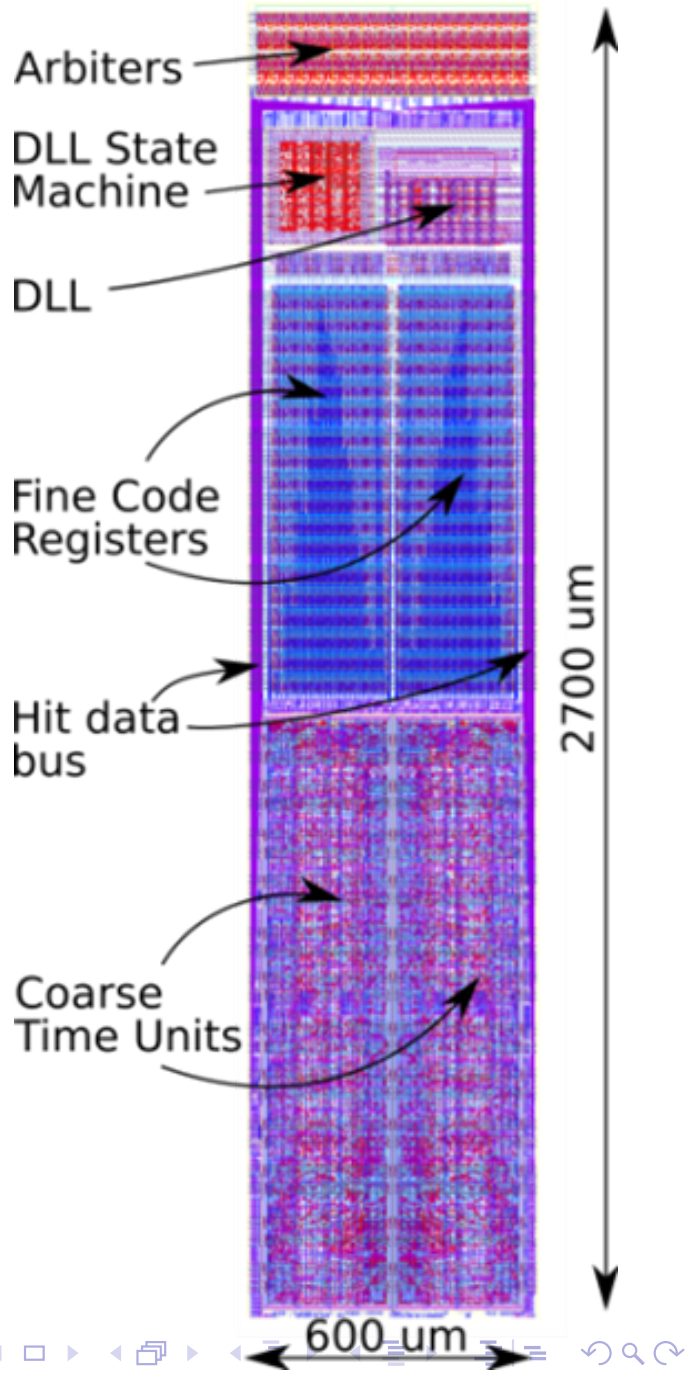




- Triple well (input transistor)
- BFMOAT substrate isolation
- signal shielding
- Power supply decoupling

TDC: Schematic and Layout





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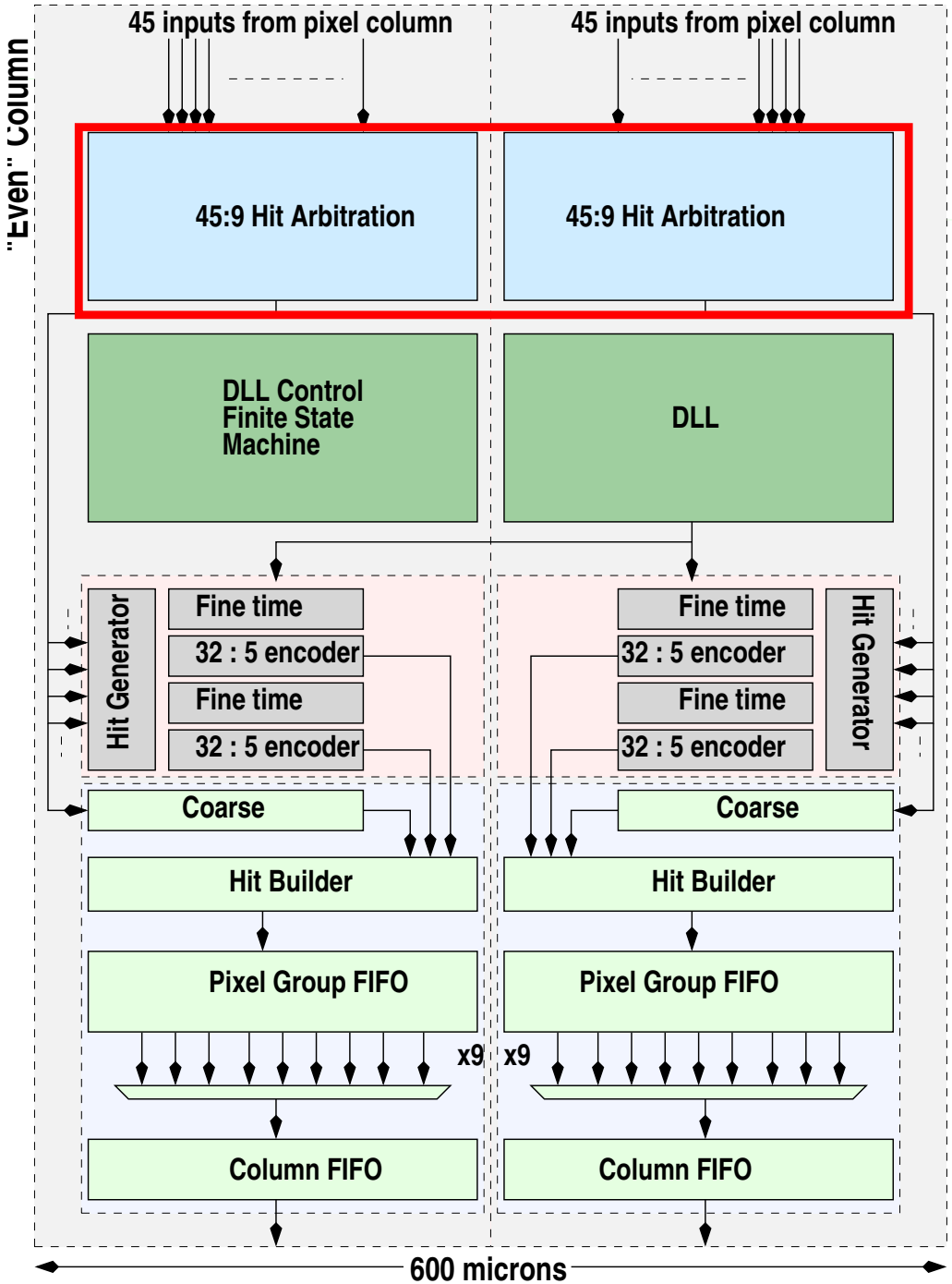

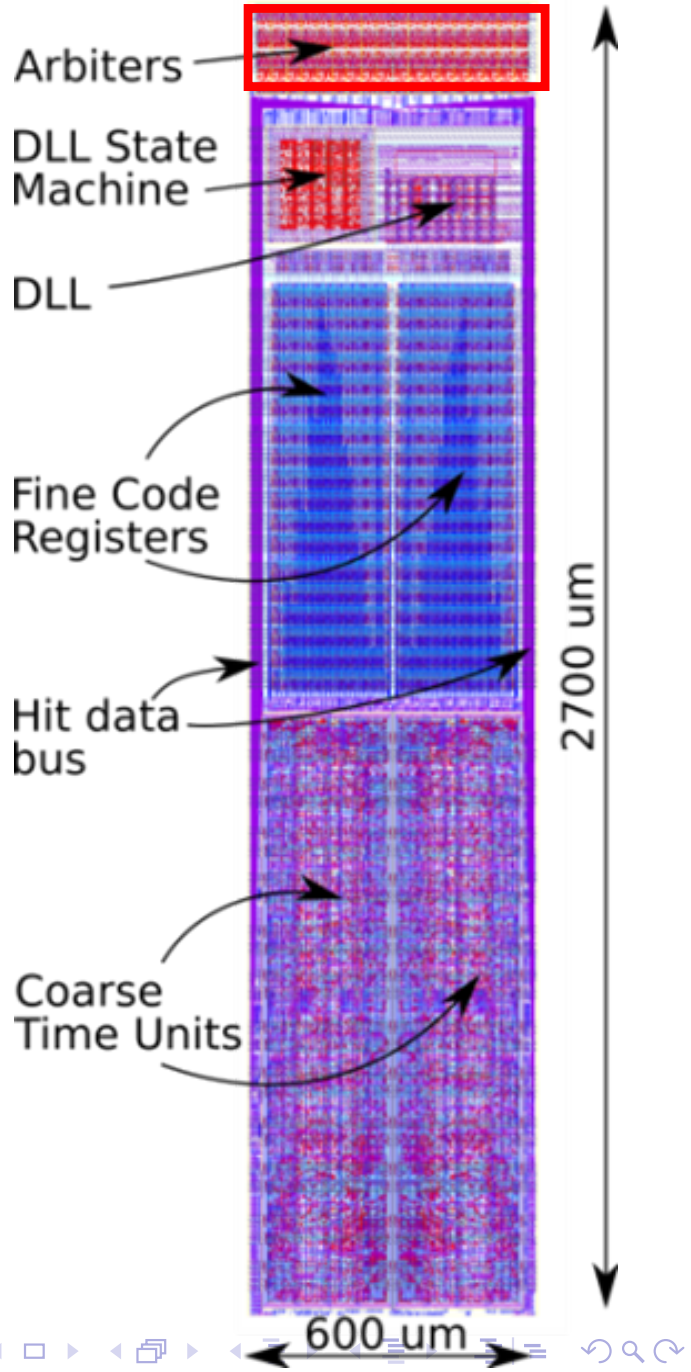

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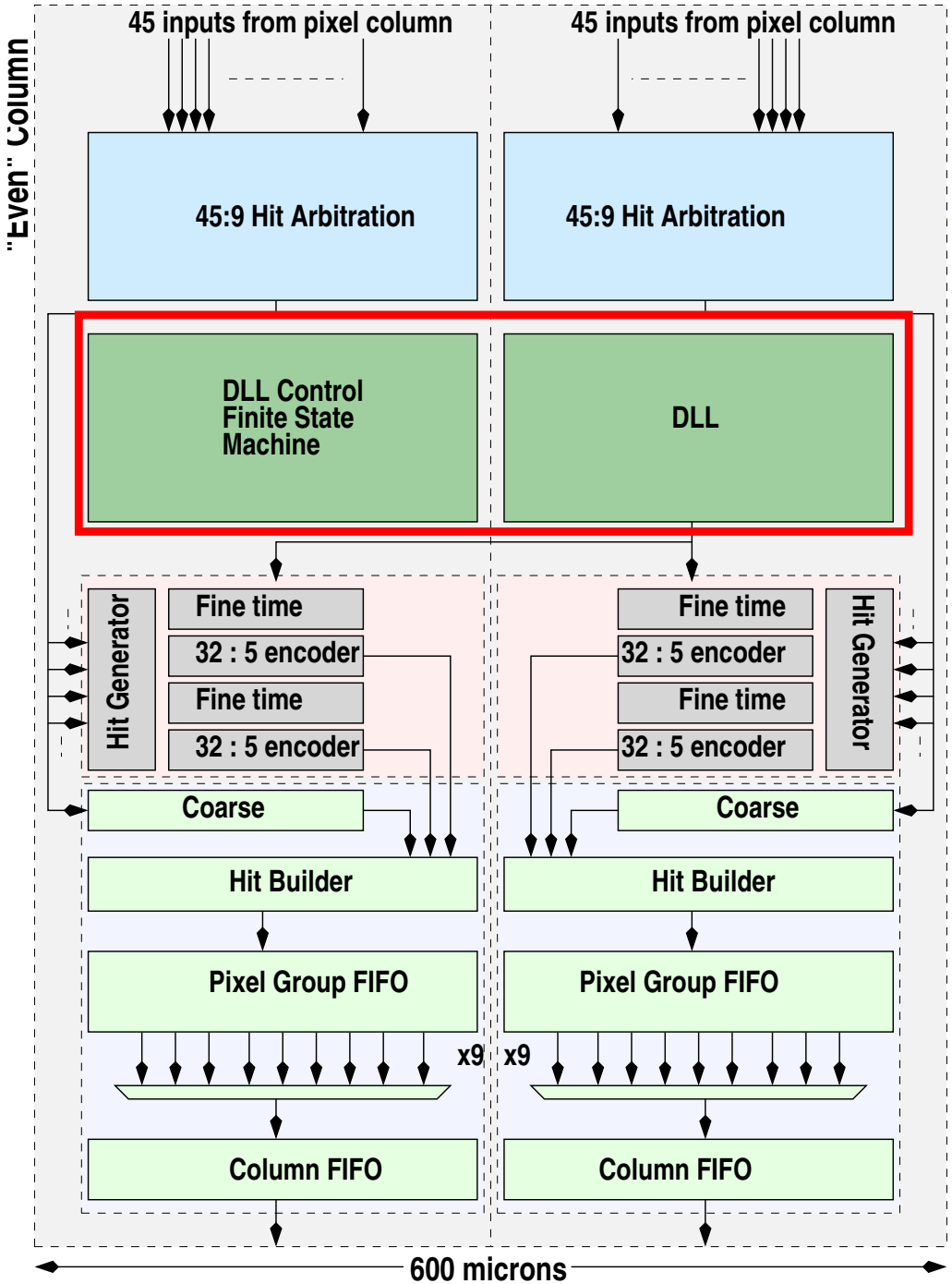

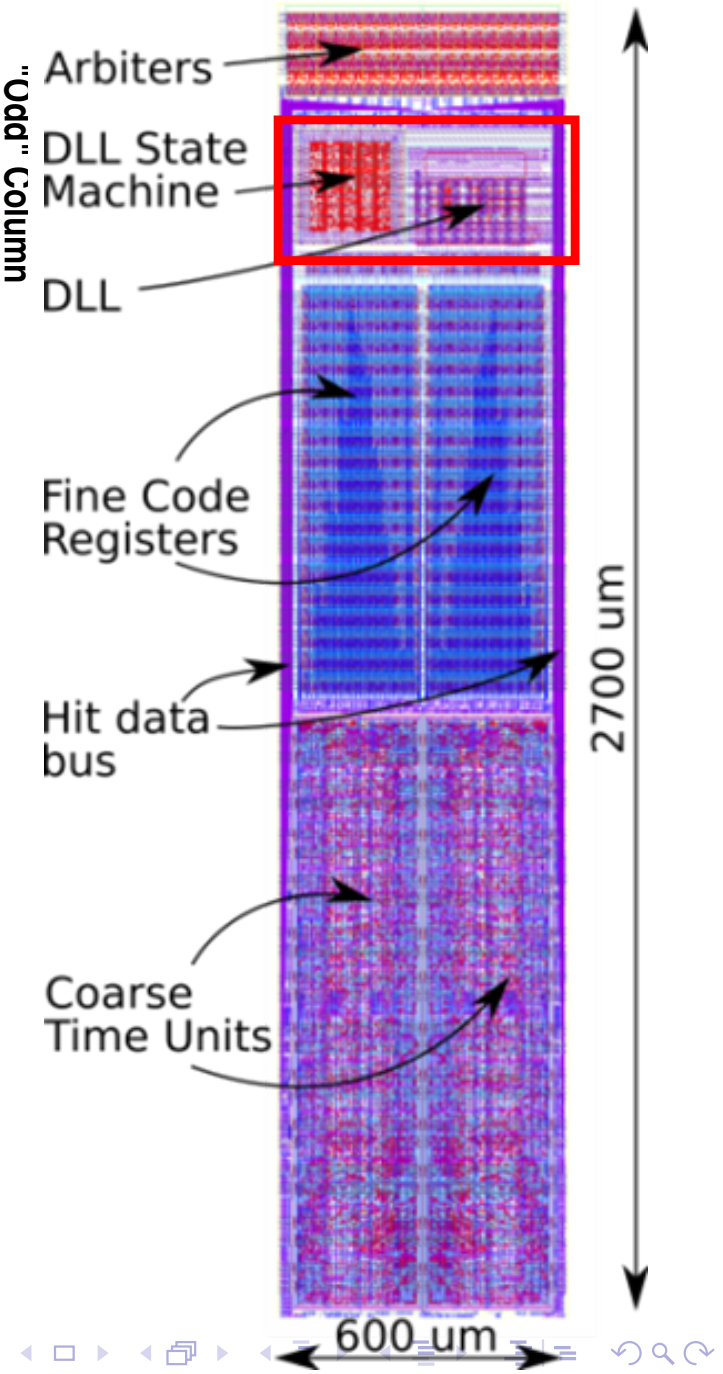

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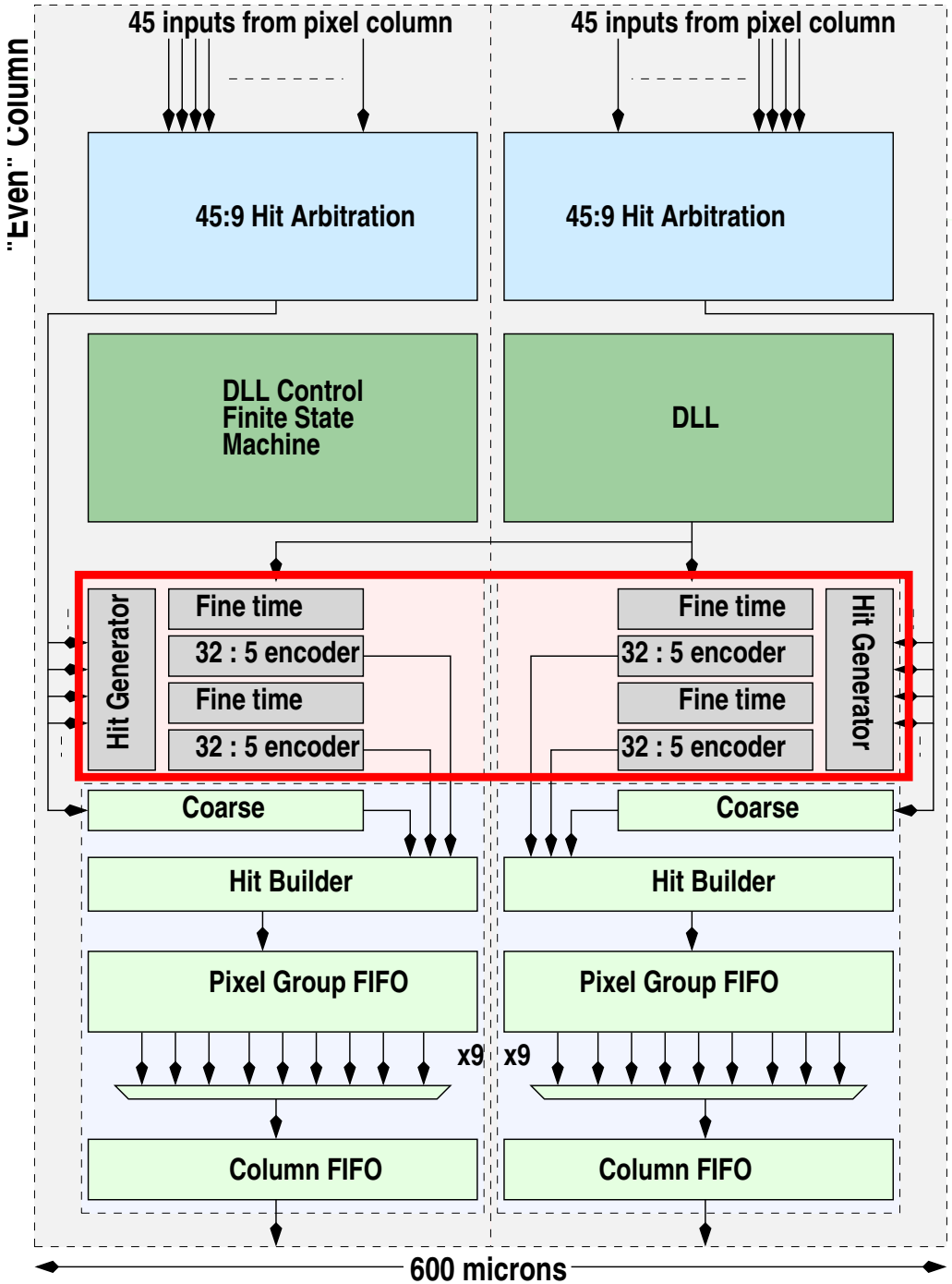

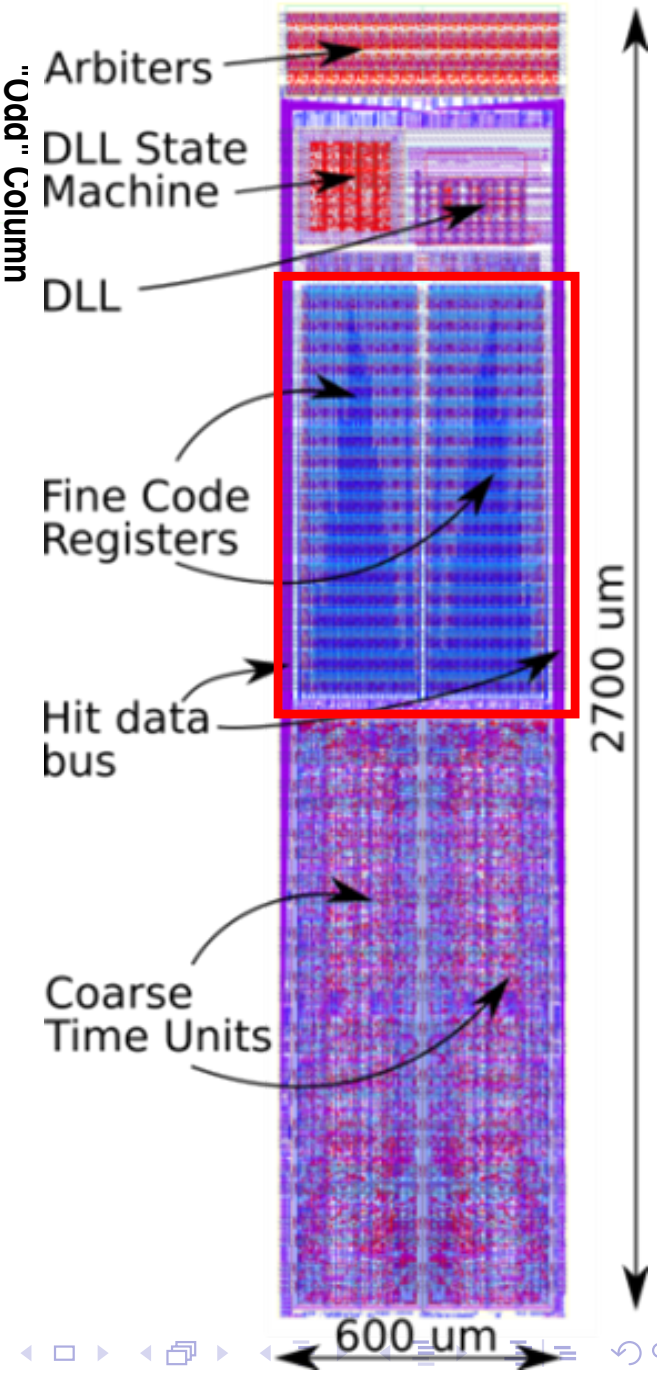

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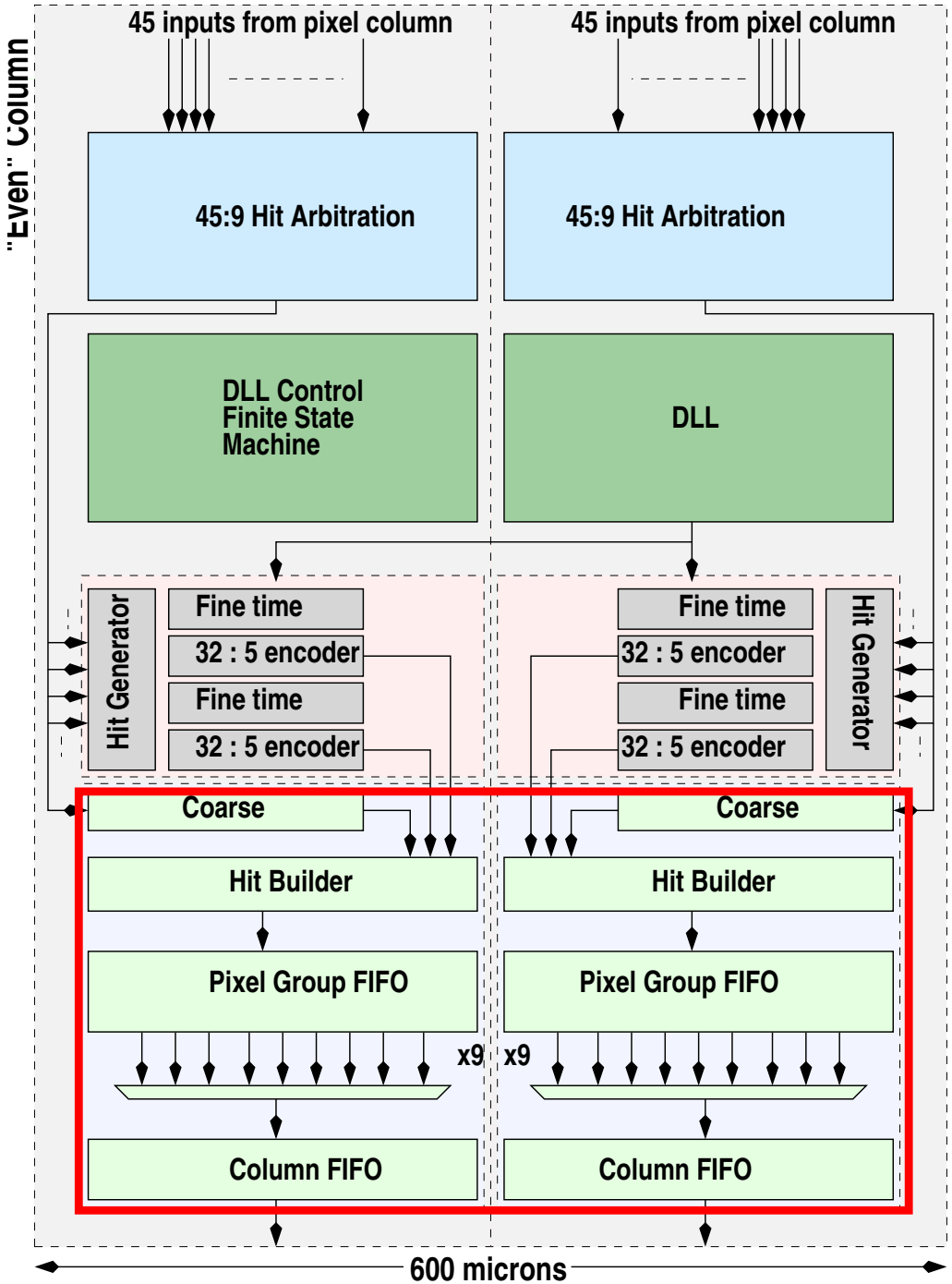
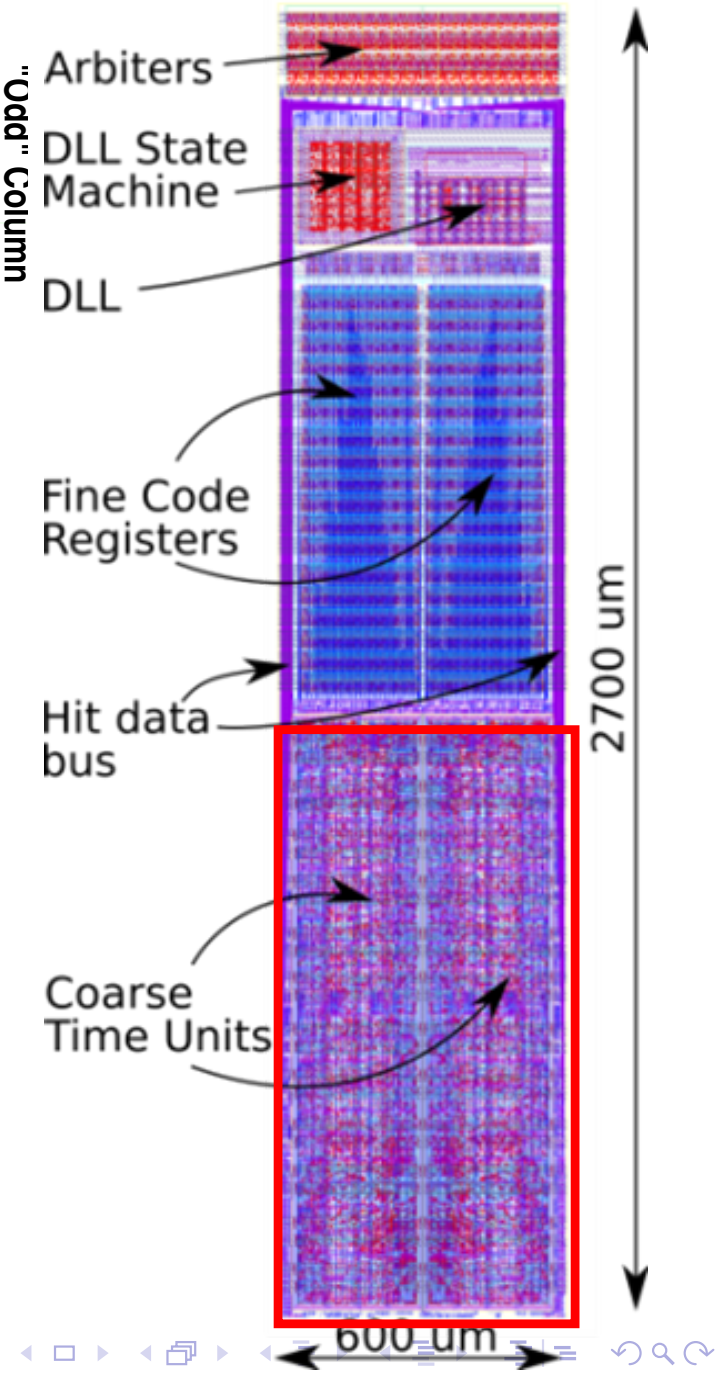
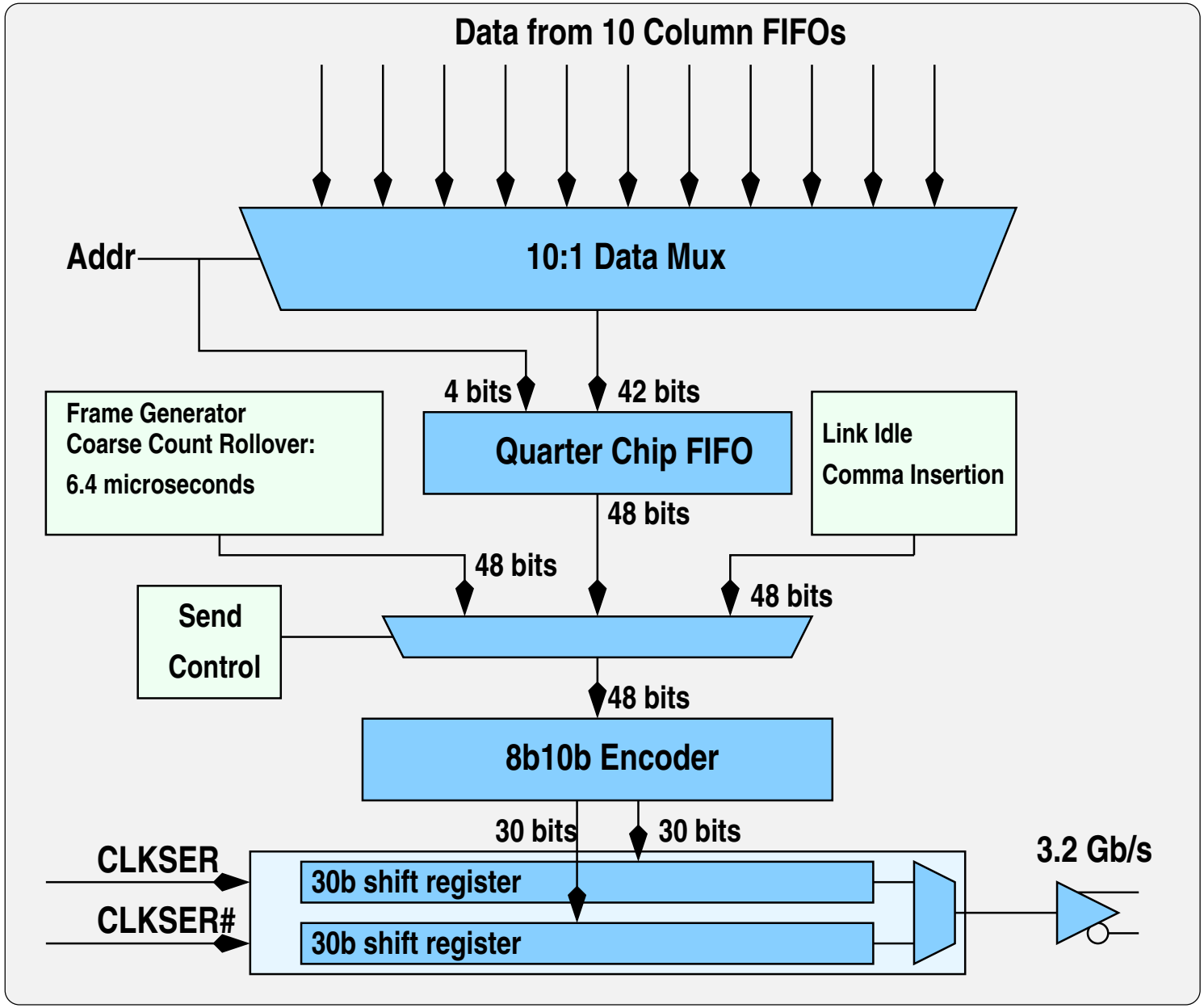
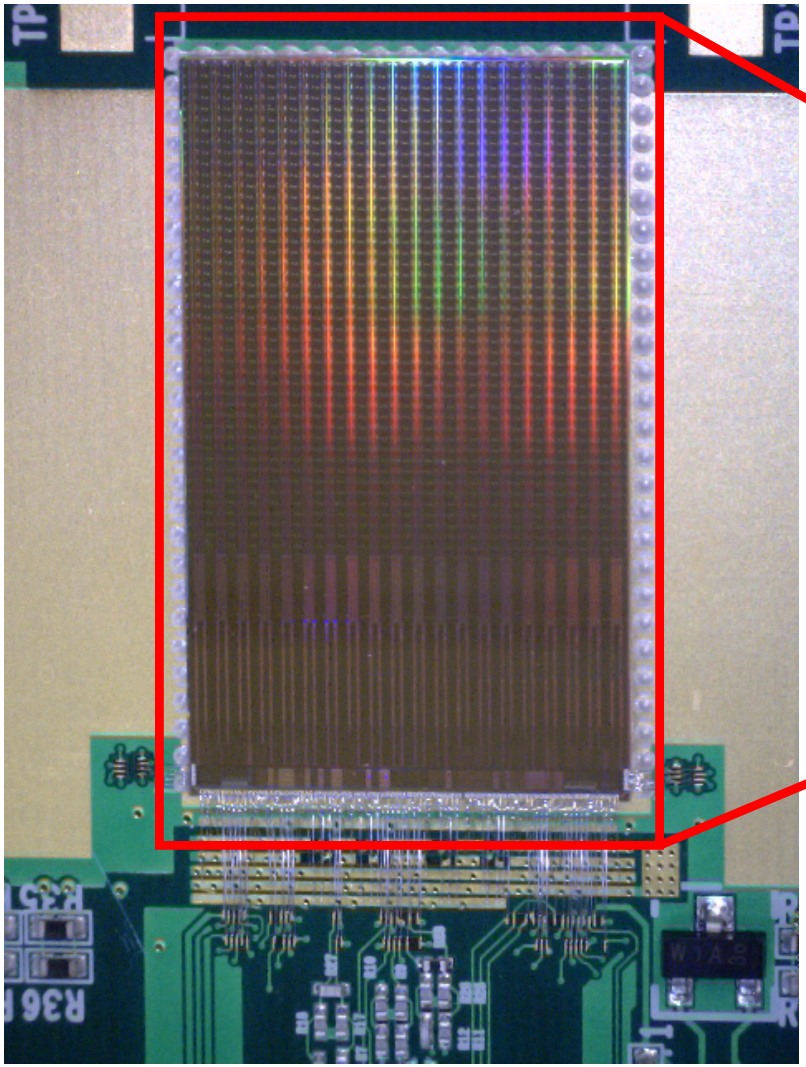


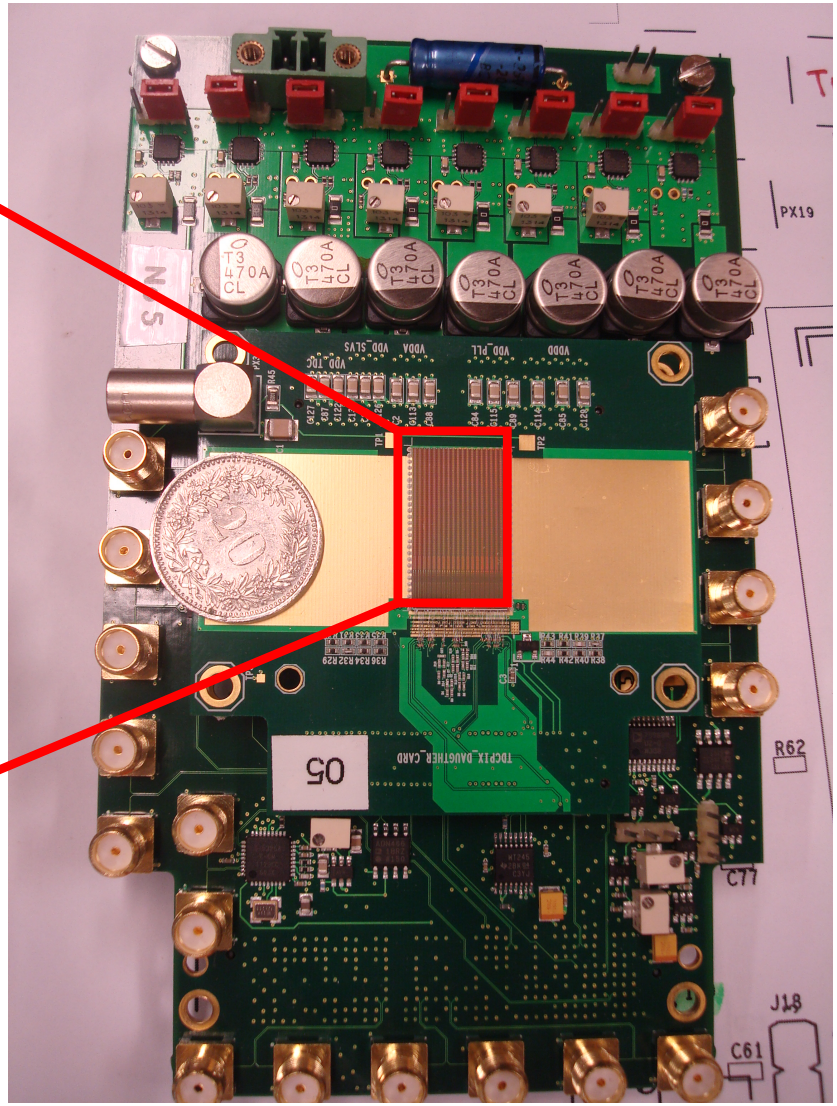


The Quarter Chip & Serialiser



TDCPix Wire Bonded to the Test Card





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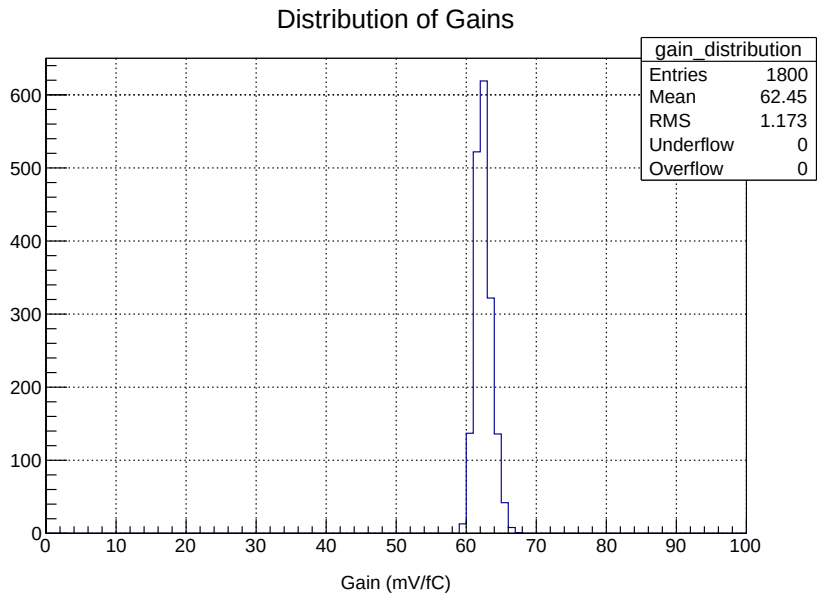
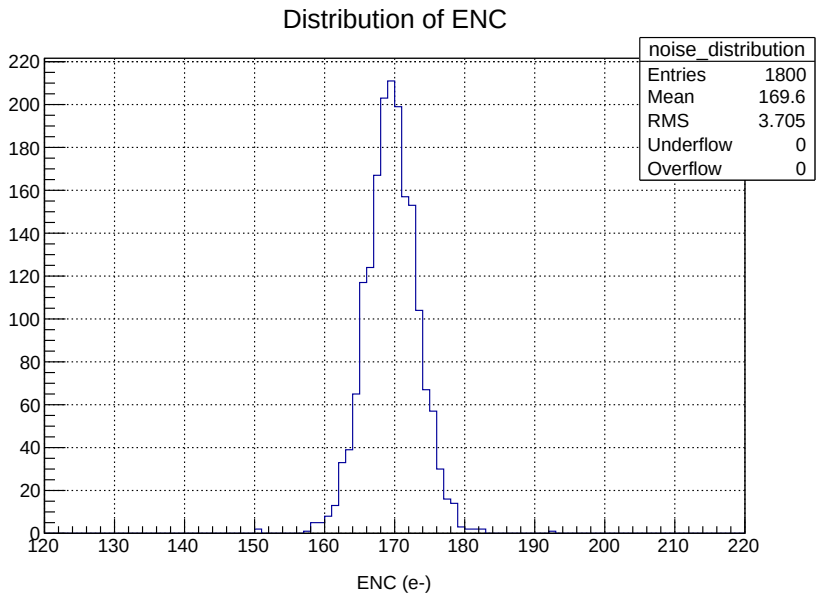
Functionality Tested

Block	Status	Remarks
Configuration	Working	5 chips tested
PLL	Working	3.2 GHz
Serialisers	Working	3.2 Gb/s
Bandgaps	Working	
Temperature Interlock	Working	
Column Biasing	Working	200 DACs
In-Pixel Threshold Trimming	Working	1800 DACs
# of bugs detected	0	

First Working Silicon

Full Pixel Array Gain & ENC Distributions



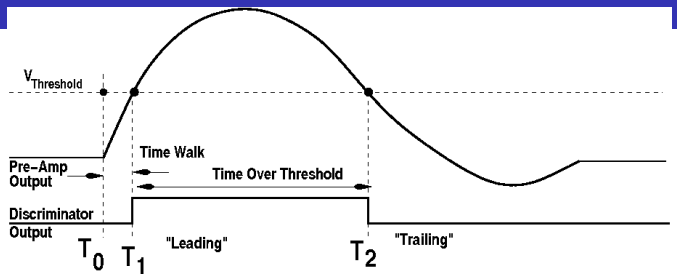


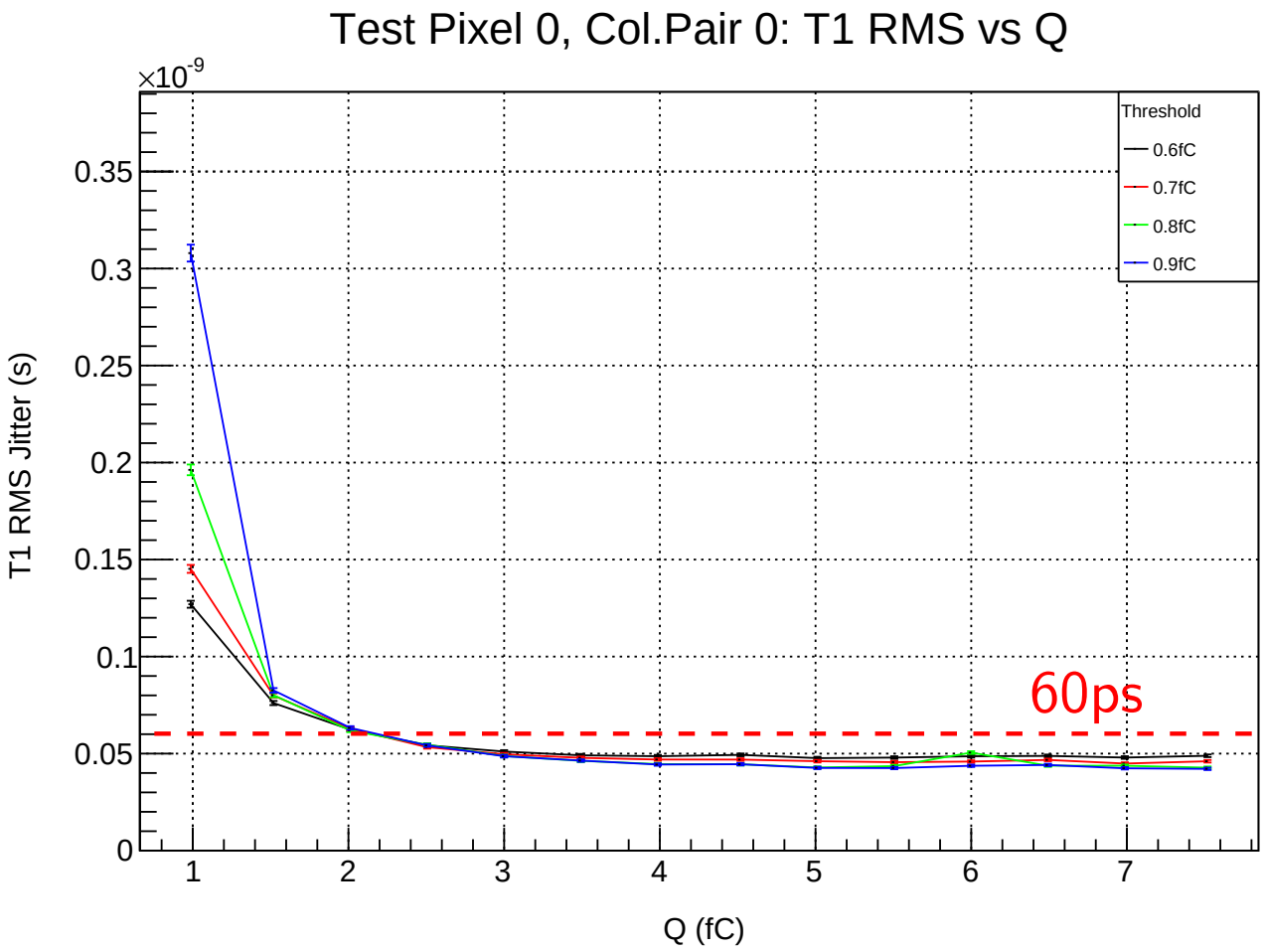
<Gain> $= 62\,\mathrm{mV/fC}$
Spread $= 1.1\,\mathrm{mV/fC}$

<ENC> $= 170e^{-}$
No sensor

Pixel Jitter

Test Pixel Jitter





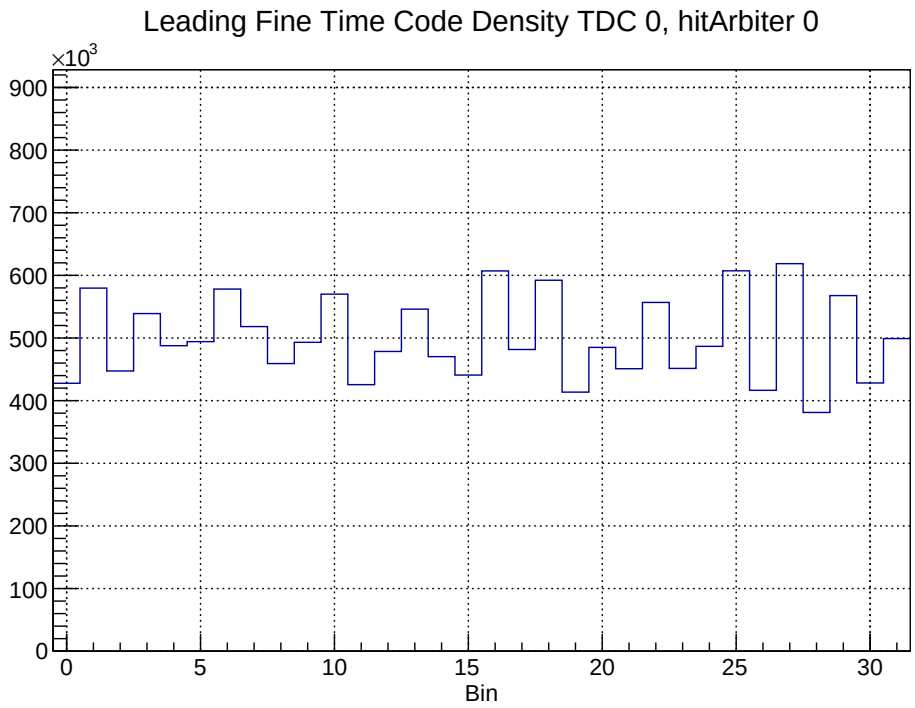
T1 RMS $<$ 60 ps at 2.5 fC

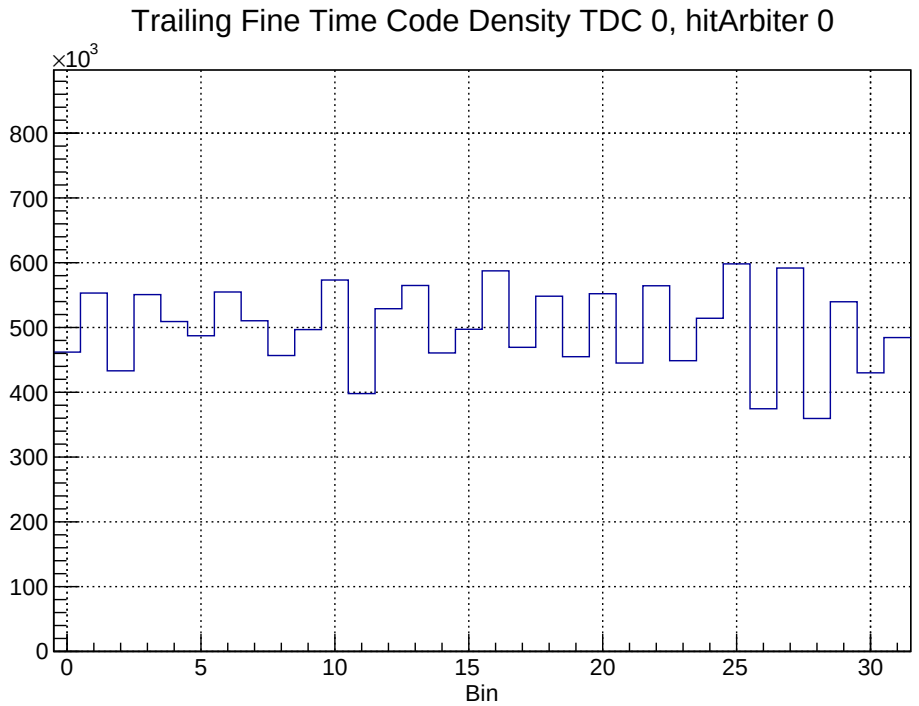
includes:

- Test pulse generation
- Test pulse distribution
- TX
- transmission line
- RX
- HitArbiter
- EoC Buffering

TDC Performance

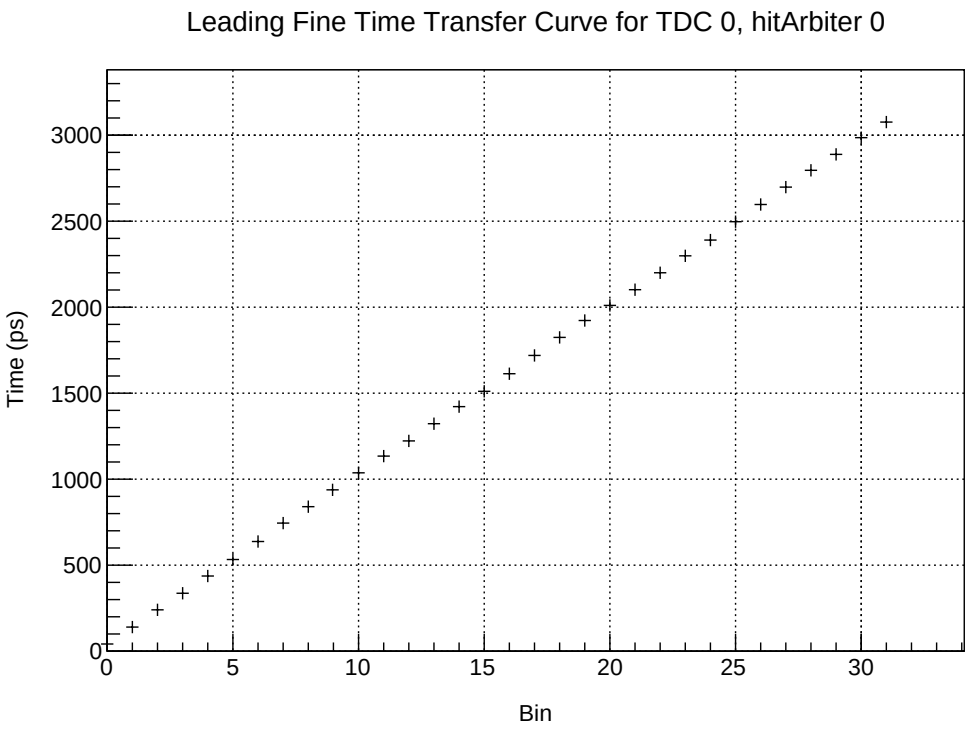
TDC Test Input: Code Density Histograms

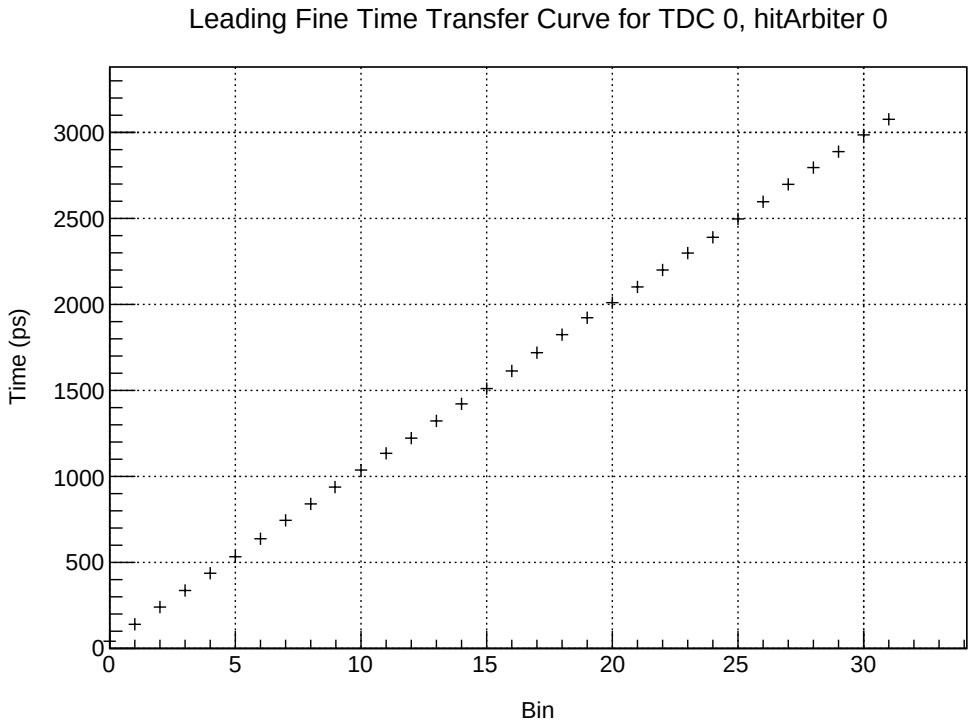




- 16 million random (unsynchronised) triggers
- bin content gives width estimate

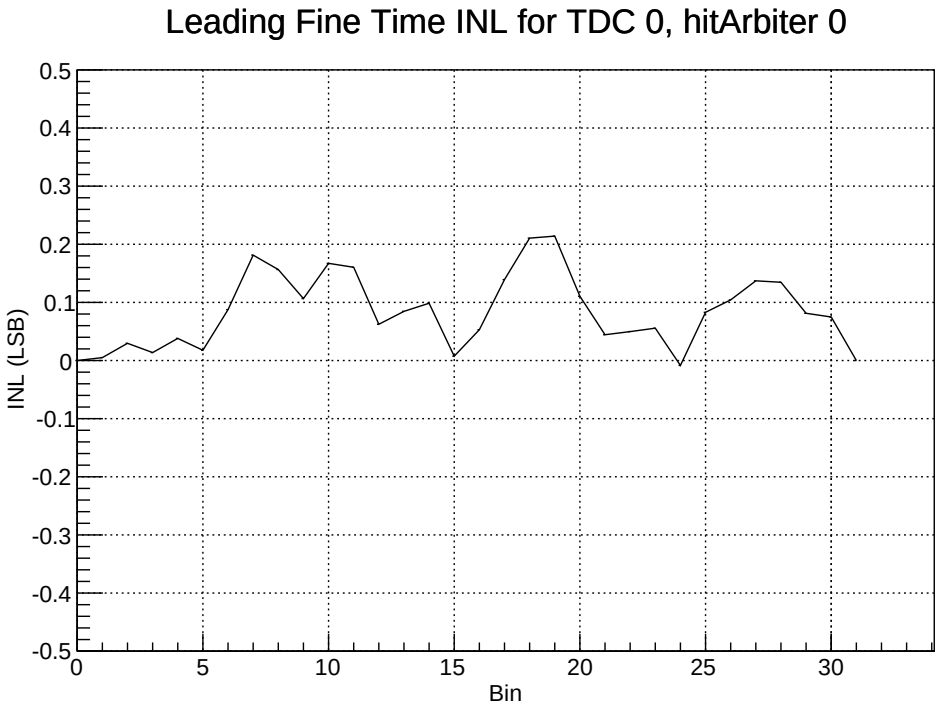
TDC Test Input: Transfer Curves

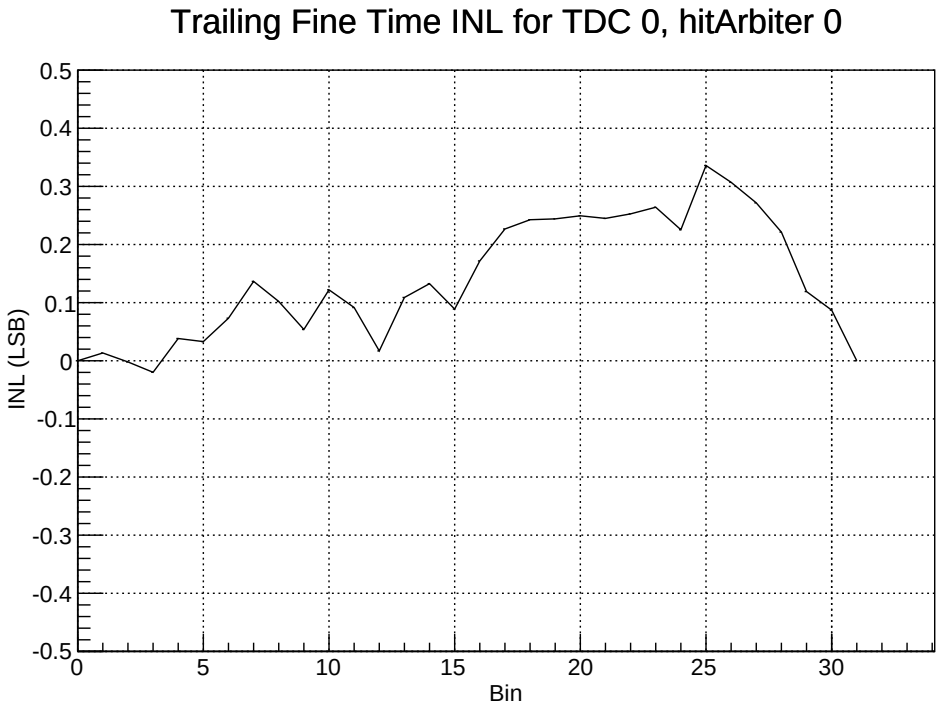




- Bin widths give the transfer curve

TDC Test Input: INL

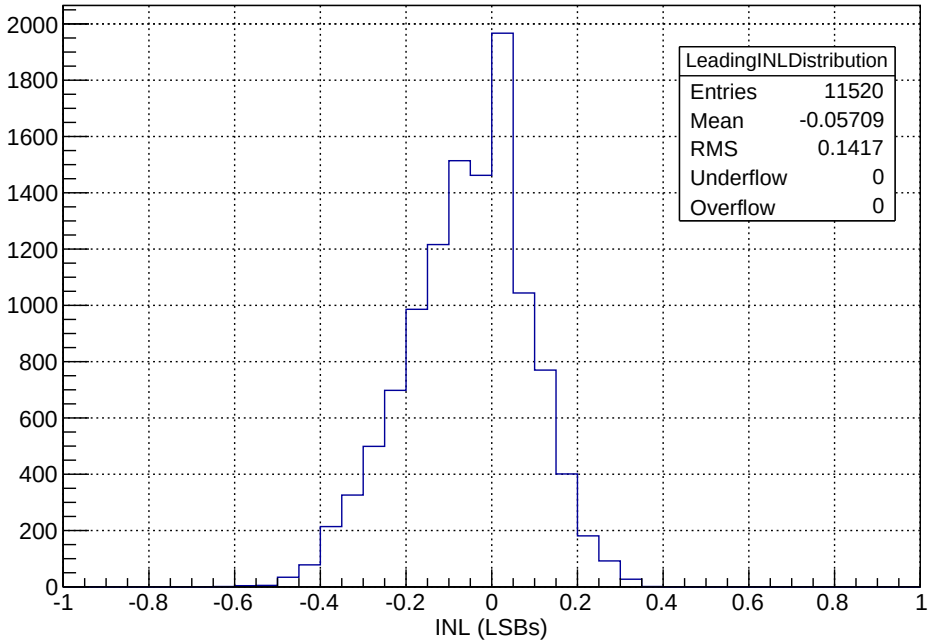




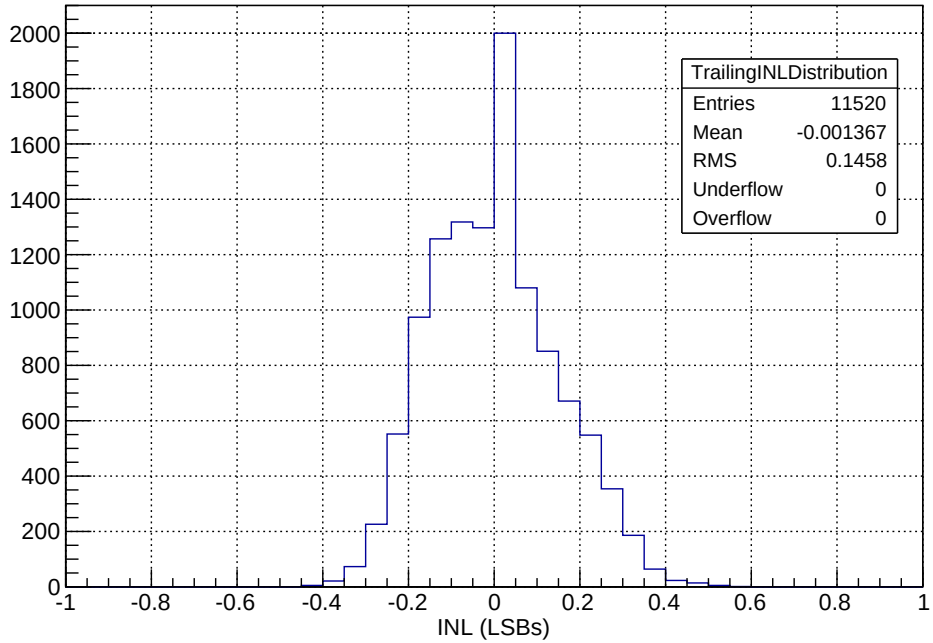
- transfer curves give the INLs

Leading/Trailing INL: All TDC Channels

Distribution of Leading Fine INL

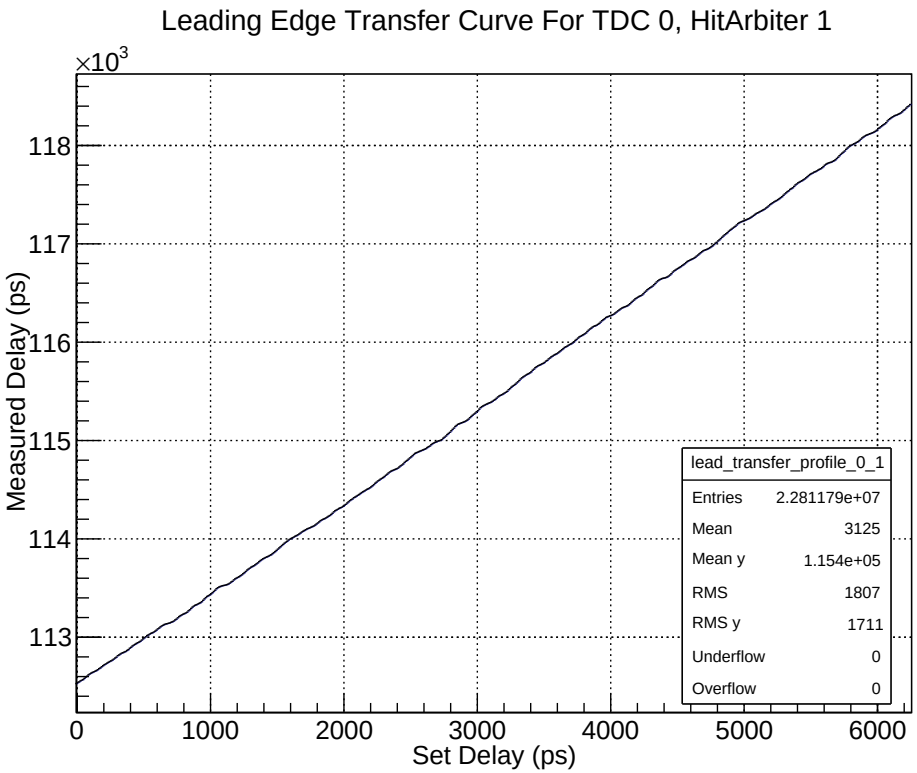


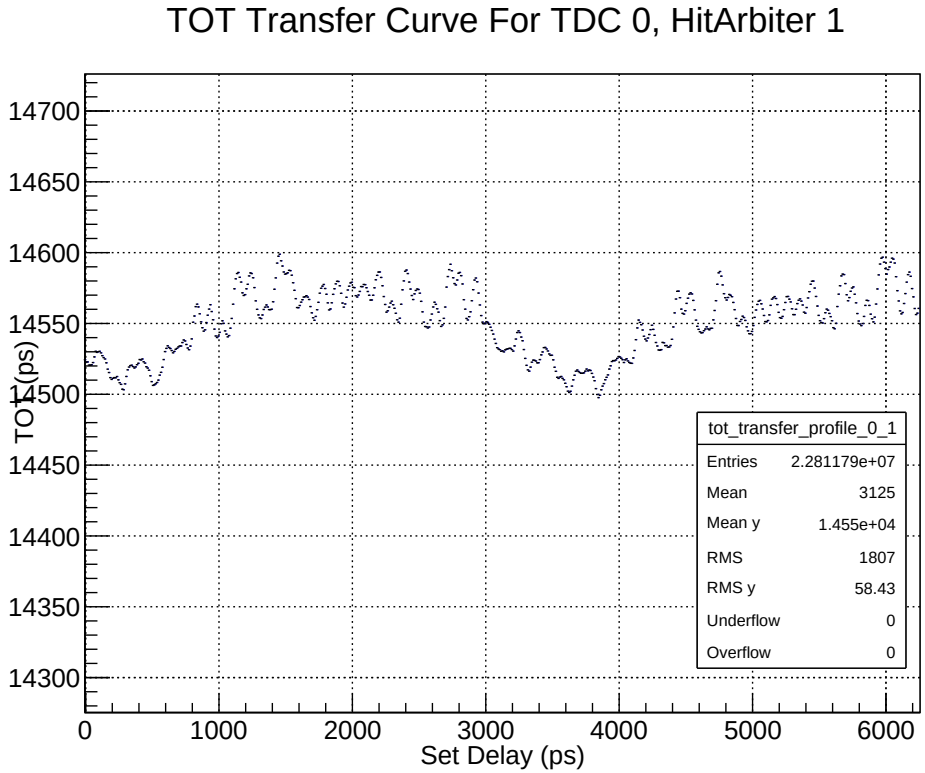
Distribution of Trailing Fine INL



RMS INL $\sim$ 0.15 LSBs

TDC Performance

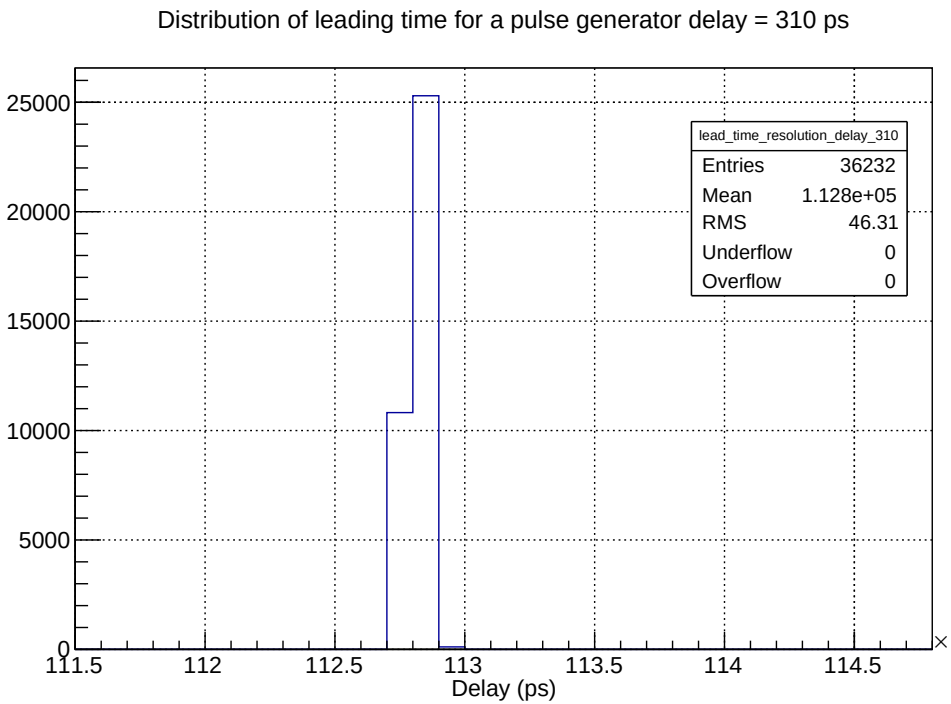


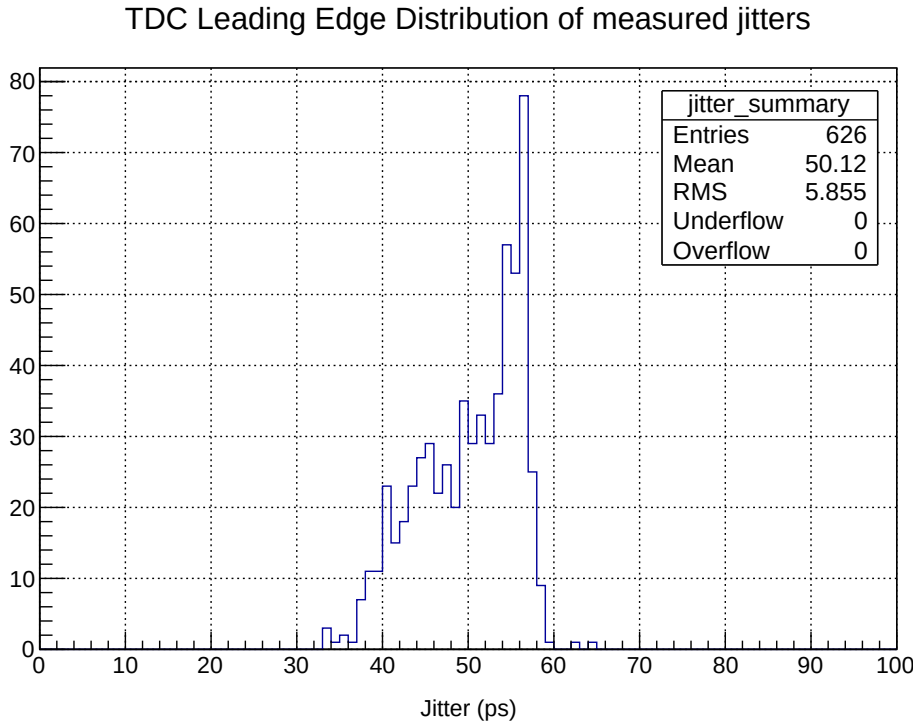


- Pixel Matrix not involved in measurement
- Two clock periods (2*3.125ns)

- Step: 10 ps
- 3.10^4 triggers/pt.

TDC Resolution

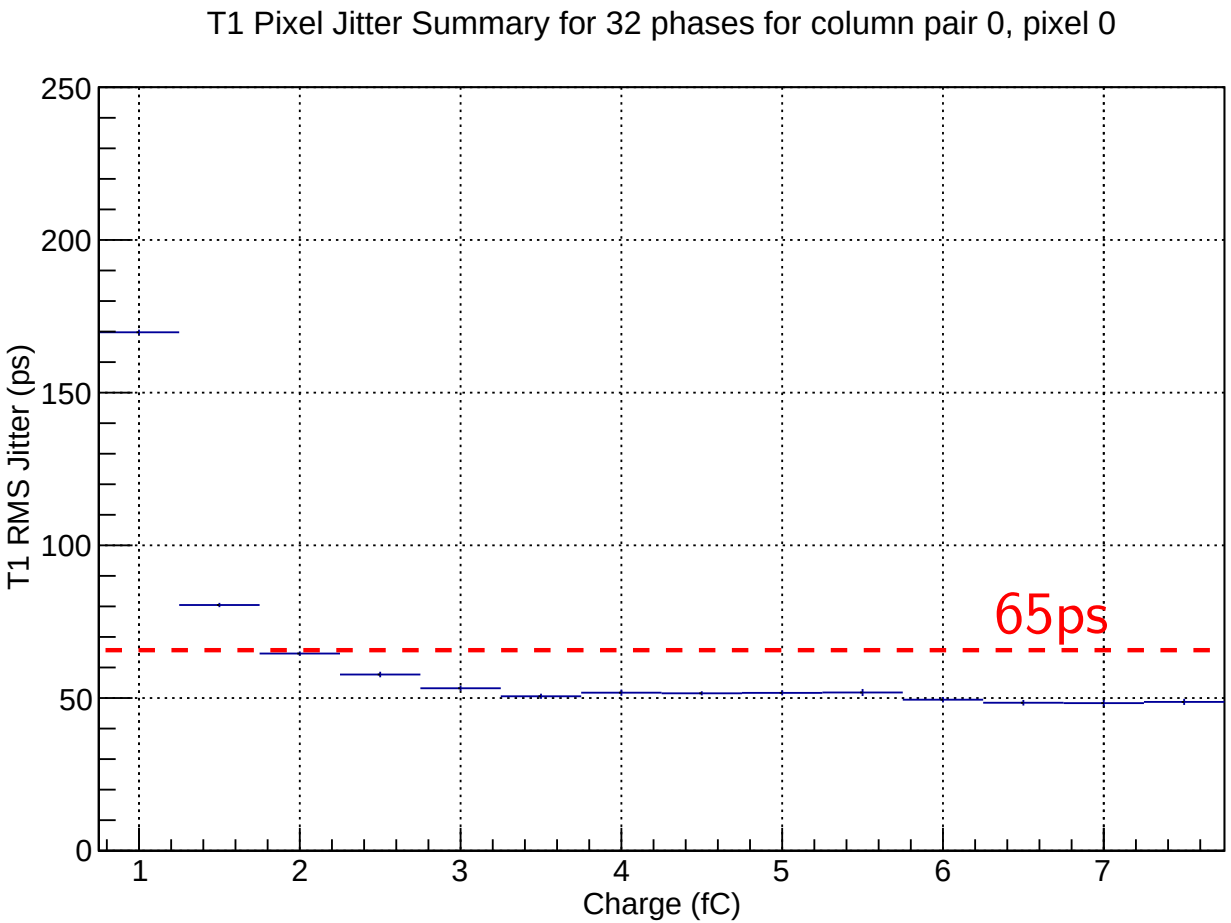




- Typical RMS $\sim 58\,ps$ RMS
- clock/pulse generator synchronisation contributes $\sim 30\,ps$ RMS
- contribution from signal distribution in the chip unknown

Full Chain Performance

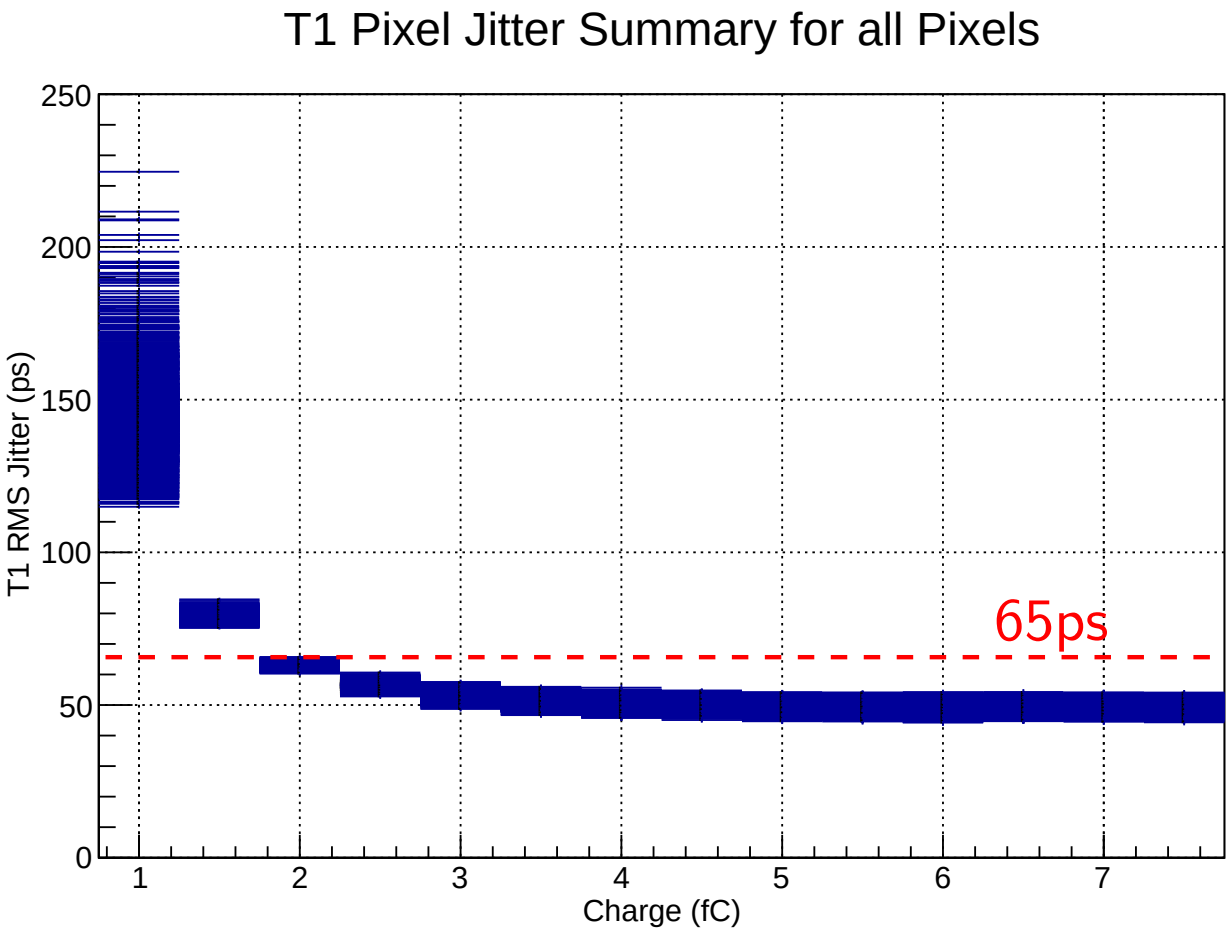
Full Chain Behaviour



$T_1(\text{RMS}) < 65\,\text{ps}$ at 2.5 fC

- trigger swept through full clk cycle
  - 32 phases
  - Step:100ps
- 10^4 triggers per phase
- No sensor present

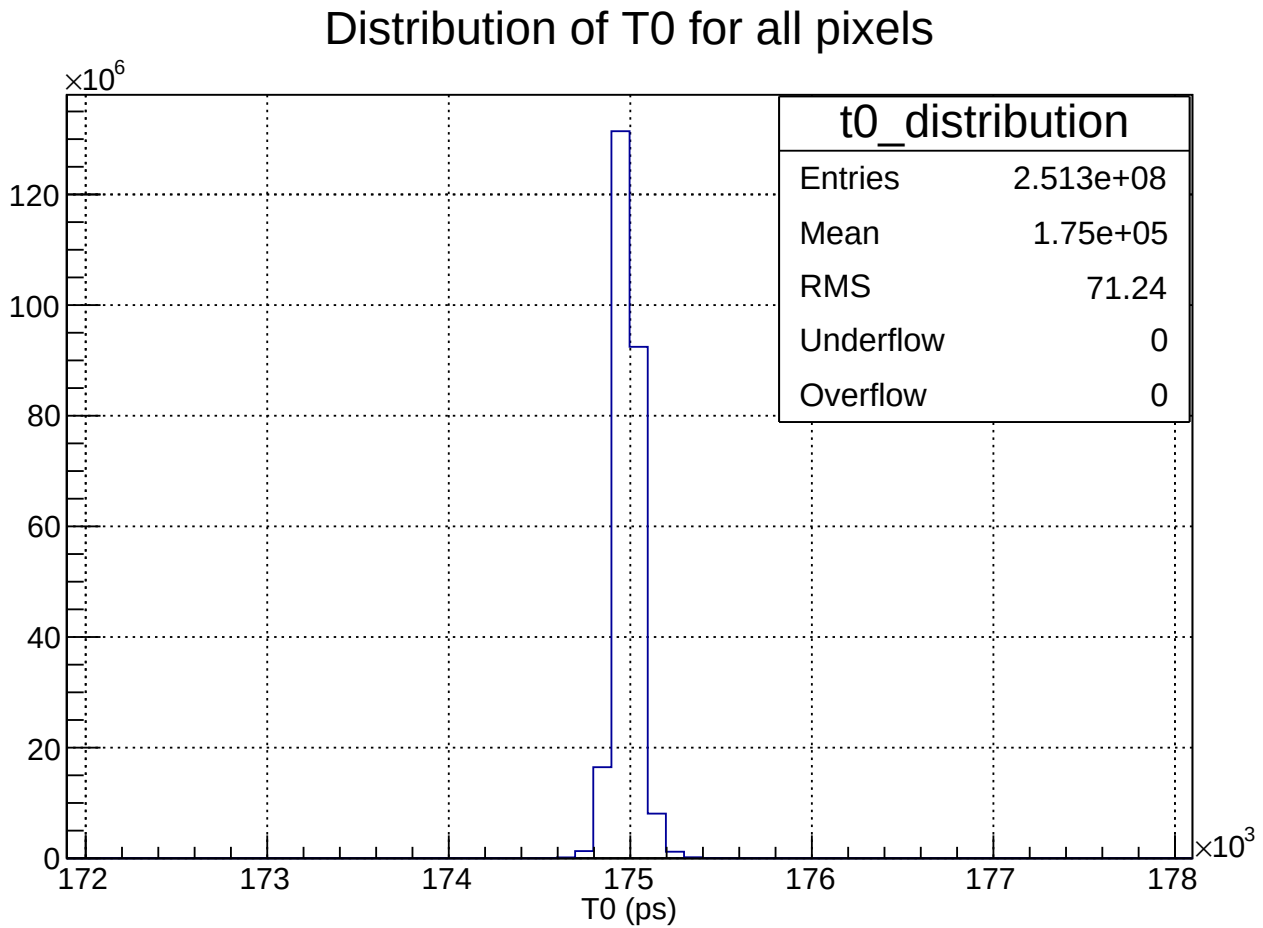
Full Chain Behaviour



$T_1(\text{RMS}) < 65\,\text{ps}$ at $2.5\,\text{fC}$

- trigger swept through full clk cycle
  - 32 phases
  - Step:100ps
- 10^4 triggers per phase
- No sensor present

TimeWalk-Corrected Time Resolution



- No sensor
- No sensor weighting
- Calibration done for every pixel
- $T_0 = T_1 - K(Q) * [T_2 - T_1]$
- Q = 1-7.5fC

"Whole Chip" Jitter $\sim$ 72 ps RMS

Introduction to NA62 and the GigaTracker

The TDCPix Chip Architecture

Measured Performance
- Pixel Jitter
- TDC Performance
- Full Chain Performance

Summary

Summary

- NA62: Ultra Rare Kaon decay measurement
  - huge beam rate $\rightarrow$ massive background reduction
  - GTK Time Tagging $<$200ps per station

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- TDCPix Architecture
  - 1800 pixel End-of-Column chip
  - 20mm x 12mm
  - self-triggering architecture
  - 4 x 3.2Gb/s on-chip serialisers

Summary

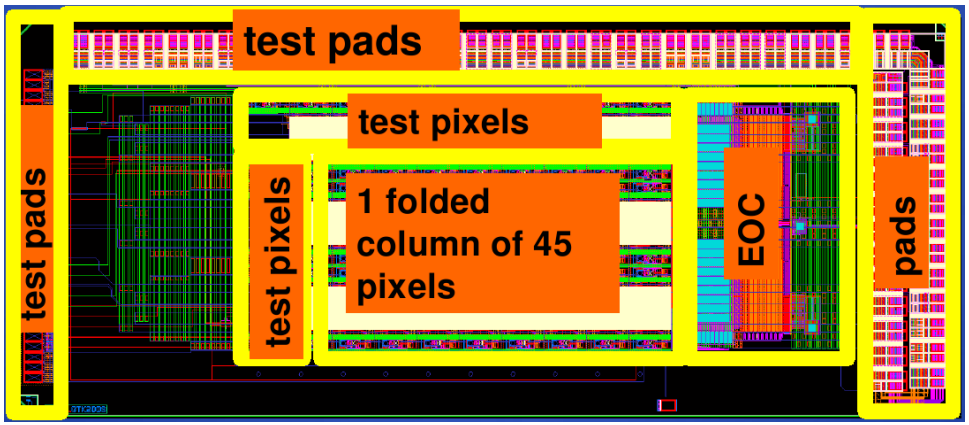
- NA62: Ultra Rare Kaon decay measurement
  - huge beam rate $\rightarrow$ massive background reduction
  - GTK Time Tagging <200ps per station
- TDCPix Architecture
  - 1800 pixel End-of-Column chip
  - 20mm x 12mm
  - self-triggering architecture
  - 4 x 3.2Gb/s on-chip serialisers
- TDCPix Performance is excellent
  - First working silicon
  - Pixel jitter $<$ 60ps at 2.5fC
  - TDC gives <60 ps rms time resolution
  - Full chain works as expected $<$ 65 ps rms at 3.5fC
  - Time Walk Correction Works as expected
  - "Whole Chip" Resolution $\sim$ 72 ps RMS

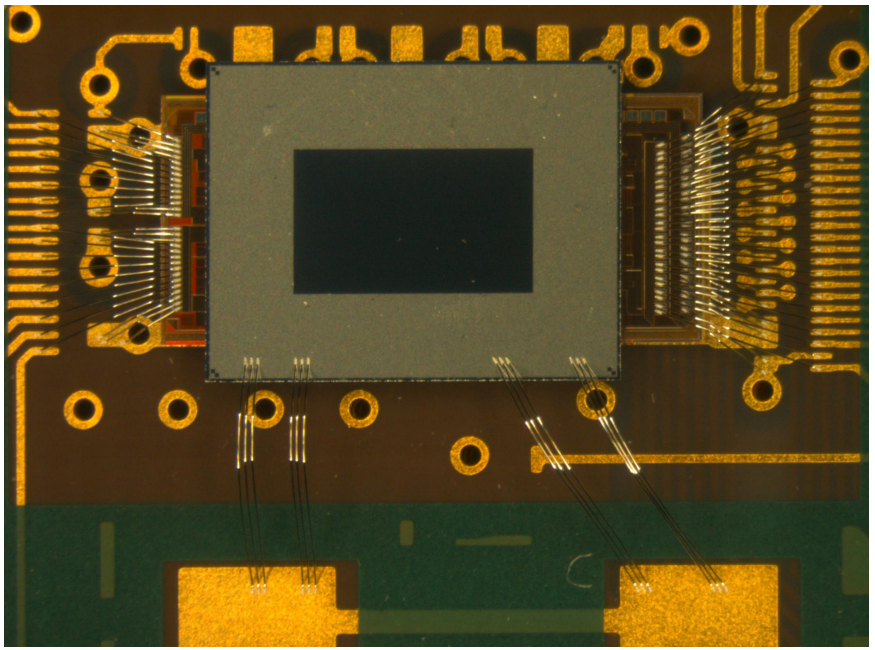
Thanks for your attention!!

Backup Slides

Demonstrator

EoC Chip & Assembly

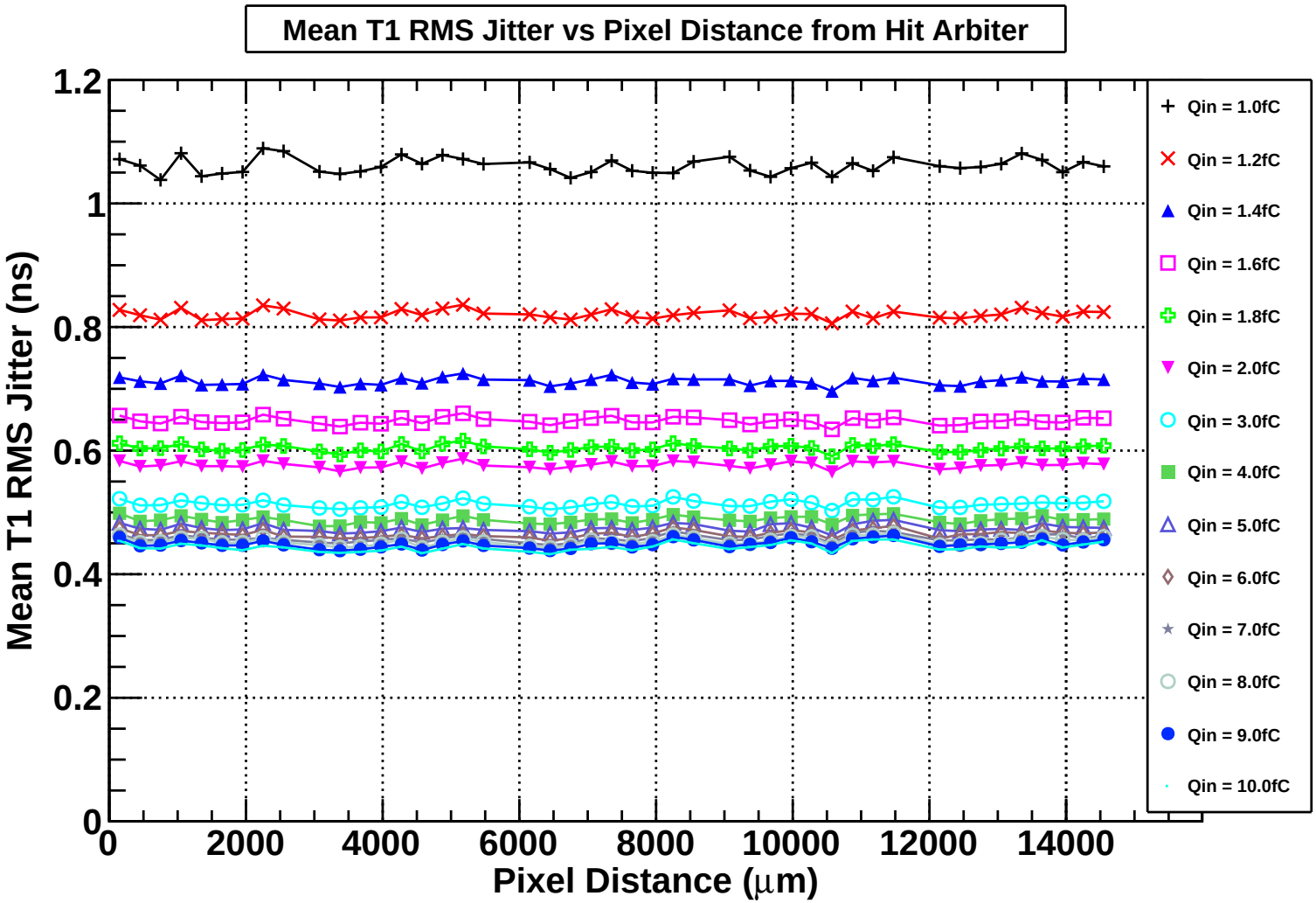




- What is the limit of the timing resolution attainable?
- Where does this limit come from?

Summary of Results

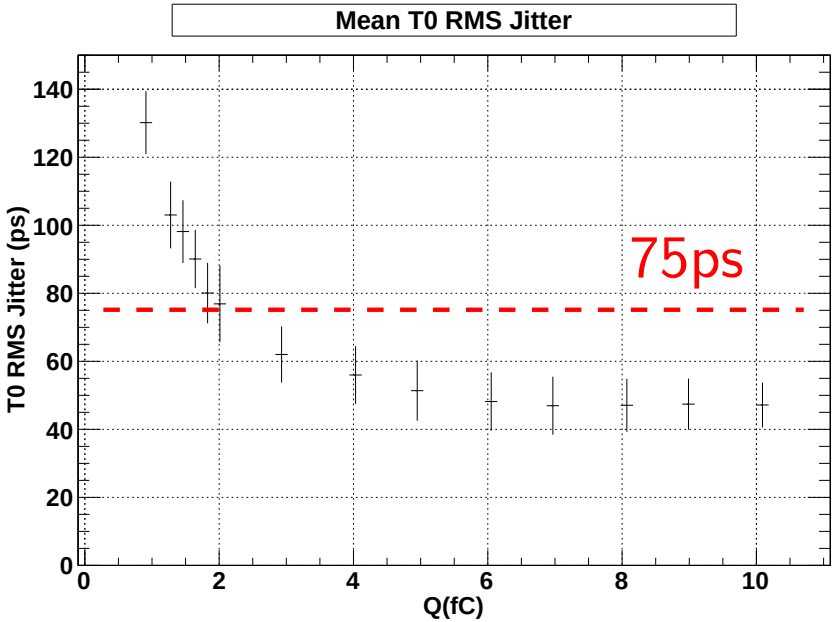
Transmission Line Uniformity T_1 RMS Jitter: ASIC



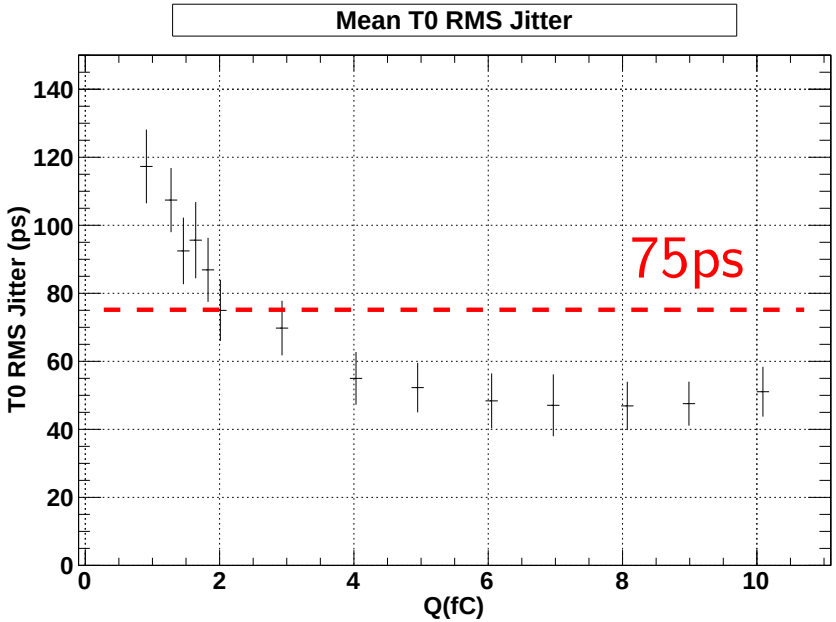
No systematic deterioration of signal quality with distance.

RMS T_0 Jitter Vs Q: Assembly (@ 300V) + Laser

Pixel 0: Far from EoC



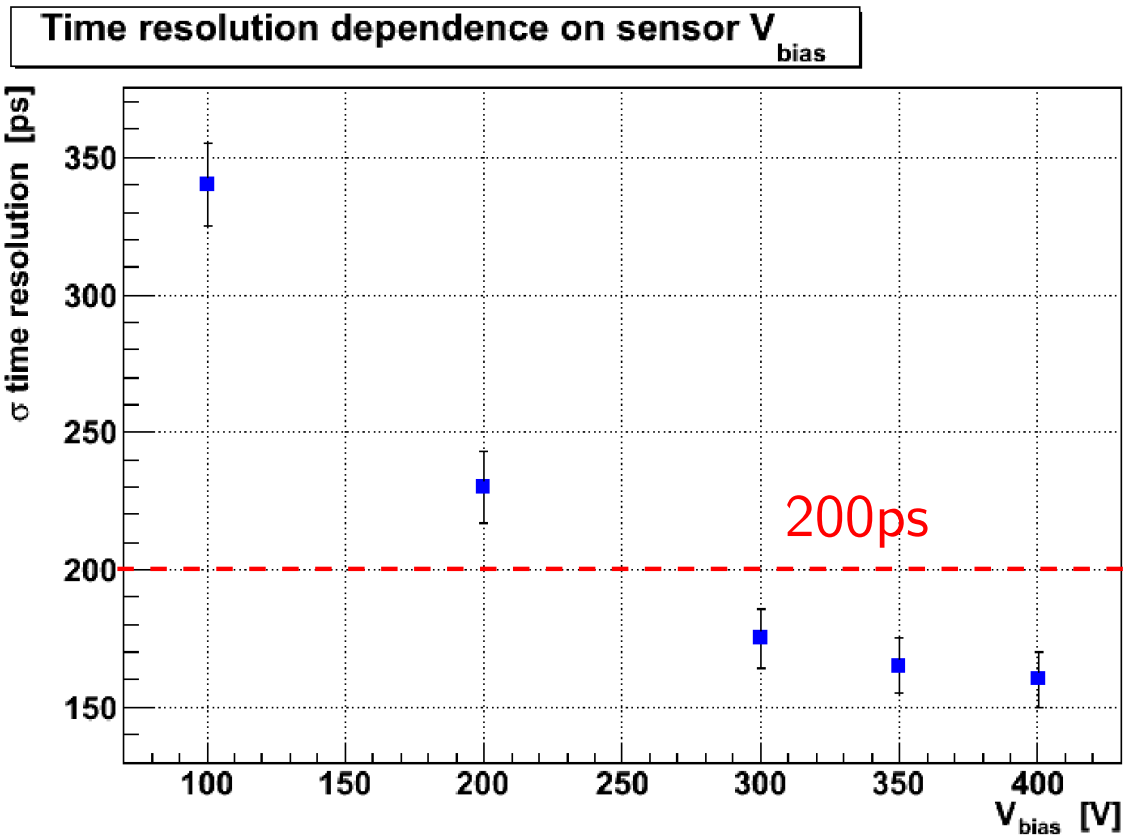
Pixel 44: Close to EoC



- Full event time reconstruction done
- EoC activity doesn't feed through to the pixels

- detector bias $= 300\,V$
- average case $\sim 75\,ps$ at $2.4\,fC$

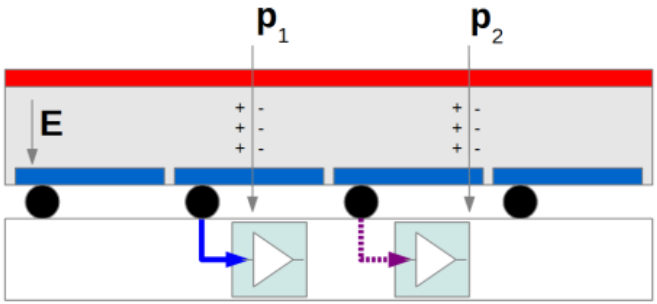
Beam Test: Time Resolution Vs Detector Bias

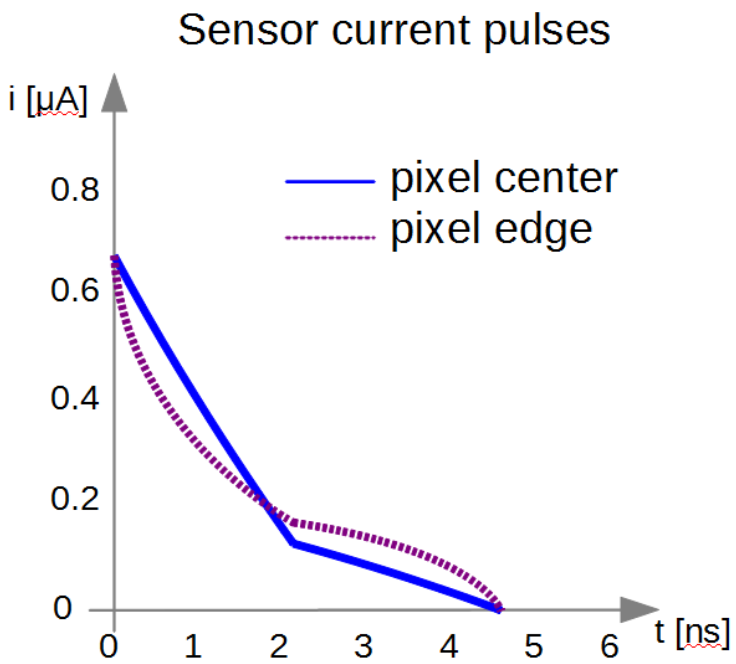


at $300\,V$ average performance is $175\,ps\,RMS$

M. Fiorini

Time Resolution Limits

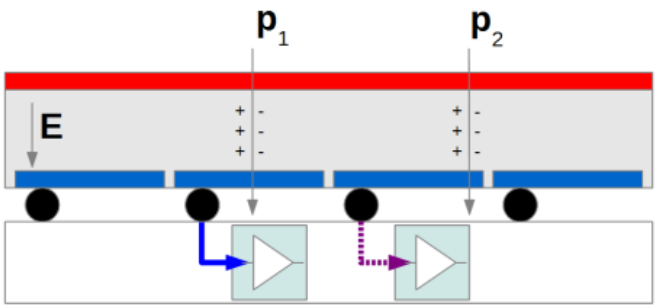


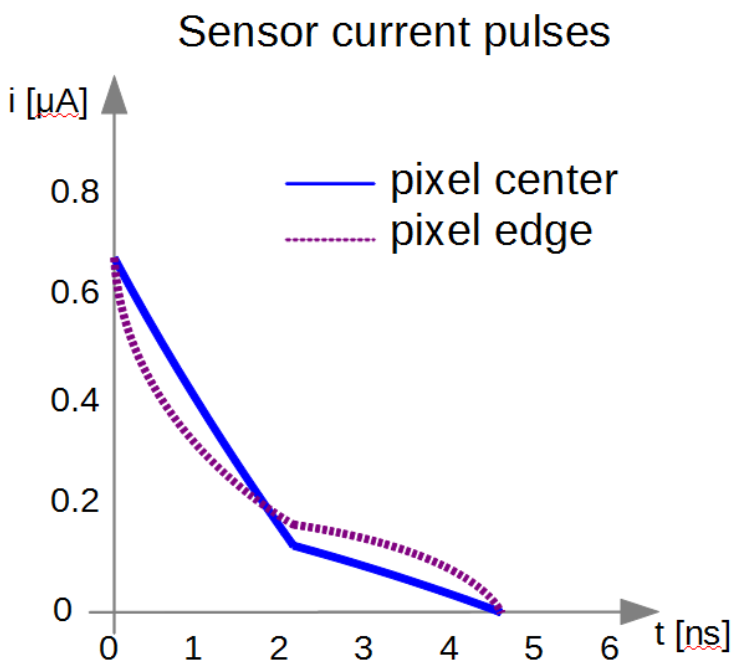


- induced current pulse on electrode changes shape
  - pre-amp output changes shape
  - adds ∼85ps

G. Aglieri Rinella

Time Resolution Limits

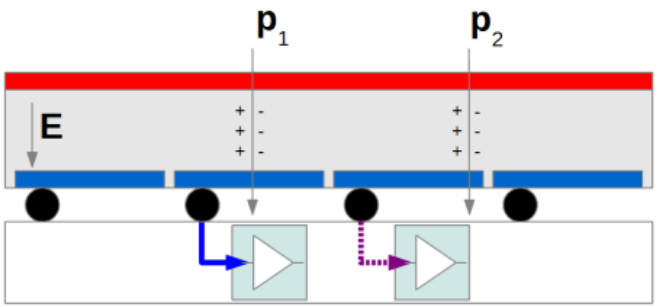


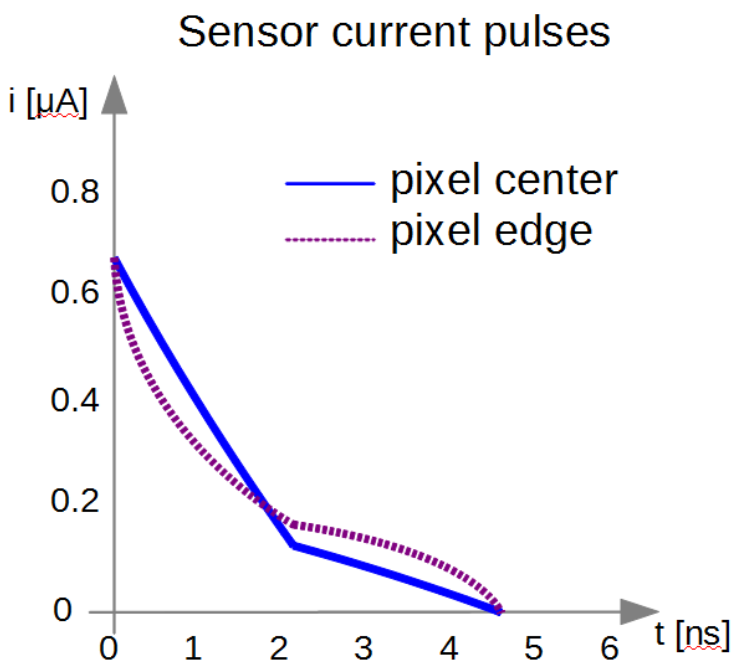


- induced current pulse on electrode changes shape
  - pre-amp output changes shape
  - adds ∼85ps
- Charge straggling also contributes
  - inhomogeneities in charge deposition
  - adds $>$ 60ps

G. Aglieri Rinella

Time Resolution Limits





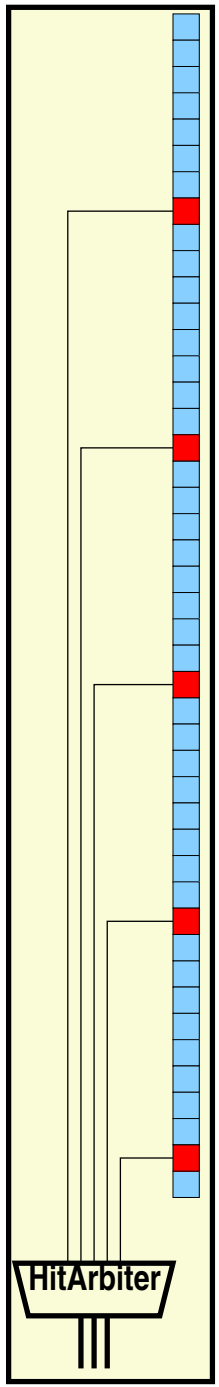
- induced current pulse on electrode changes shape
  - pre-amp output changes shape
  - adds ∼85ps
- Charge straggling also contributes
  - inhomogeneities in charge deposition
  - adds $>$ 60ps
- uncorrectable contributions for current sensor

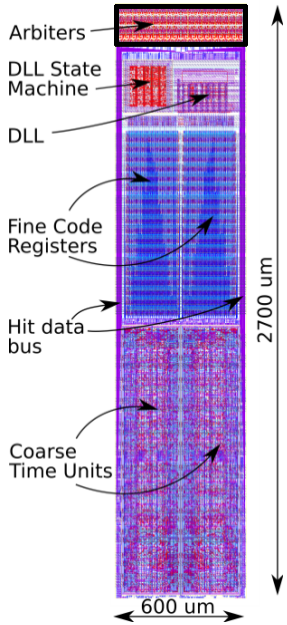
G. Aglieri Rinella

Hit Arbiter

TDC: Hit Arbiter

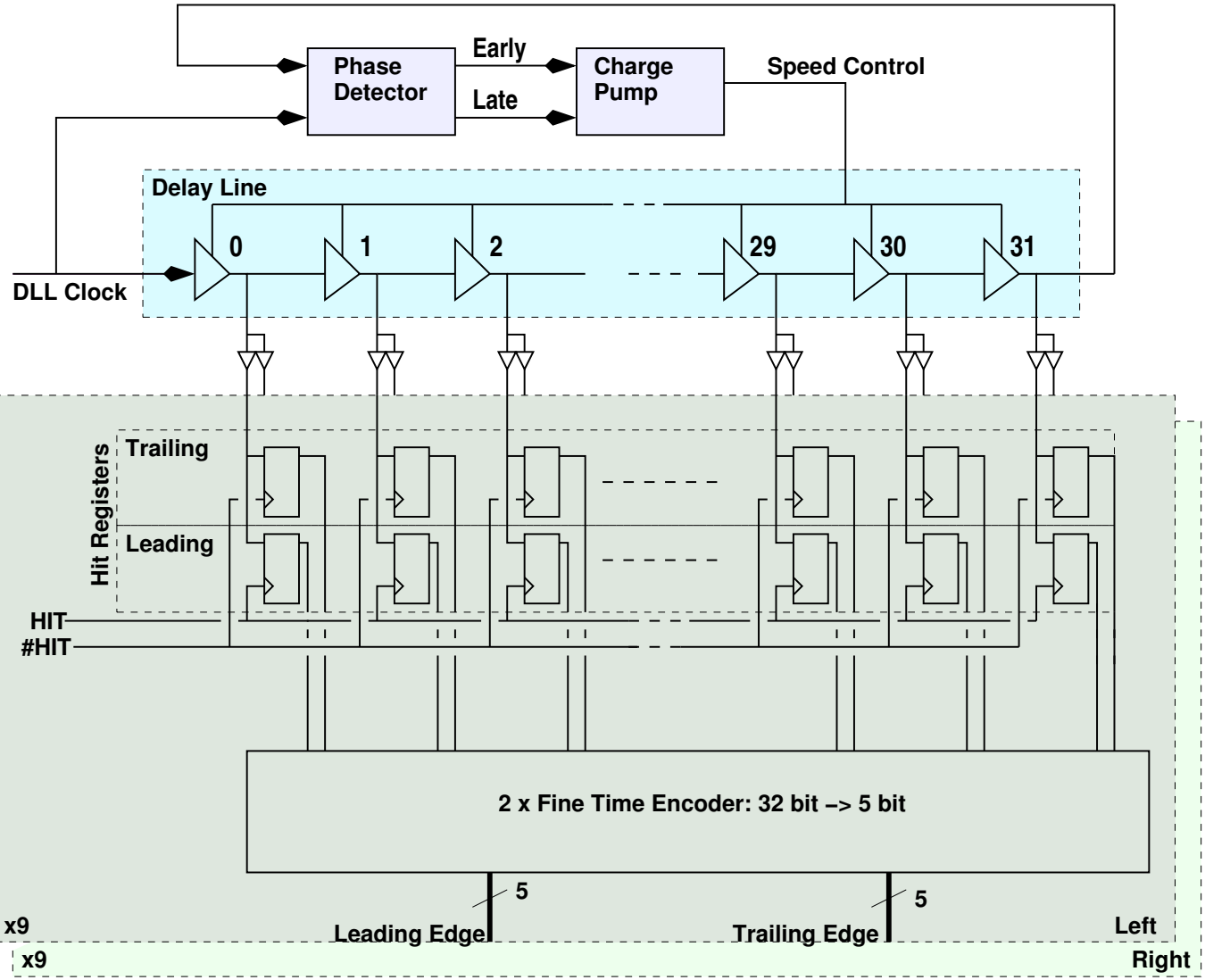
- fully asynchronous
  - timing information preserved
- 5 pixel + 1 test inputs
- hit signal
- 5 bit hit address + 5 bit pileup
- non-adjacent pixels connected to adjacent channels

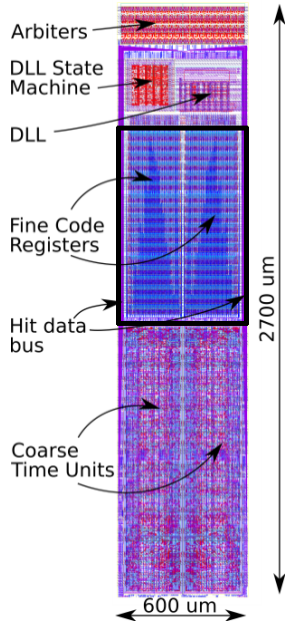




DLL & Hit Registers

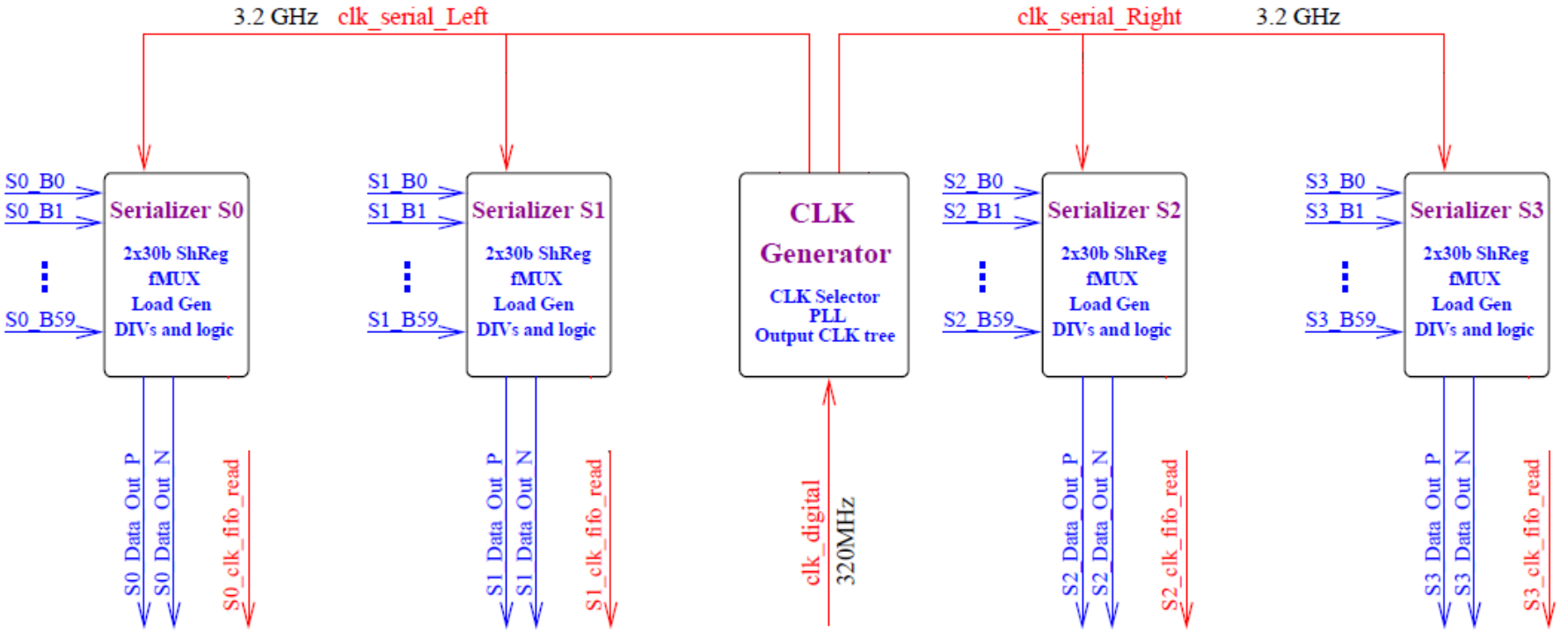
TDC: DLL & Fine Registers

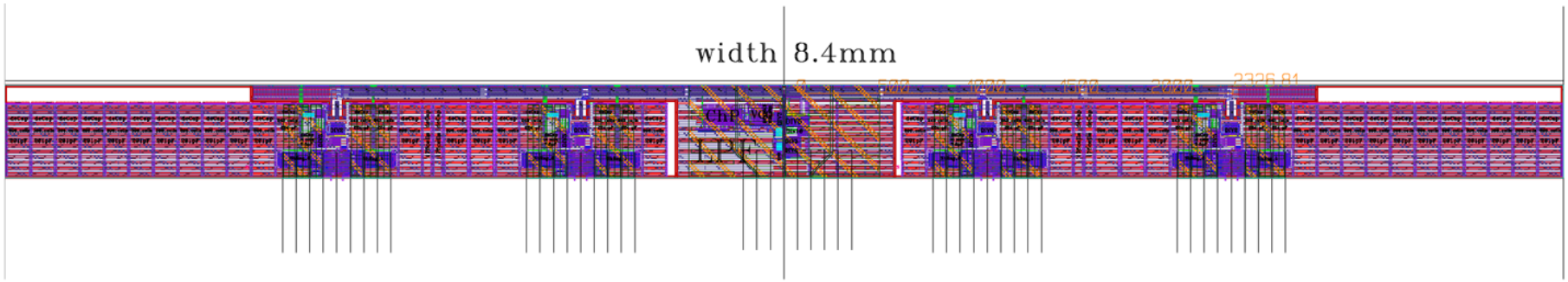




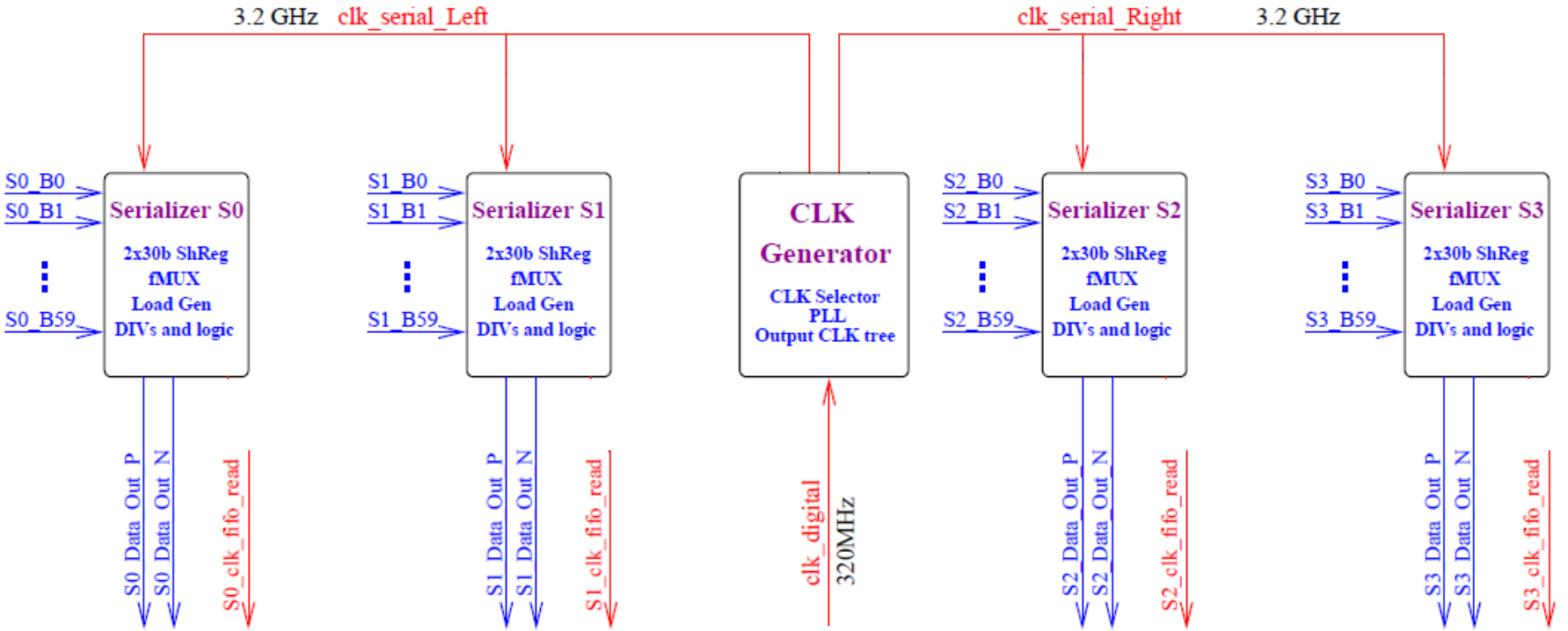
PLL & Serialisers

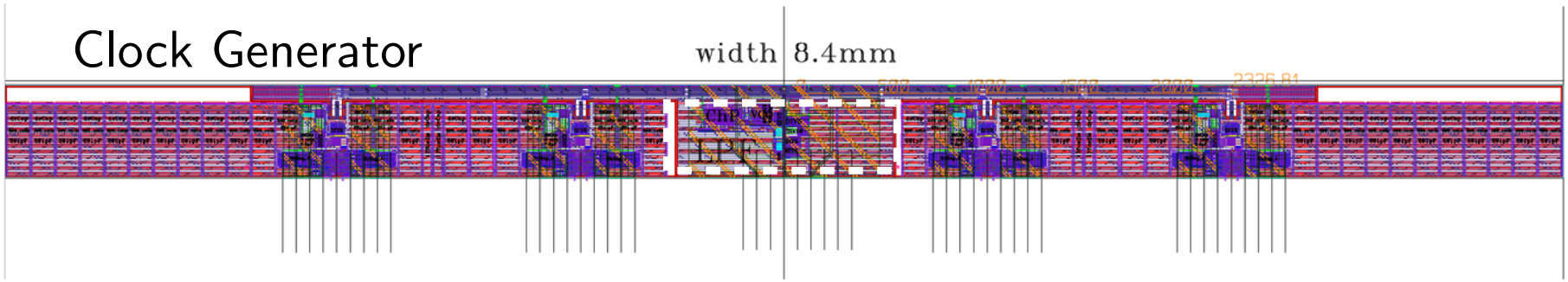
PLL and Serialisers



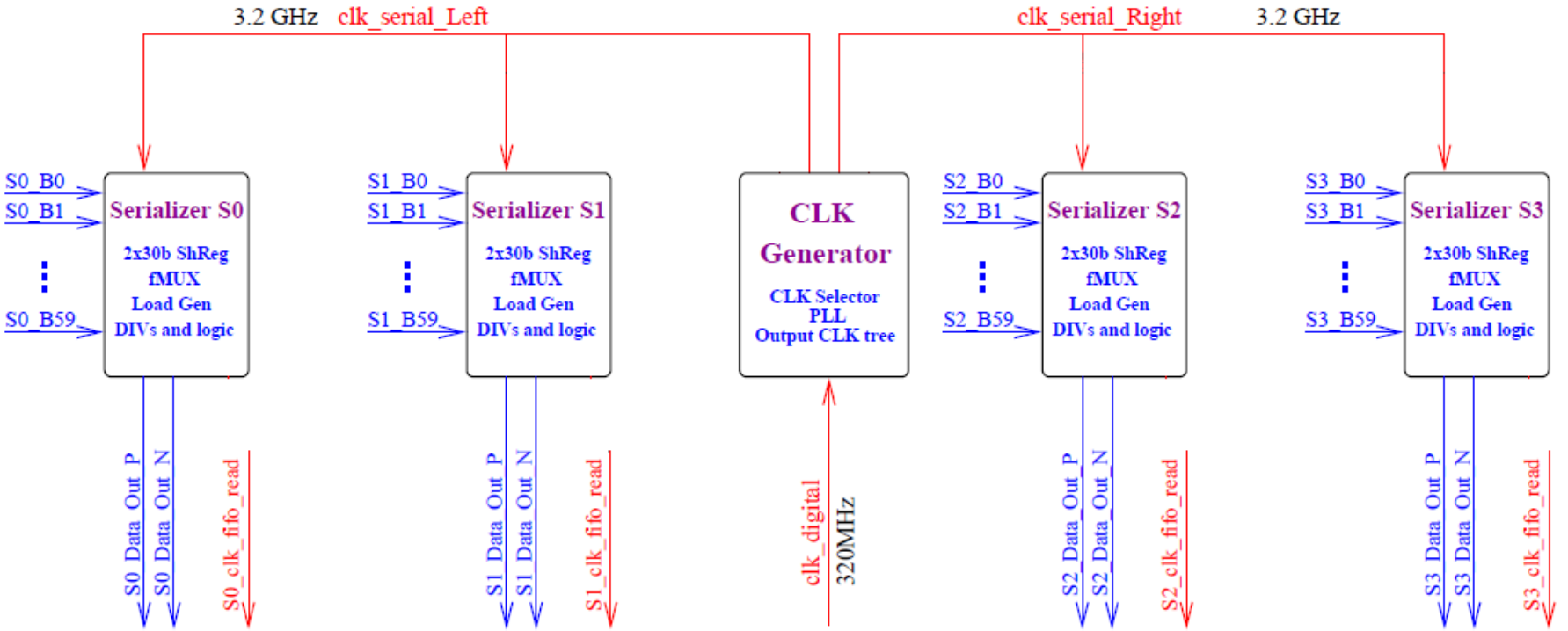


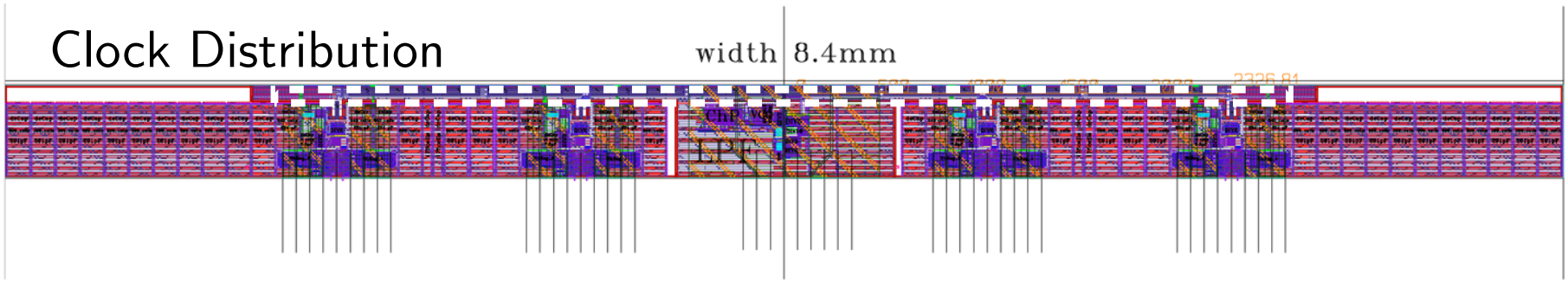
PLL and Serialisers



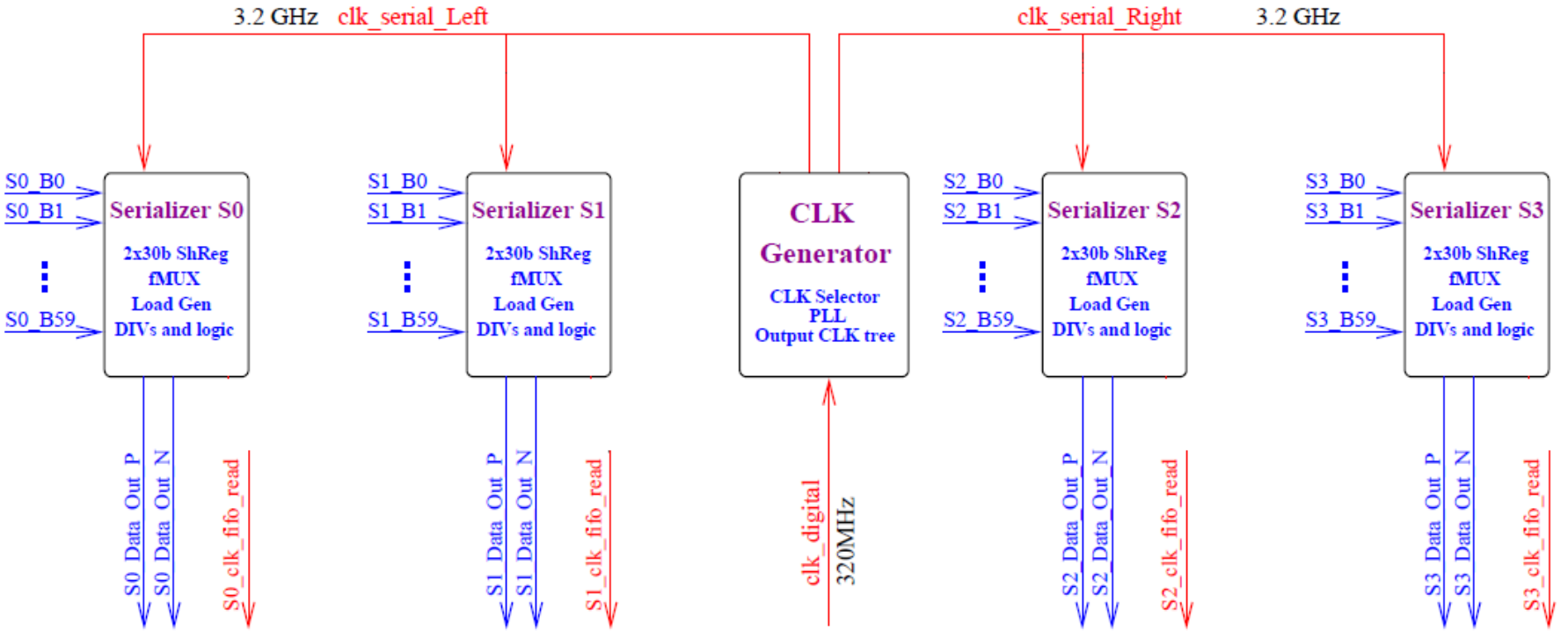


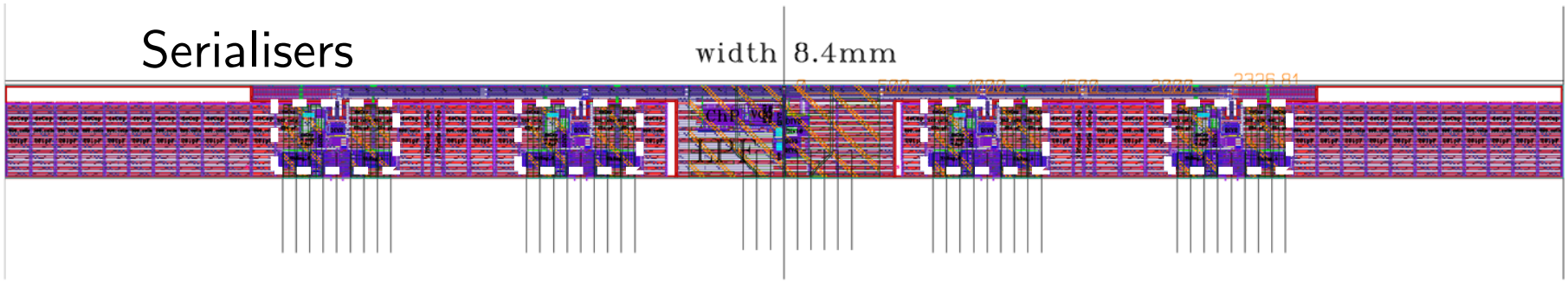
PLL and Serialisers



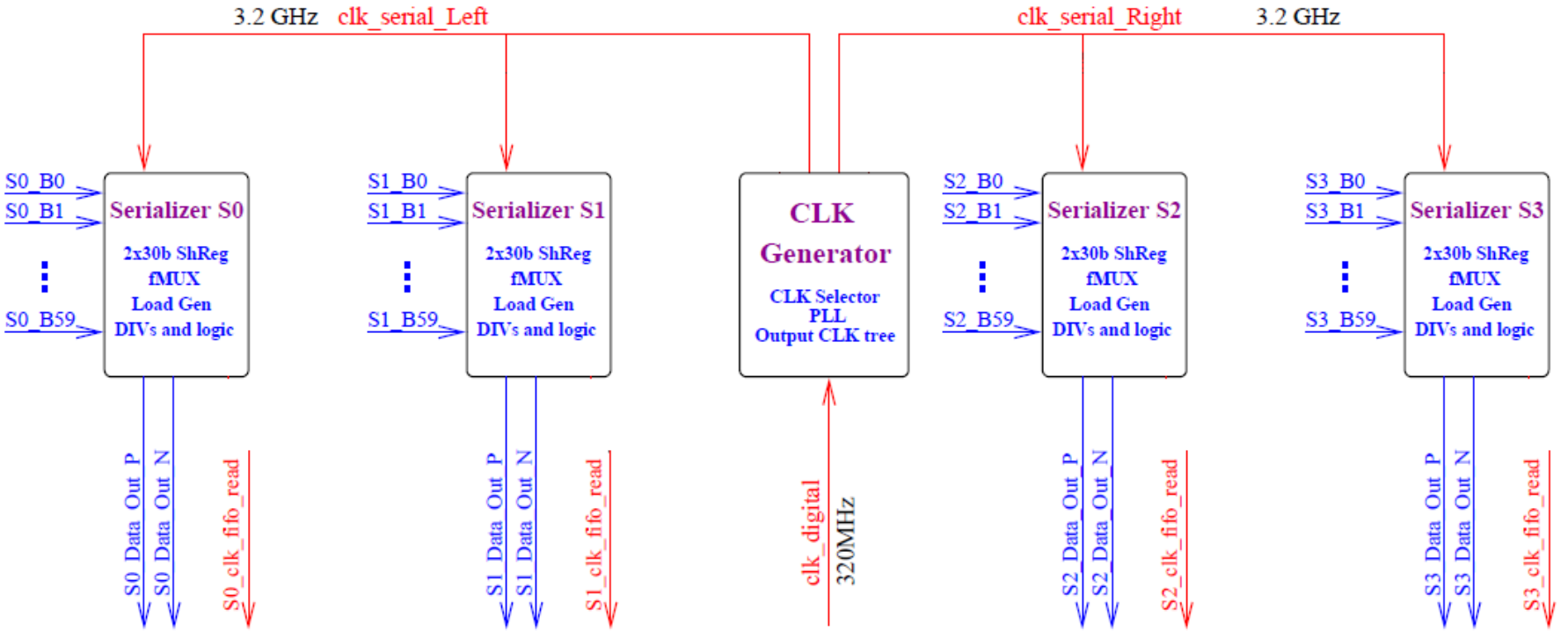


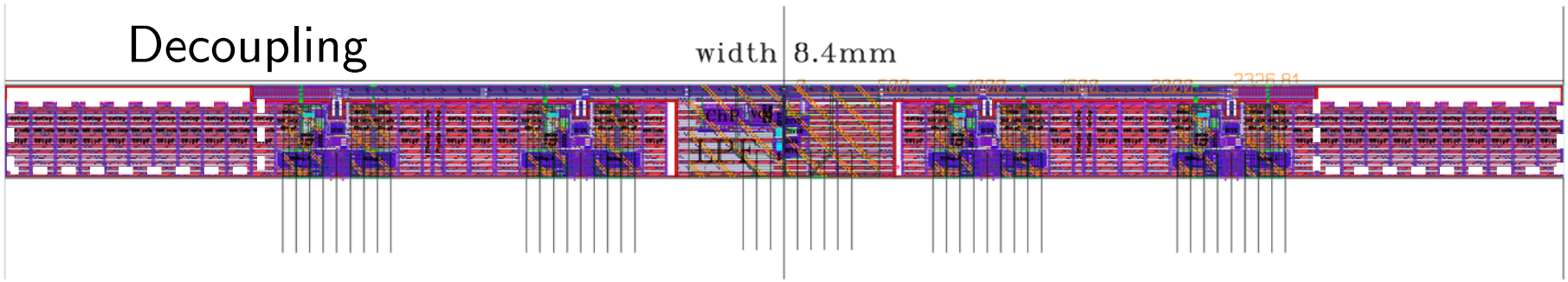
PLL and Serialisers



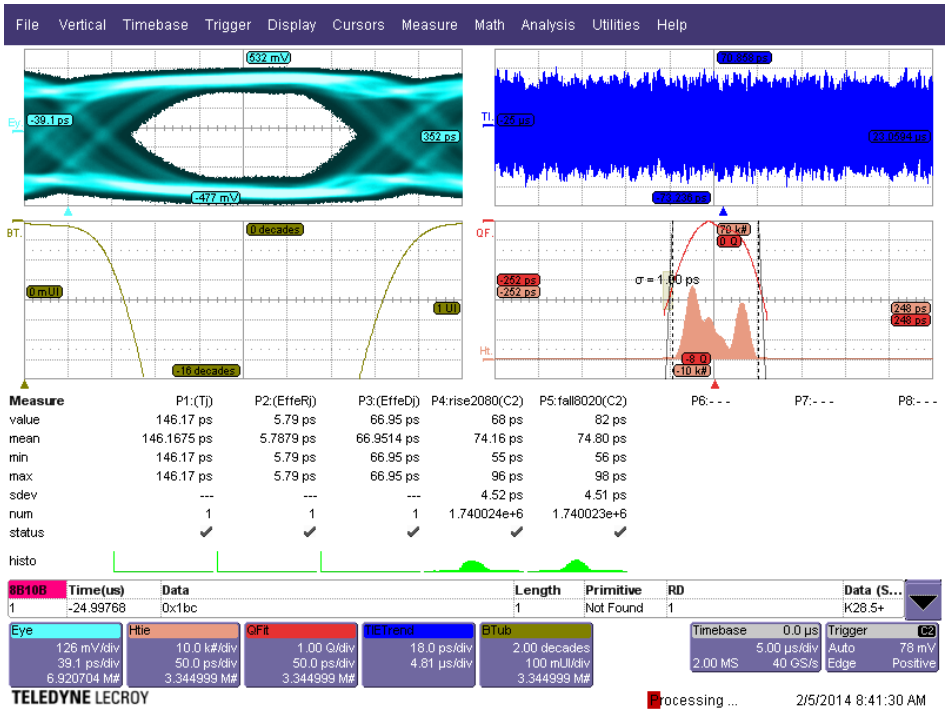


PLL and Serialisers





Serial Outputs at 3.2Gb/s

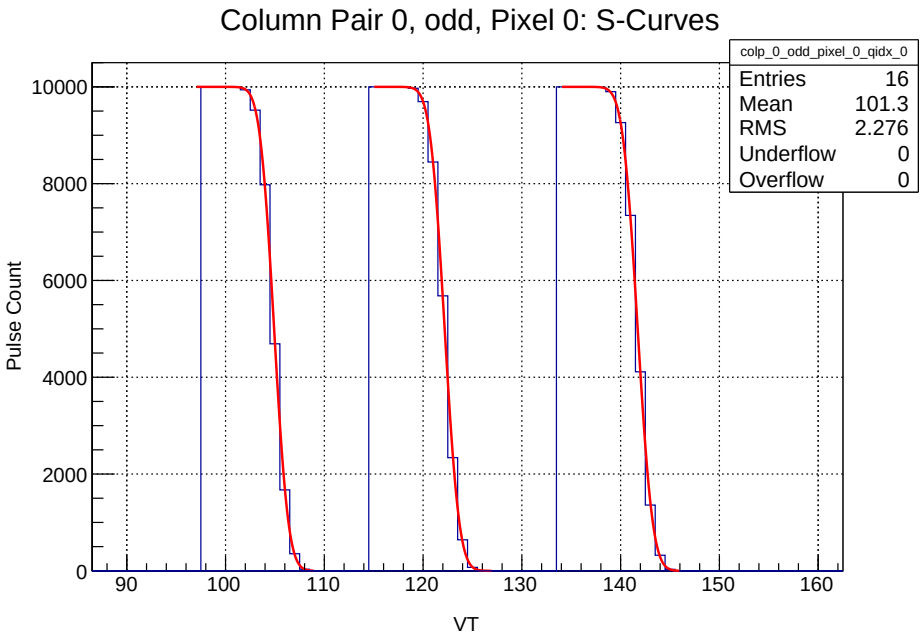


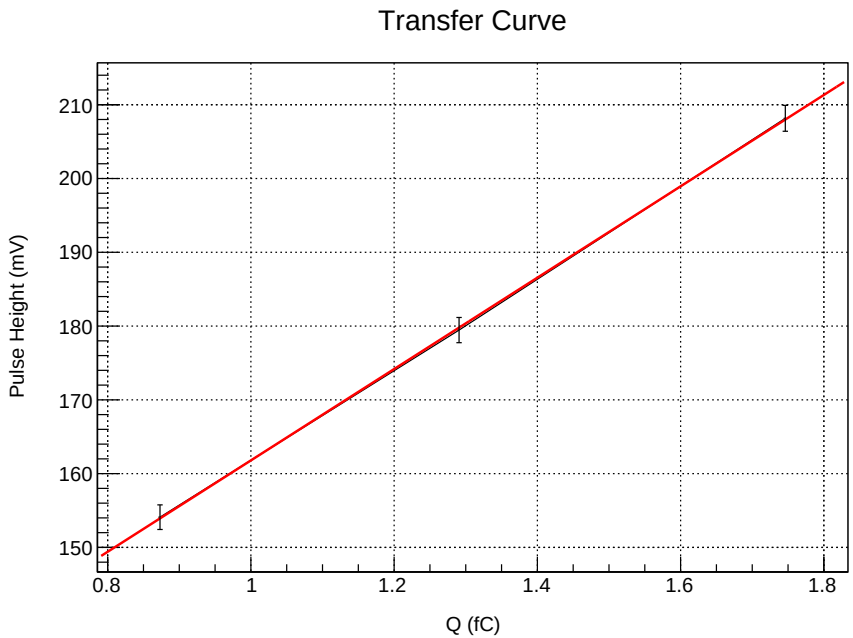
- Idle words correct
  - synchronisation works

- Total Jitter $< 150\,\text{ps}$
- FPGA GTX recv. lock reliably
- DAQ works reliably

Pixel Behaviour

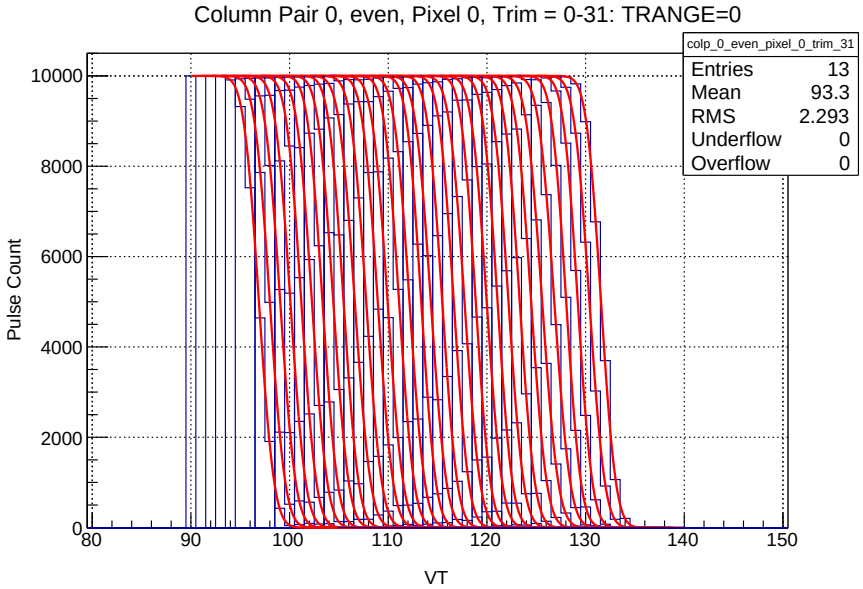
S-Curves → Pre-Amp Transfer Function

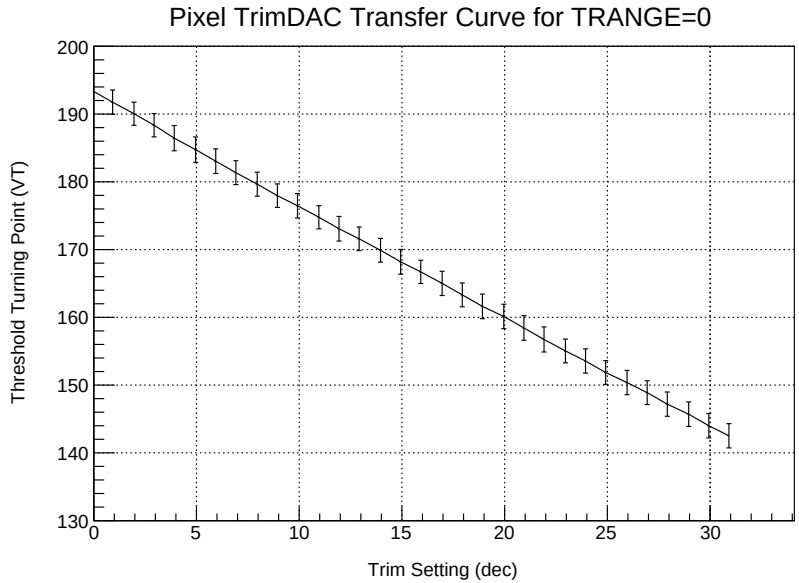


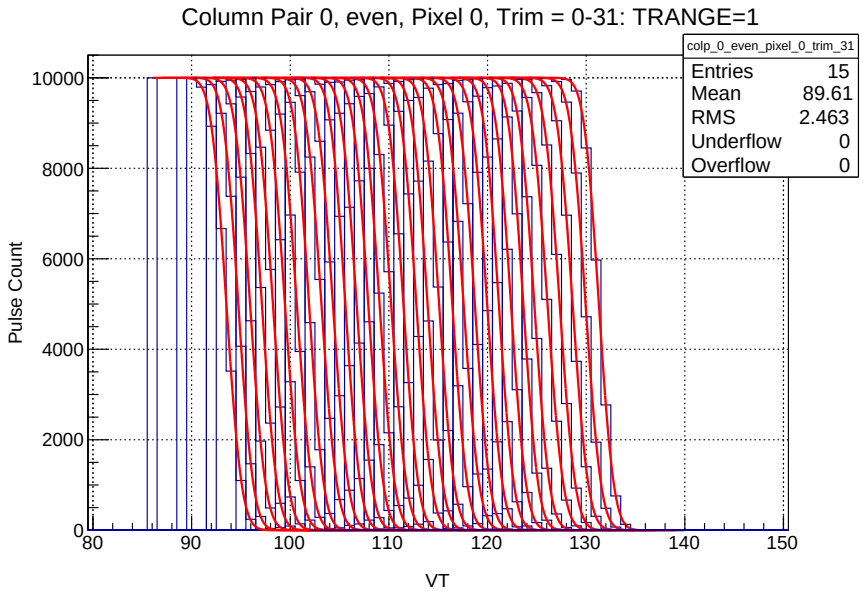


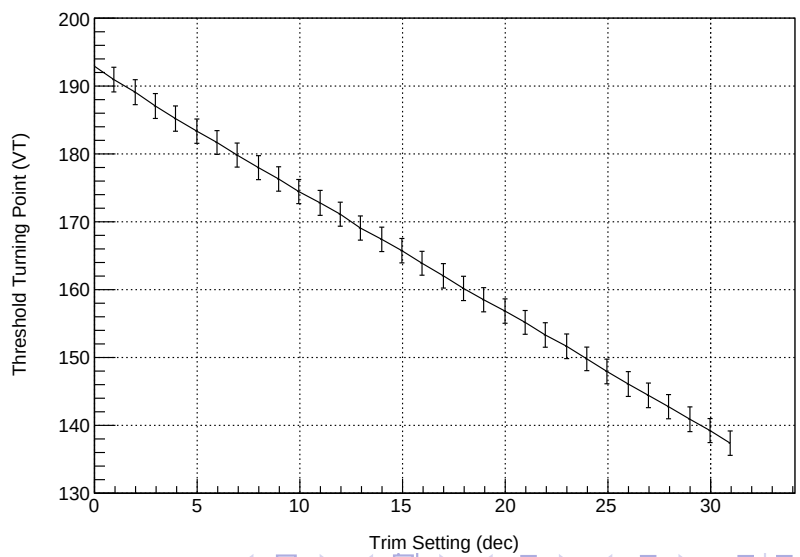
- $Q_{injected}$ adjusted for CAL DAC gain
- Transfer fit → discriminator offset and front end gain
- Polarity setup for a hole signal
  - P-on-N sensor (baseline)
  - "electron" polarity works too

Trim and TRANGE Functionality

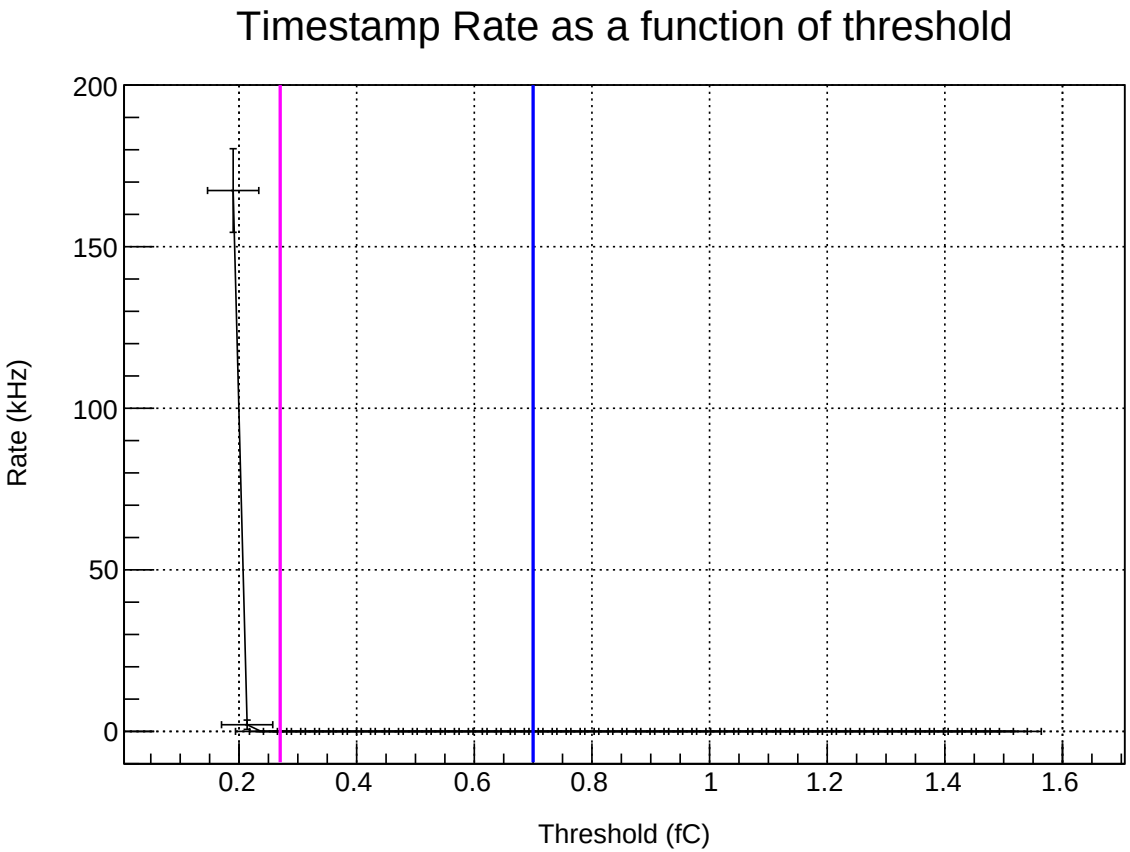


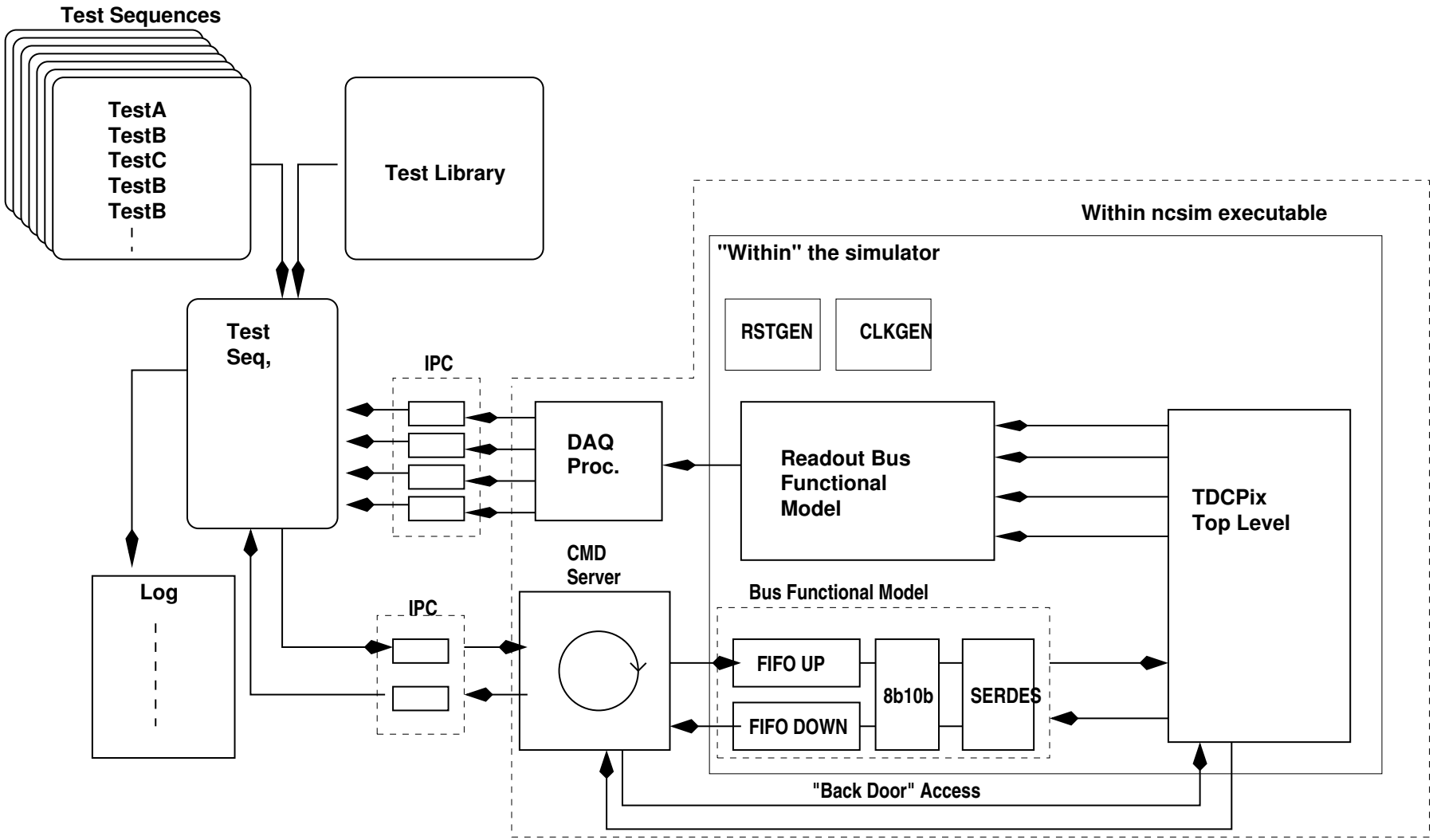






How low will the threshold go?



- All pixels enabled (& trimmed)
- Pink: minimum threshold $\sim 0.26\, fC$ ($1600e^-$)
- Blue: nomimal threshold $0.7\, fC$

Top Level Test Bench