The FPGA based Trigger and Data Acquisition system for the CERN NA62 experiment

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on behalf of the NA62 TDAQ group

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Outline

- The NA62 experiment

- The NA62 TDAQ system

- The FPGA based common system
  - TEL62 board
  - TDCB
  - TALK board

The NA62 experiment

- NA62 main goal: measure the BR of the ultra-rare FCNC process $K^+ \to \pi^+ \nu \bar{\nu}$ with 10% accuracy. This can be achieved collecting O(10^2) events in 2 years of data taking.

- SM prediction: BR($K^+ \to \pi^+ \nu \bar{\nu}$) = (0.781±0.075±0.029)x10^{-10}
  Experimental result: BR($K^+ \to \pi^+ \nu \bar{\nu}$) = (1.73+1.15-1.05)x10^{-10}
- The process offers an highly sensitive test of the Standard Model and is a clean probe for the non-trivial structure of physics beyond the SM.
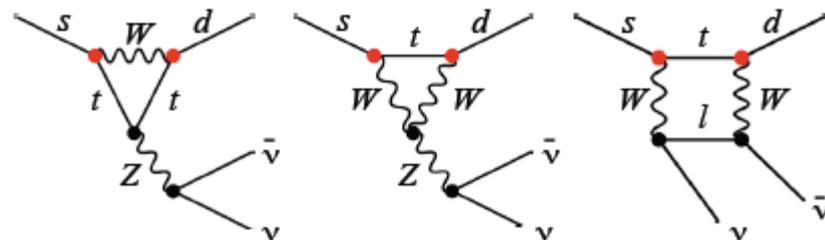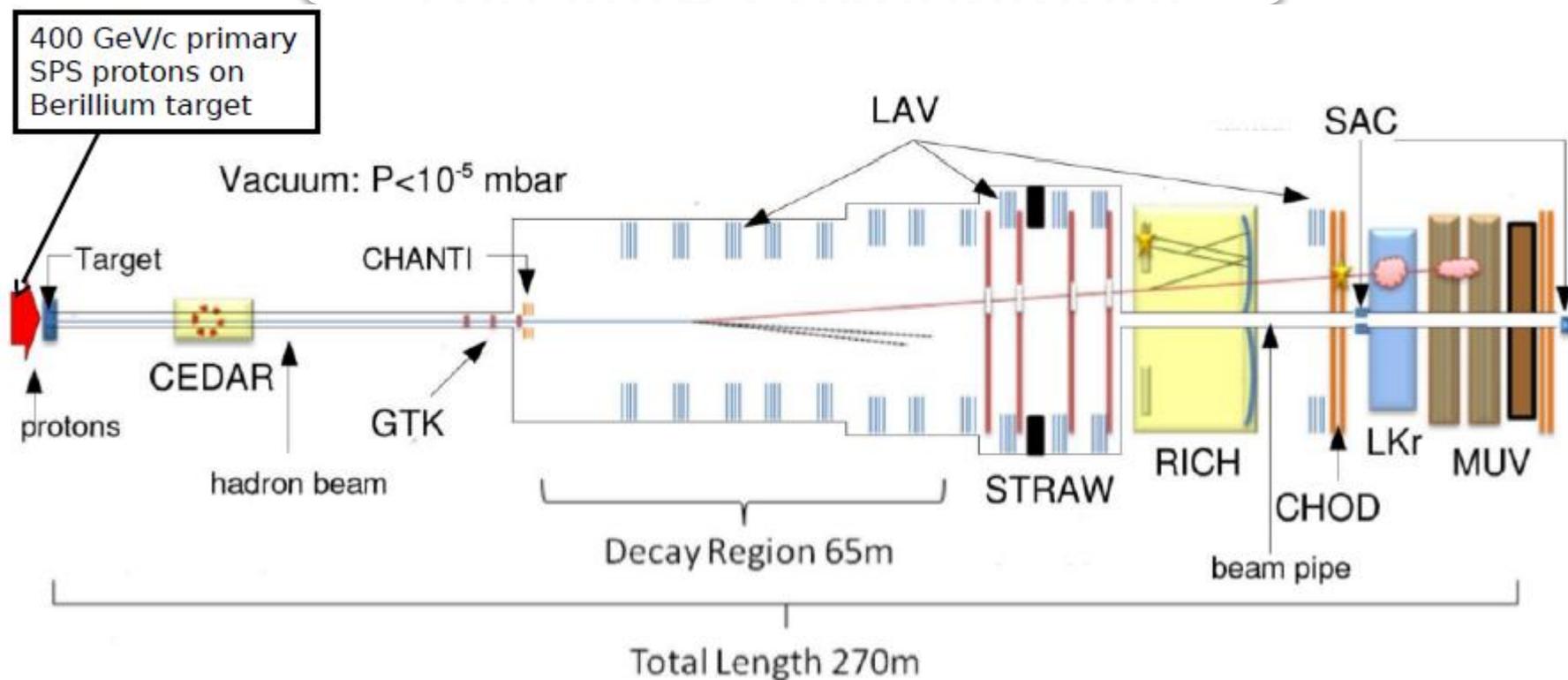
Main backgrounds (BR)

$K^+ \to \mu^+ \nu_\mu$	63.55%
$K^+ \to \pi^+ \pi^0$	20.66%
$K^+ \to \pi^+ \pi^0 \pi^0$	1.76%
$K^+ \to \pi^+ \pi^+ \pi^-$	5.59%
$K^+ \to \pi^0 e^+ \nu_e$	5.07%
$K^+ \to \pi^0 \mu^+ \nu_\mu$	3.35%

Experimental strategy

- 10^{13} K decays (2 years)
- Acceptance ~ 10%
- Background rejection
  - 10^4 from kinematics
 - 10^8 from particle veto and PID

The NA62 experiment

400 GeV/c primary SPS protons on Berillium target

Vacuum: P<10⁻⁵ mbar

LAV   SAC

Target   CHANTI

protons   hadron beam

CEDAR   GTK

RICH   LKr   MUV   STRAW   CHOD   beam pipe

Decay Region 65m

Total Length 270m

- Secondary charged beam (75±1%) GeV/c
- Rate at beam tracker 750 MHz
- 6% K$^+$ (94%: π$^+$, proton)
- K decay rates / year: 4.5 x 10^{12} (65m decay region)

- Expected rate on downstream detectors 10MHz
- Up to 3MHz (MUV3) and 5MHz (CEDAR) per single channel
- 750MHz on GTK stations
- O(100ps) time resolution needed to avoid mismatching between π and beam particle

The NA62 TDAQ system
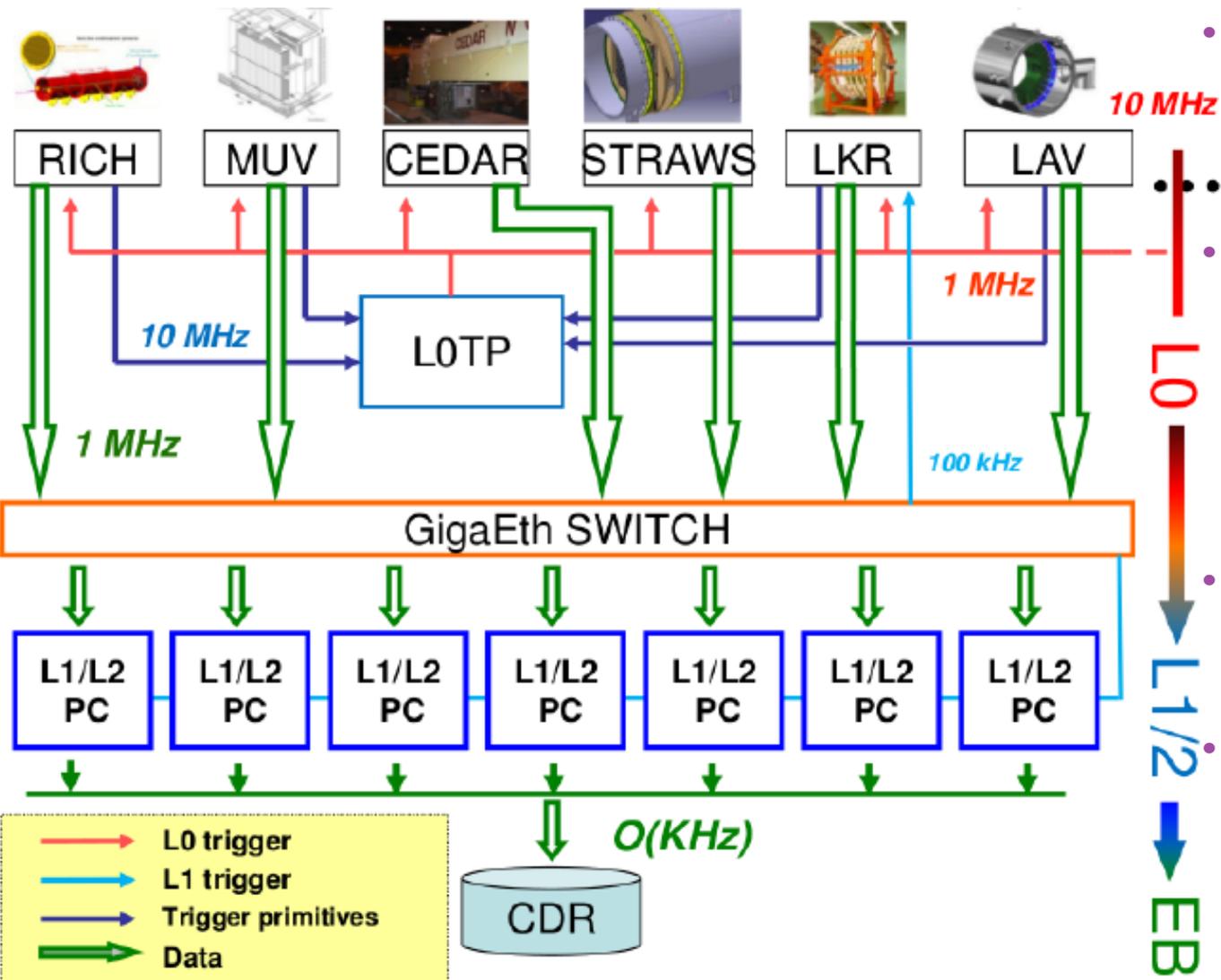
- 12 subdetectors, ~80000 channels, 25 GB/s raw data

- **L0: hardware level synchronous**, based on trigger primitives from fast subdetectors
  10MHz → 1MHz
  1ms latency

- **L1: software level** on single detector data
  1MHz → 100kHz

- **L2: software level** with complete information
  100kHz → 10kHz
  L1/L2 latency: spill

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The NA62 TDAQ system

- The high rate of kaons and the search for a rare decay require very high performances in terms of minimum dead time and random veto and maximum efficiency in data collection with no zero suppression.
- Fast detectors in L0 for timing reference needed (clock asynchronous with events).

- The TDAQ system is based on the TEL62 common board: completely digital data stream from FE to TDAQ.
- Detectors involved in L0 (except LKr) have both data acquisition and trigger primitives generation inside the common board.
- The L0TP receives primitives from detectors, merges the information and takes a decision, sends back a L0 request through TTC system to TEL62s to collect data on PC farm.
- L1 and L2 implemented inside the same PCs to avoid useless data transfer.

The NA62 TDAQ system

- Example of L0 trigger primitives generation on TEL62 boards:
  - 1 track on CHOD: time and space coincidence between correspondent quadrant of the two planes
  - Multiplicity cut on RICH: histograms in 3ns bins
  - LAV: a signal over a certain threshold from one of the 12 stations
  - LKr: clusters identified by an array of ~40 TEL62s evaluating ADC sampling of 4x4 super cells (*see poster by N. De Simone*)
  - MUV3: signal from one channel
- Example of trigger for main decay and background rate reduction (kHz)

Component	Initial	CHOD	RICH	x !MUV3	x !LKr
$K^+ \to \pi^+\pi^0$	2114	744	591	545	150
$K^+ \to \mu^+\nu_\mu$	6504	4052	3634	25	24
$K^+ \to \pi^+\pi^+\pi^-$	572	36	13	11	7
$K^+ \to \pi^+\pi^0\pi^0$	180	43	33	30	2
$K^+ \to \pi^0 e^+\nu_e$	519	173	131	131	34
$K^+ \to \pi^0\mu^+\nu_\mu$	343	140	113	7	4
π^+	526562	538	219	33	21
$\pi^+ \to \mu^+$	99144	2418	2352	33	33
$K^+ \to \mu^+$	11792	837	822	5	5
$\pi^- \to \mu^-$	21375	178	155	0	0
$K^- \to \mu^-$	3035	11	5	0	0
Total rate		9169	8067	819	280

Main decays (rows $K^+ \to \pi^+\pi^0$ through $K^+ \to \pi^0\mu^+\nu_\mu$)

Beam halo (rows π^+ through $K^- \to \mu^-$)
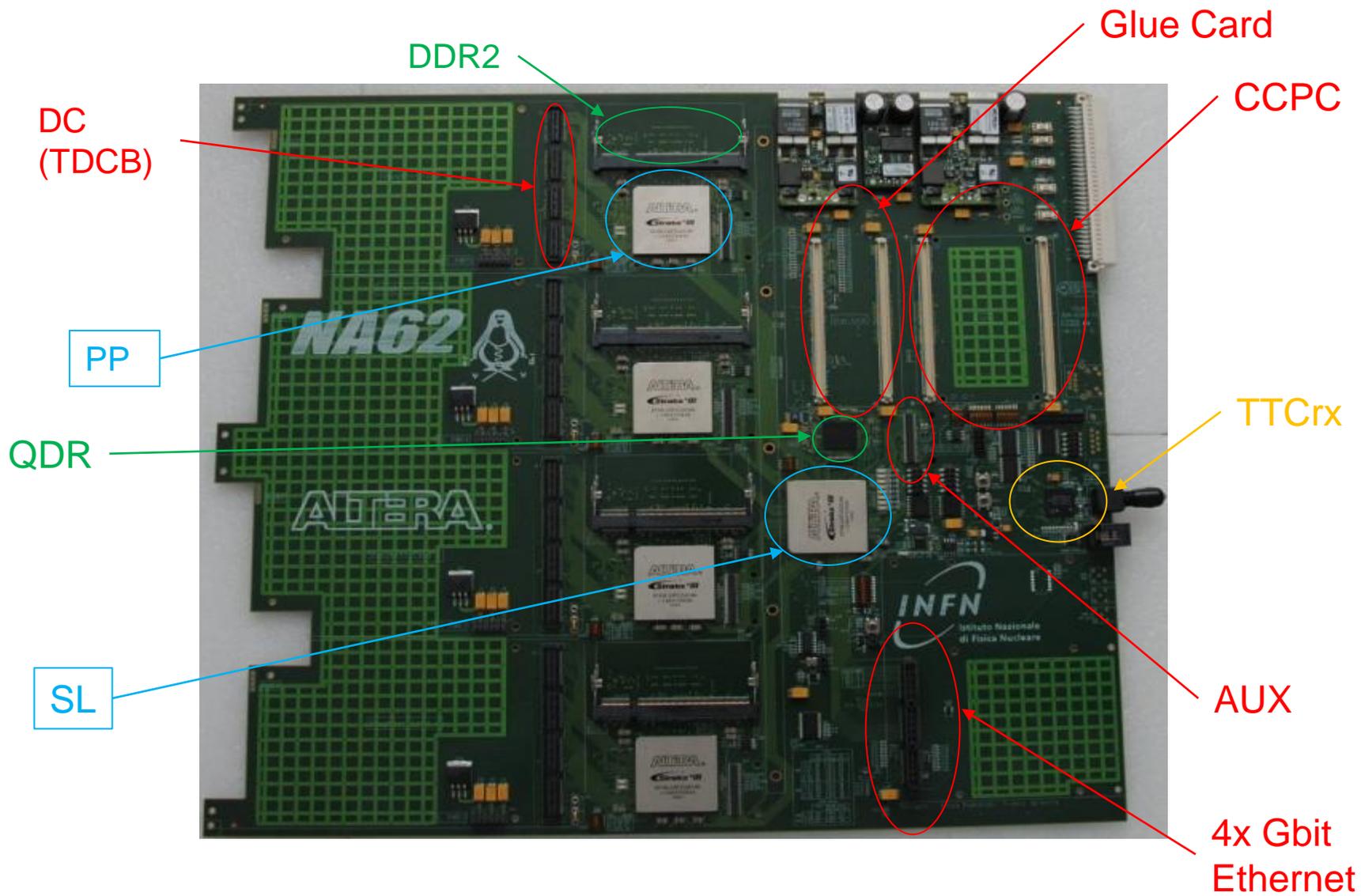
TEL62

Trigger ELectronics for NA62

the common FPGA based motherboard for trigger generation and data acquisition
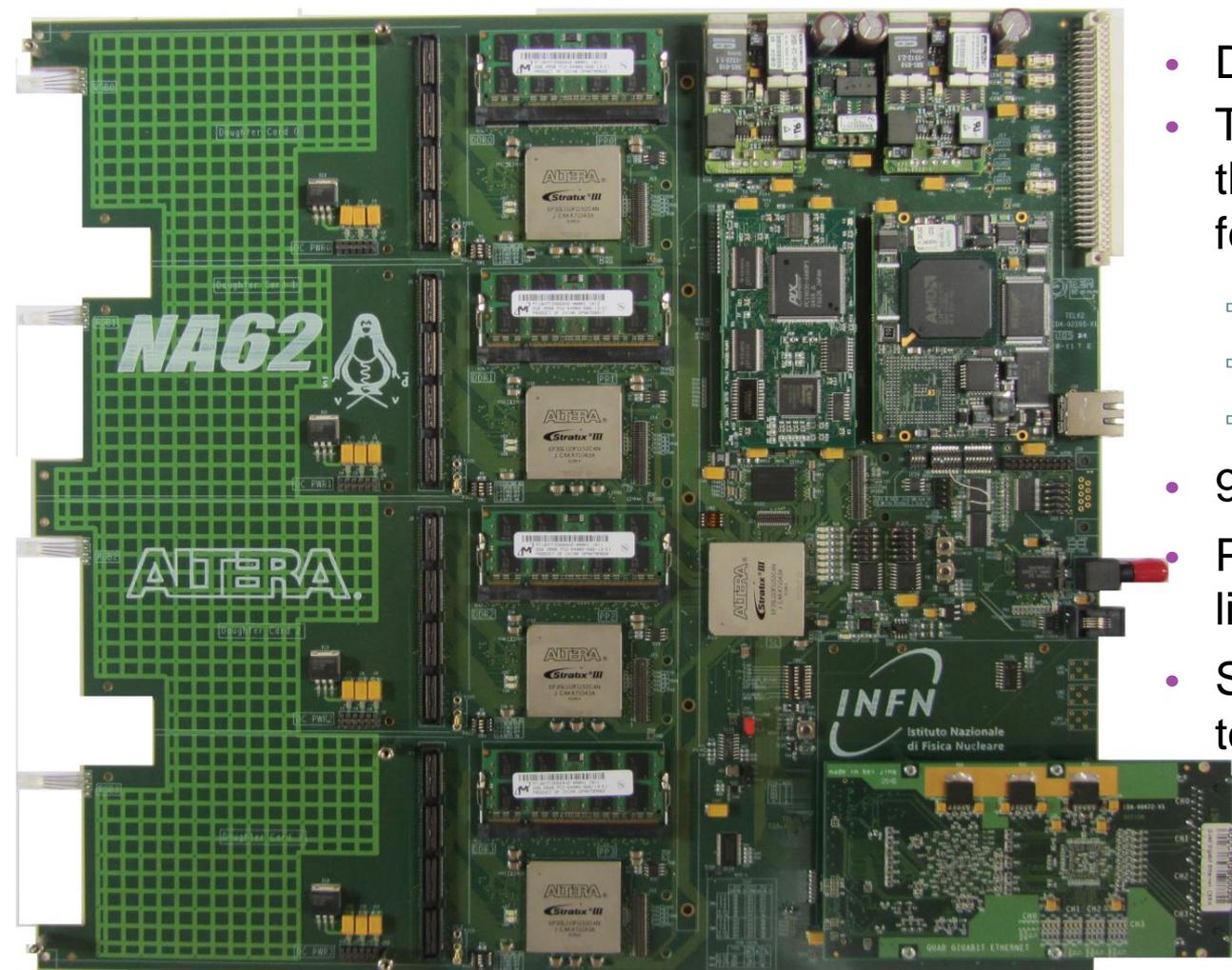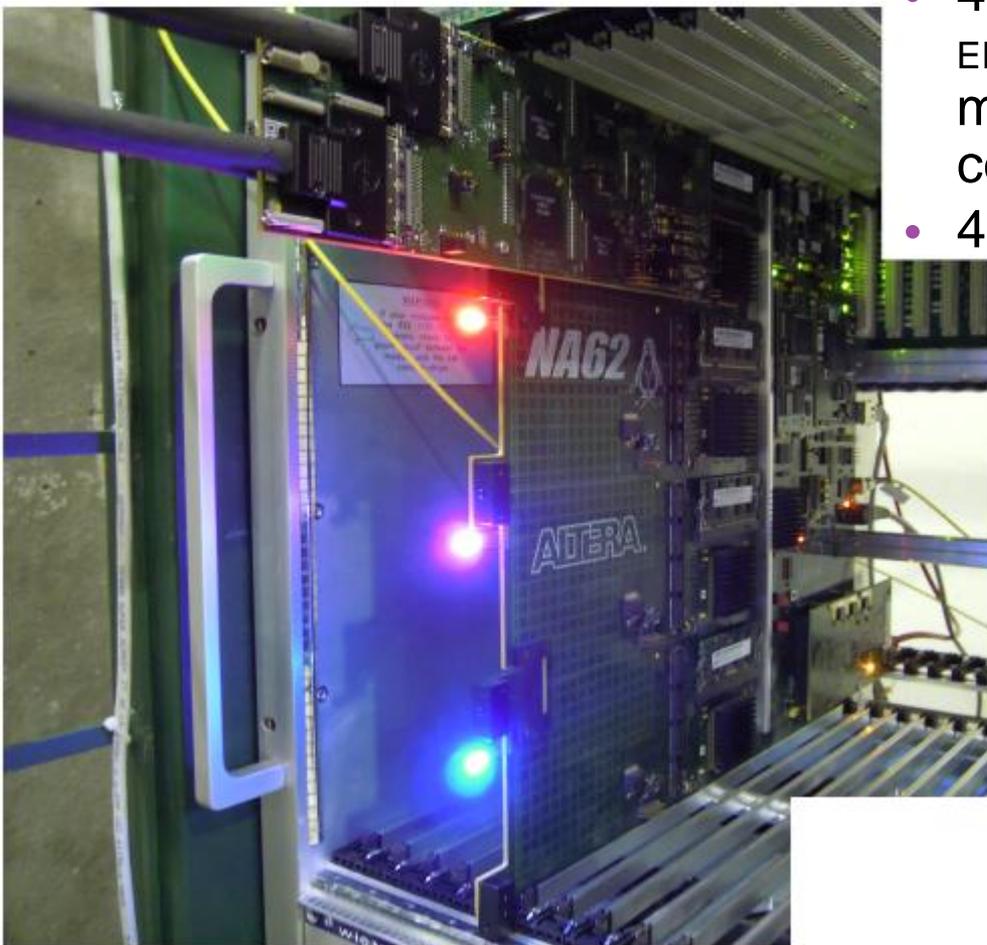

- Developed at INFN Pisa
- TEL62 is a major upgrade of the TELL1 designed by EPFL for LHCb experiment
  - 8x computational power
  - 20x buffer memory
  - Connectivity
- 9U Eurocard standard
- Printed circuit of 16 layers, all lines controlled in impedance
- Special routing of clock tree to avoid signal jitter

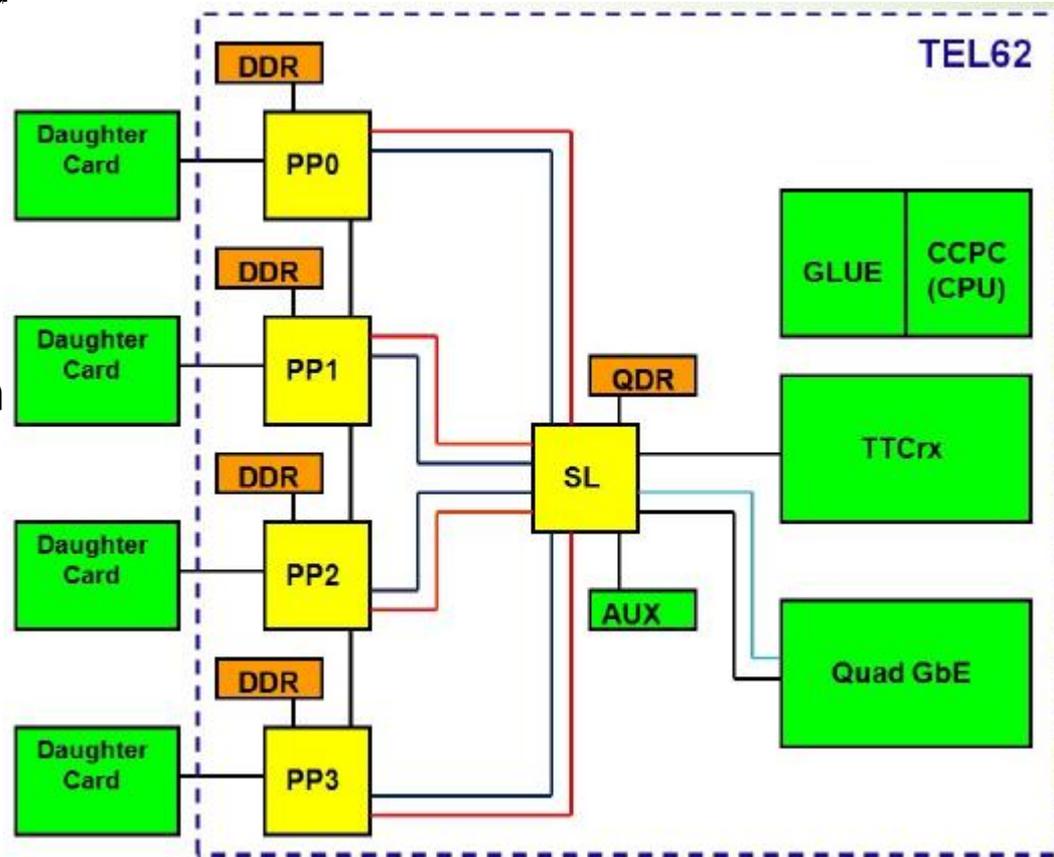Total production O(100) boards

TEL62

TEL62

- 4 PP-FPGAs (Altera StratixIII EP3SL200F1152) connected to 4 mezzanines through a 200-pin connector
- 4 DDR2 memory buffers (2GB)

  - One central SL-FPGA (same Altera StratixIII) connected to PPs through two independent 32-bit data buses at 160MHz (5Gb/s per PP)

  - 1 QDR RAM as intermediate buffer
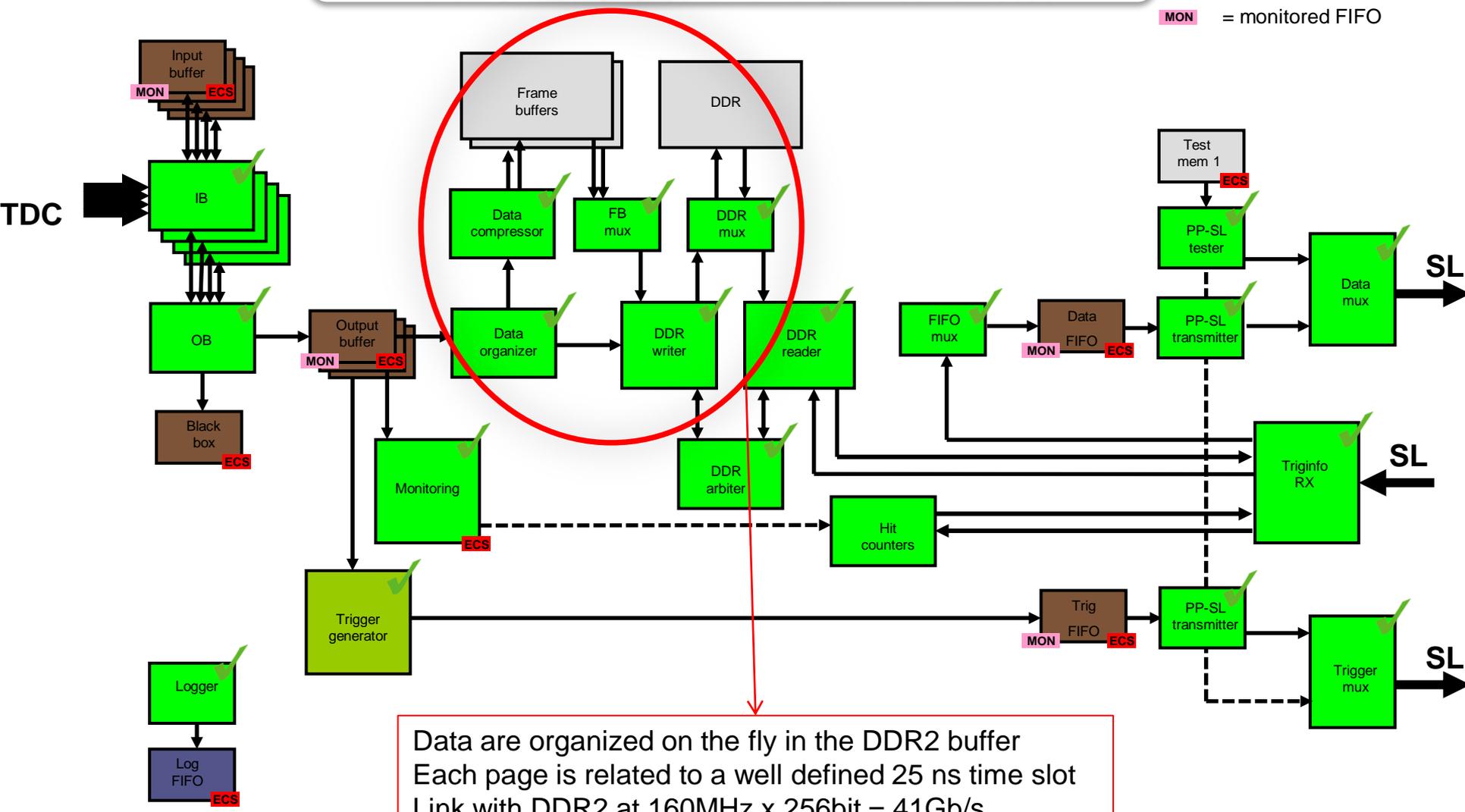 - Custom Quad-GBE mezzanine as output board (4x 1Gbit Ethernet channels)

TEL62

- GLUE card and CCPC mezzanines for slow control and configuration
  Connected through PCI bus
- 3 different communication protocols:
  - JTAG, I2C, ECS
- Clock and L0 trigger information received from an optical TTC link. TTCrx chip on board to decode them
- 2 EPCS64s store the configuration of FPGAs
- AUX connector for TEL62 boards interconnection
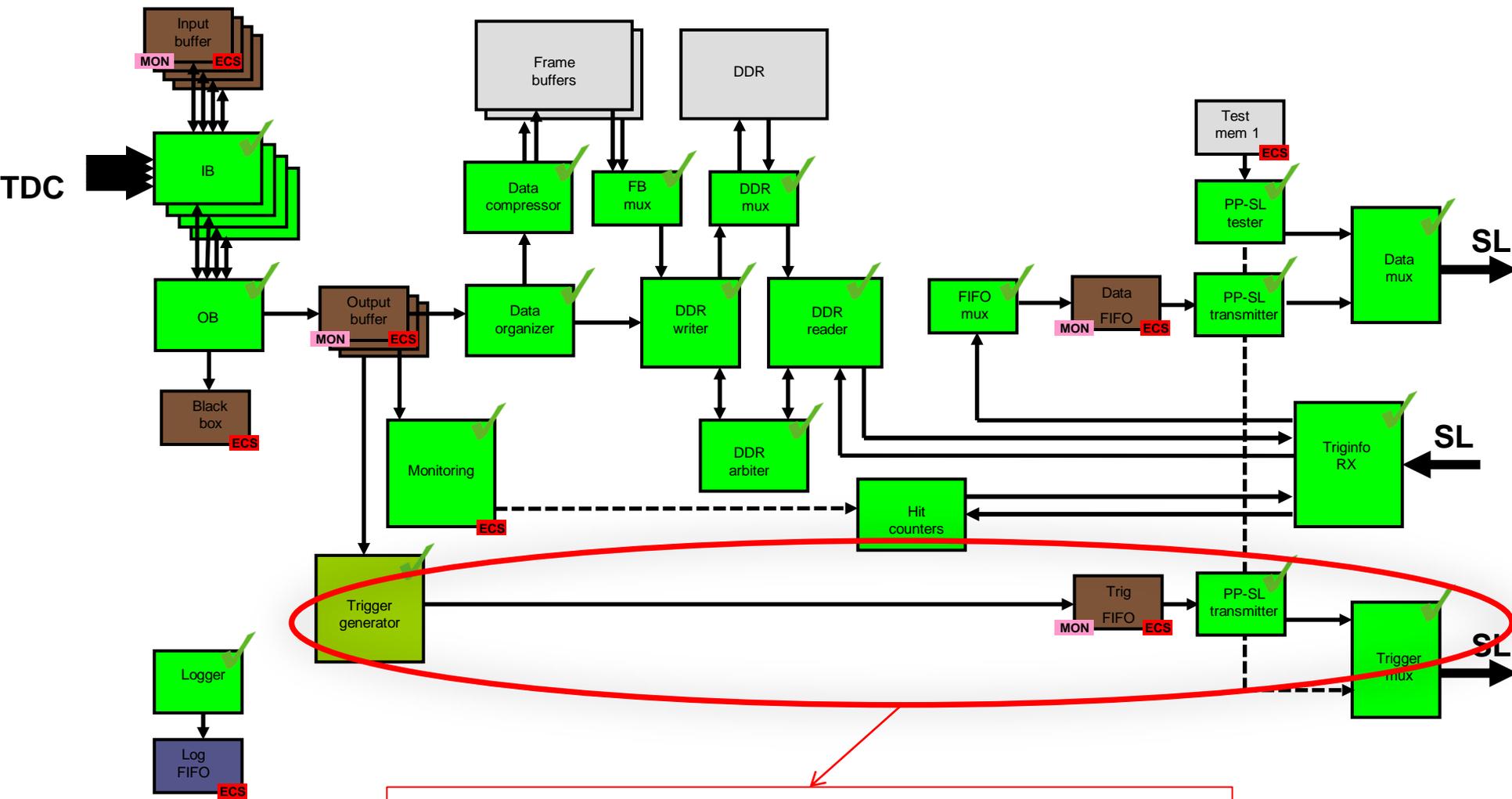 (2 independent 16bit buses)

TEL62 PP-FPGA FW

ECS = accessible from CCPC

MON = monitored FIFO

Data coming from 4 TDCs are collected and merged

TEL62 PP-FPGA FW

ECS = accessible from CCPC

MON = monitored FIFO

TDC

Input buffer
MON ECS

IB

OB

Black box
ECS

Output buffer
MON ECS

Frame buffers

DDR

Data compressor

FB mux

DDR mux

Data organizer

DDR writer

DDR reader

DDR arbiter

Monitoring
ECS

Hit counters

Test mem 1
ECS

PP-SL tester

PP-SL transmitter

FIFO mux

Data FIFO
MON ECS

Data mux

SL

Triginfo RX

SL

Trigger generator

Trig FIFO
MON ECS

PP-SL transmitter

Trigger mux

SL

Logger

Log FIFO
ECS

Data mux

Data are organized on the fly in the DDR2 buffer
Each page is related to a well defined 25 ns time slot
Link with DDR2 at 160MHz x 256bit = 41Gb/s
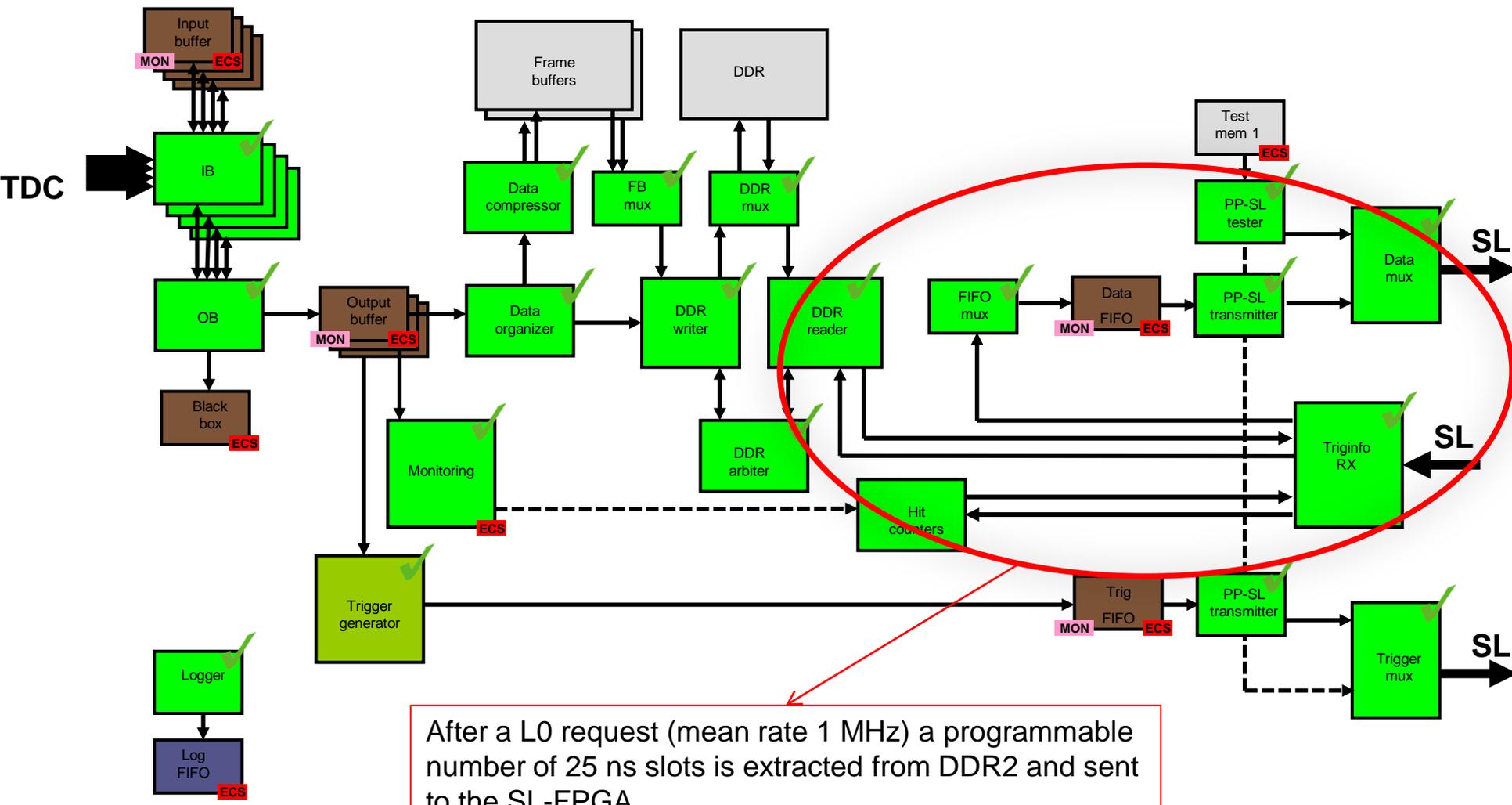
TEL62 PP-FPGA FW

ECS = accessible from CCPC

MON = monitored FIFO

A copy of the data flow is used for trigger primitives generation

TEL62 PP-FPGA FW

ECS = accessible from CCPC

MON = monitored FIFO

After a L0 request (mean rate 1 MHz) a programmable number of 25 ns slots is extracted from DDR2 and sent to the SL-FPGA

TEL62 SL-FPGA FW

ECS = accessible from CCPC

MON = monitored FIFO

△ Choke generator

TTC interface decodes trigger information and sends it to PP-FPGAs
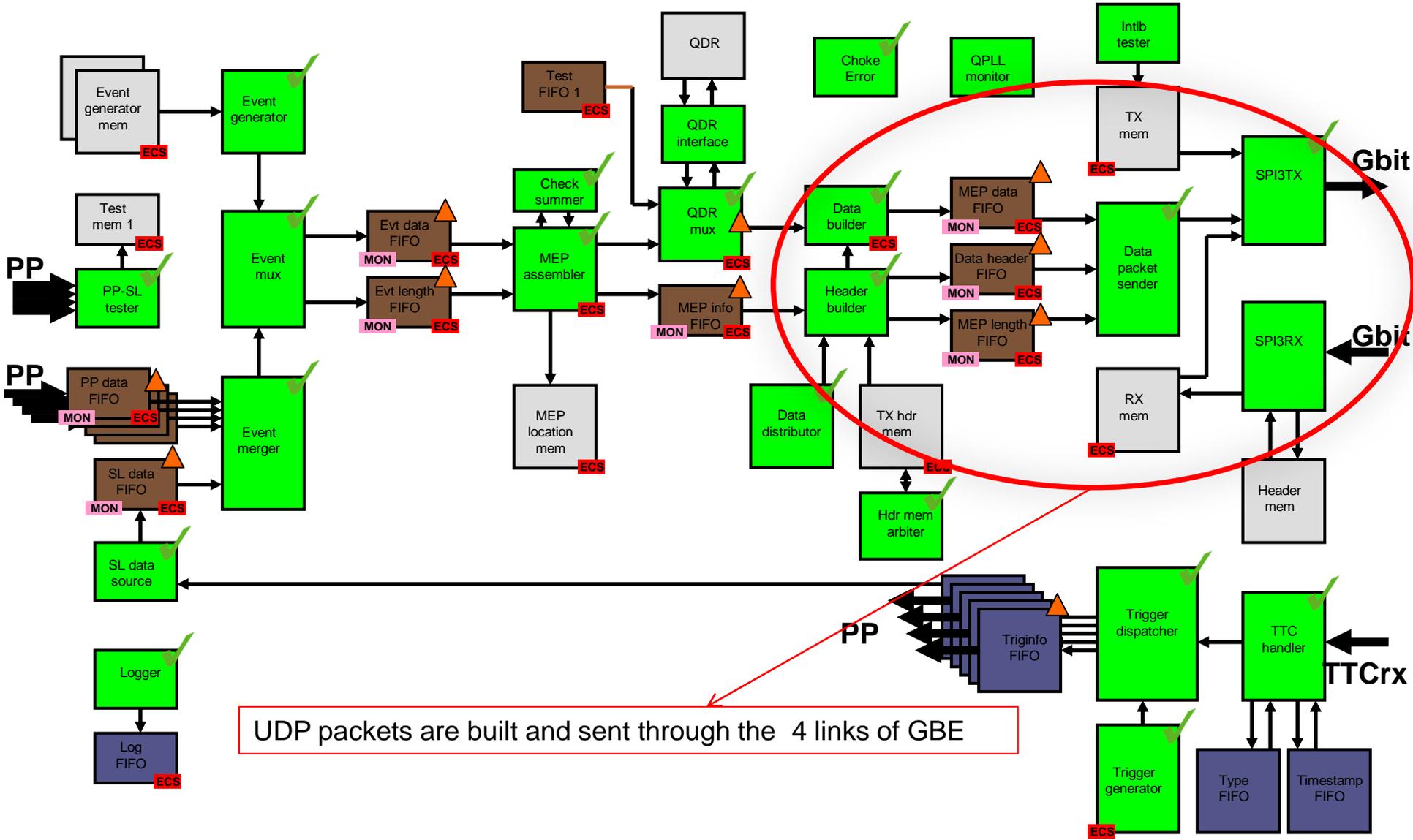
TEL62 SL-FPGA FW

ECS = accessible from CCPC

MON = monitored FIFO
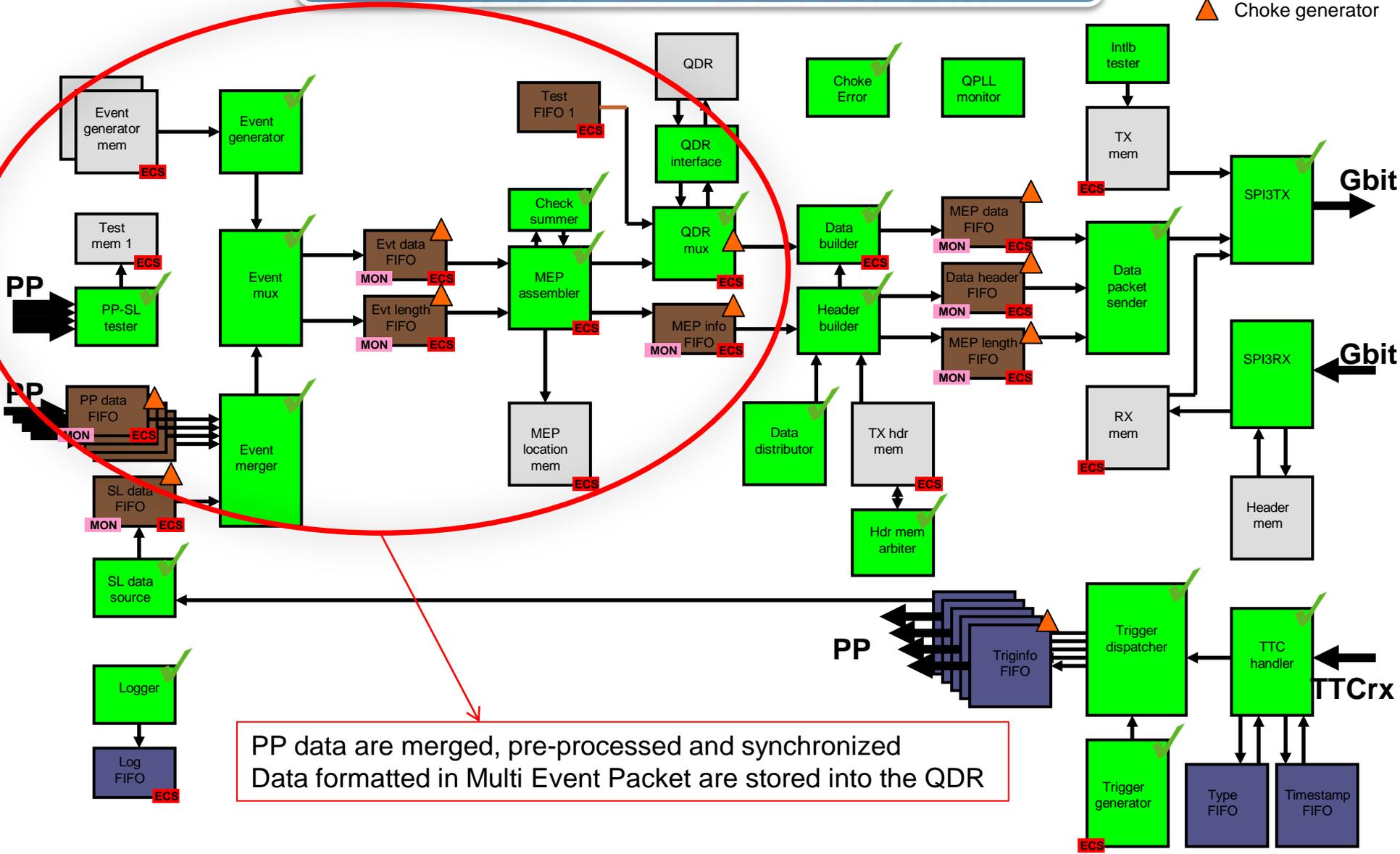
△ Choke generator

PP data are merged, pre-processed and synchronized
Data formatted in Multi Event Packet are stored into the QDR

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TEL62 SL-FPGA FW

UDP packets are built and sent through the 4 links of GBE

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TDCB

TDC Board

Custom TEL62 mezzanine developed in Pisa
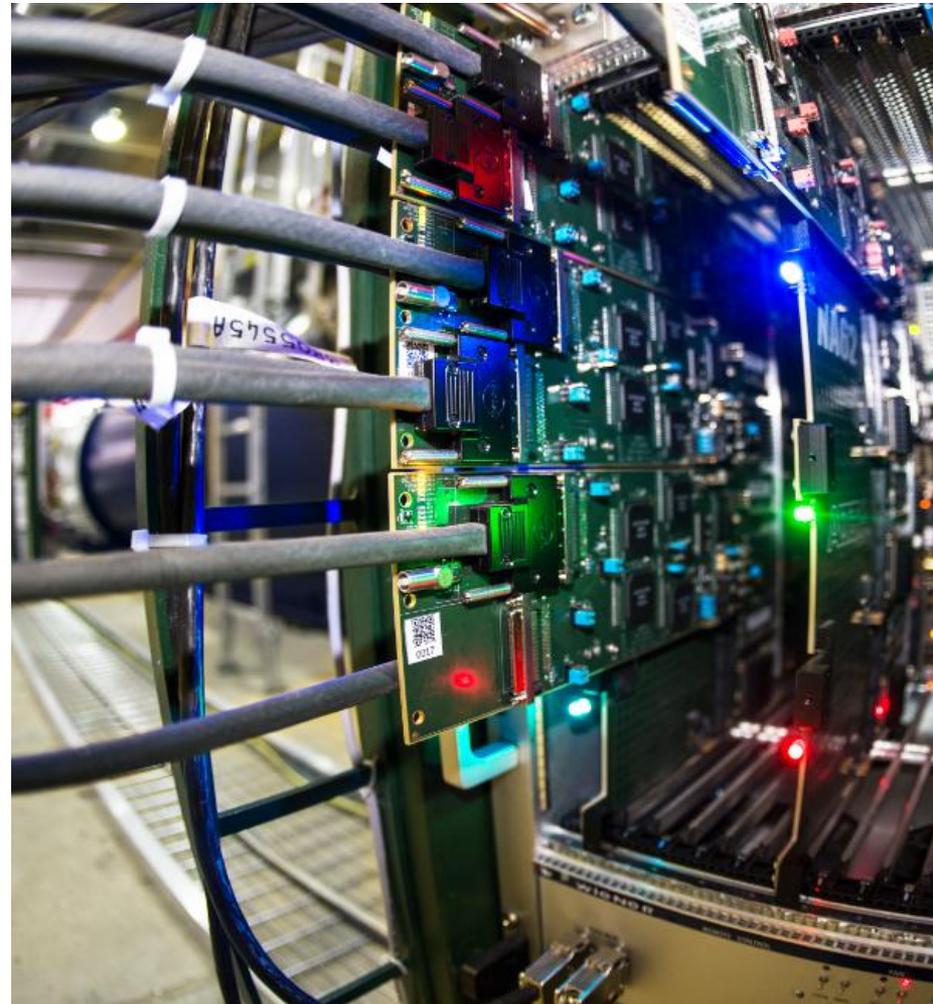

- 10 layers PCB
- 4 High Performance Time to Digital Converter (HPTDC) developed at CERN
  - 4x32 LVDS input channels (16x32=512 per TEL62)
  - 19bit leading and trailing time measurements with 100ps LSB
- VHDCI 68-pin connectors for standard 34-pair SCSI cables

- 1 TDCC-FPGA (Altera CycloneIII EP3C120F780)
- EPCS64
- 2x1MB SRAM
- QPLL (clock jitter < 40 ps)
- JTAG and I2C protocols for communication

TDCB TDCC-FPGA FW

TDCC-FPGA firmware functionalities

- TDC interface: implementation of TDC communication protocol
- Data from TDC read periodically and then buffered
- Data processing: packets with timestamp and counter enter data stream to the TEL62

- JTAG master for TDC configuration
- I2C manager

- TDC data emulator for testing and debugging purposes
- Calibration of FE board through the spare pair of connectors
- Controller of SRAM memories

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TDCB

- Used by most of the subdetectors
  - CEDAR, CHANTI, LAV, RICH, CHOD, MUV
- Resolution of subdetectors not affected
- Rates
  - 4x32bit data buses to TEL62 at 40MHz (1.2 Gb/s per TDC stream)
  - Up to 10MWord/s from HPTDC (single channel)
  - Trigger matching mode: 4 buffers of 256 word (1 per 8 channel group) read every 6.4 µs (40MWord/s per 8 channel group)
- Issues only with CEDAR
  - Possibility to use just 4 channels per TDC (1 each 8 channel group) to cope with the expected highest channel rate (~ 5MHz)

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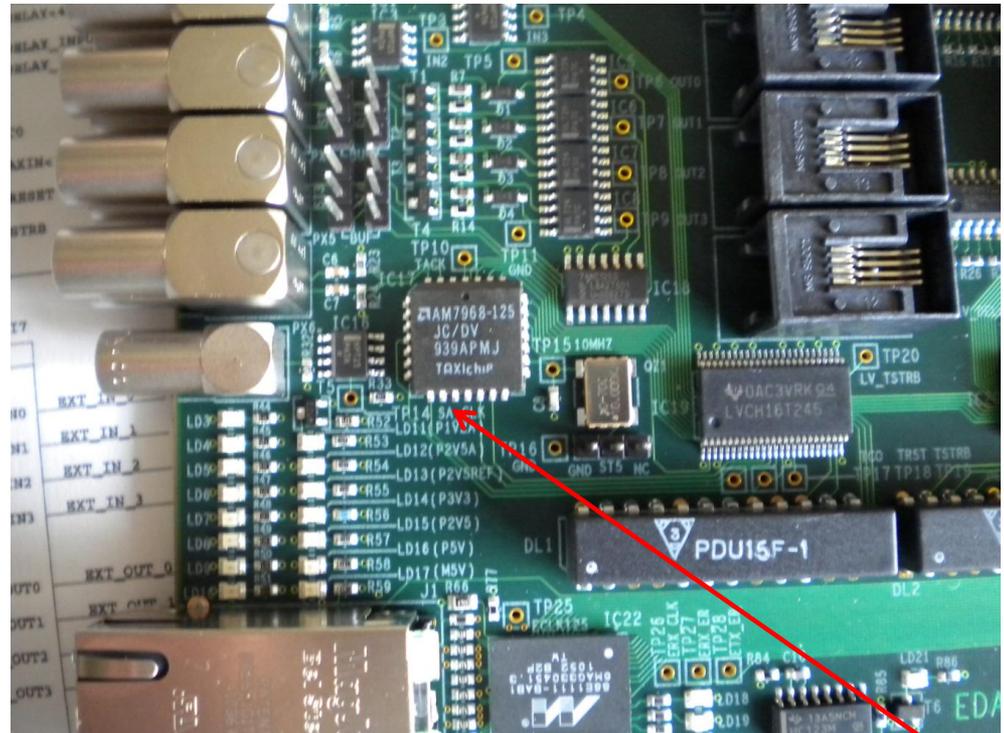
TALK

Trigger Adapter for Liquid Krypton calorimeter

A multipurpose daughter board for the TEL62 developed at CERN
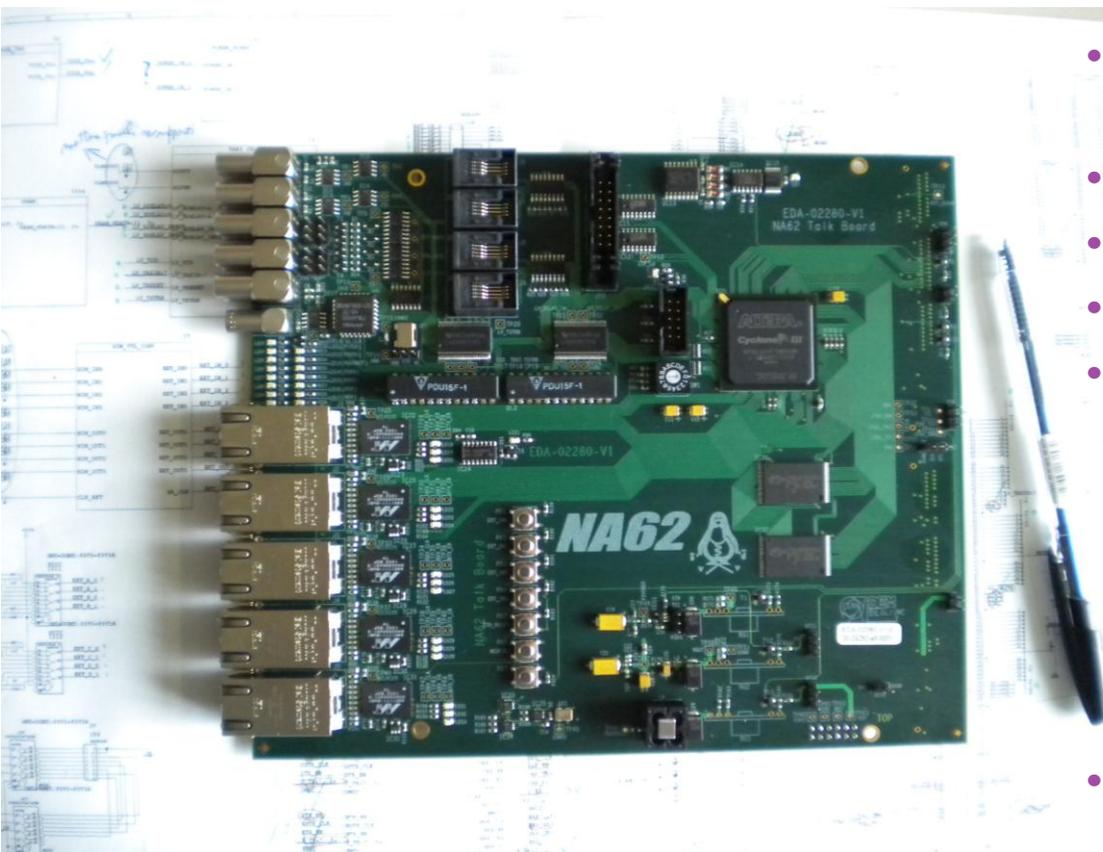
- PCB 10 layers
- Impedance controlled lines for clocks
- 1 FPGA CycloneIII (same as TDCB)
- 1 Taxi Chip
- 5x32bit buses to the TEL62
- I/O connectors on one side and internal surface
  - 5 Ethernet connectors driven by Marvell 88e1111 chip
  - 5 lemos for input/output
  - 4 RJ11 connectors
  - 1 connector for the LTU
- Control access through TEL62, or dedicated JTAG, I2C, Ethernet
- 6U VME frame for standalone use

TALK

- TALK main purpose: interface between old LKr readout and TTC system for NA62 TR in 2012.

- In 2012 runs and before the deployment of the CREAM modules (*see poster by S. Venditti*) the readout has been done through SLM+CPD system
  - Trigger distribution based on TAXI
  - Timestamp not propagated in CPD

- In NA62 L0 timestamp is not propagated through TTC, but regenerated inside TEL62s

- TALK provides the interface between TTC (through his TEL62 motherboard) and TAXI chip: PECL signals through LEMO


TAXI CHIP

- The FPGA produces the timestamp list to be merged in the readout PC (sent via Ethernet)

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TALK

Other functionalities

- During TR 2012 has been used as proto L0TP
  - Primitives collection through Ethernet
  - Old style NIM triggering through LEMO
  - Trigger decision to the LTU using dedicated connector
  - RJ-11 connectors to receive choke/error LVDS lines from detectors

- LKr calibration logic
  - TALK operated standalone on VME support
  - Logic implemented inside the FPGA instead of the old NIM and CAMAC modules
  - Ethernet commands will program calibration in/out burst, rates, pulses synchronous on not with NA62 clock

LTU

RJ-11
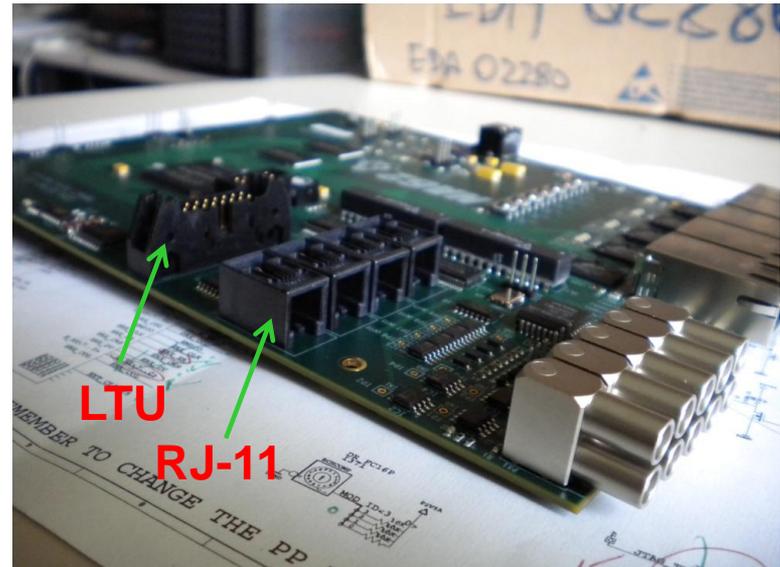
- Test bench for CREAM modules
  - L0 trigger through LEMO or through TTC system via LTU and fiber
  - L1 through Ethernet for same events

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Conclusions

- A general purpose FPGA based motherboard (TEL62) has been developed as integrated trigger and data acquisition system for NA62
  - Satisfactory results during 2012 runs with the first firmware version
  - New faster firmware under test, to be used in 2014 first physics run
- A TDC based daughter-board (TDCB) has been designed for digital time and ToT measurements needed by NA62 requirements
  - Final production of O(100) boards starting
- A multi purpose daughter-board (TALK) has been developed and was essential for 2012 TR data taking
  - In the future will remain for testing purposes and for LKr calibration

We look forward to the 2014 data!