Microfabricated silicon on-detector cooling systems

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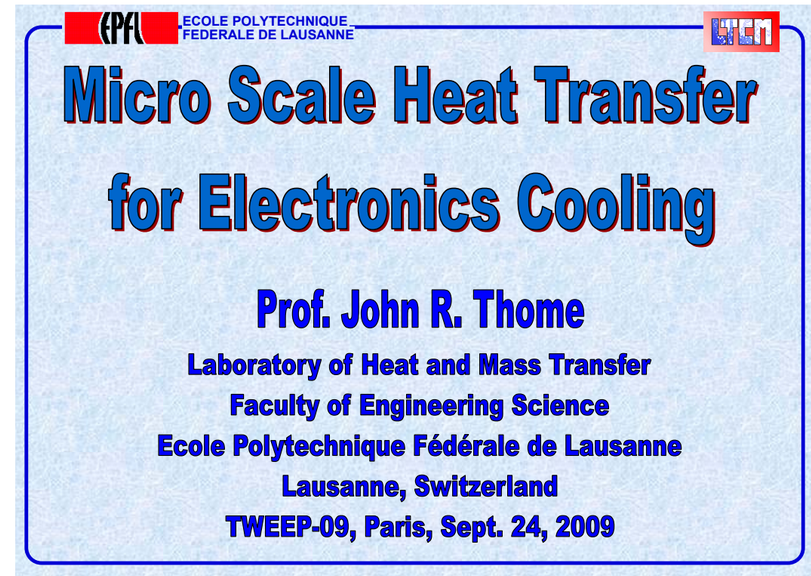
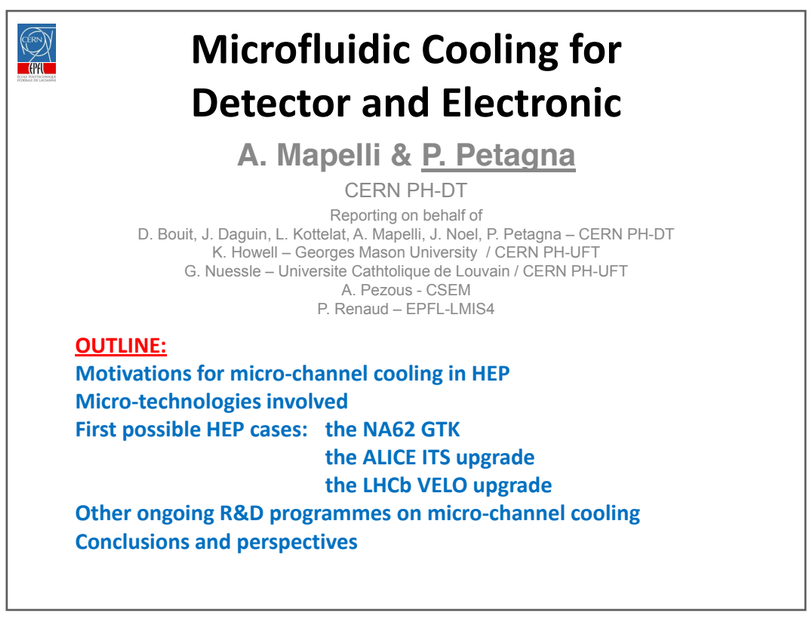
TWEPP 2013
Perugia, Italia

microCool at TWEPP 2011

Two years ago we showed how, based on Prof. Thome's talk at TWEPP 2009, **PH-DT** had started studying and developing on-detector microfluidic cooling systems with a particular focus on the **NA62 GigaTracKer**.





Since then this system has been approved by the NA62 experiment. It has also been recently selected by for the upgrade of the **LHCb VeLo** and it is under consideration as an alternative for **ALICE ITS** upgrade.

In this talk we will review the current status of these three developments with a focus on microfabrication, integration and fluidic connectivity.

Motivation

Issues to be addressed when designing on-detector cooling systems

1. Minimization of material budget
2. Efficient thermal management
3. Minimization of ΔT between heat source and heat sink

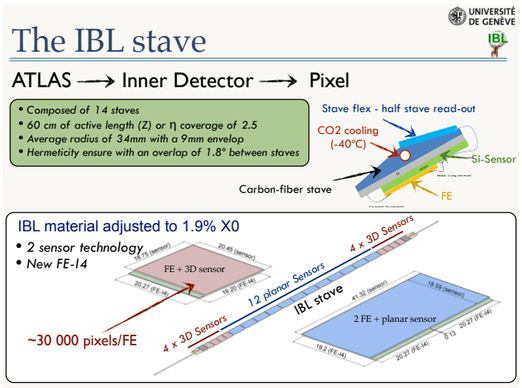
Integration of cooling and detector lay-out

The cooling has to be considered as an integral part of the detector and the experiment, therefore physicists and engineers shall collaborate from the beginning of the conceptual design of the systems, with an overall view on all subparts.

Engineering Cooling Forum
30 October 2008, CERN

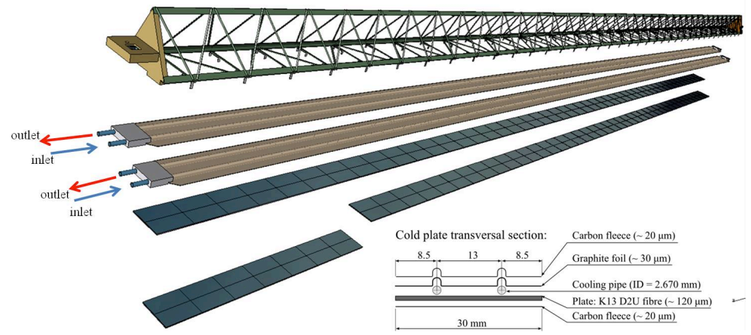
Integrating Cooling in Support Structures..
..or somewhere in the Silicon?

ATLAS IBL

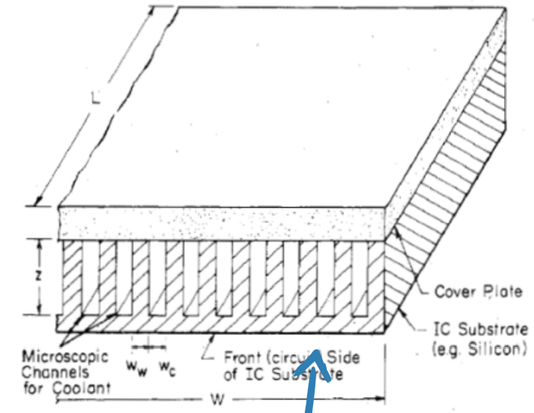


from J. Bilbao http://indico.cern.ch/sessionDisplay.py?sessionId=6&confId=208719#20130125

ALICE ITS Upgrade



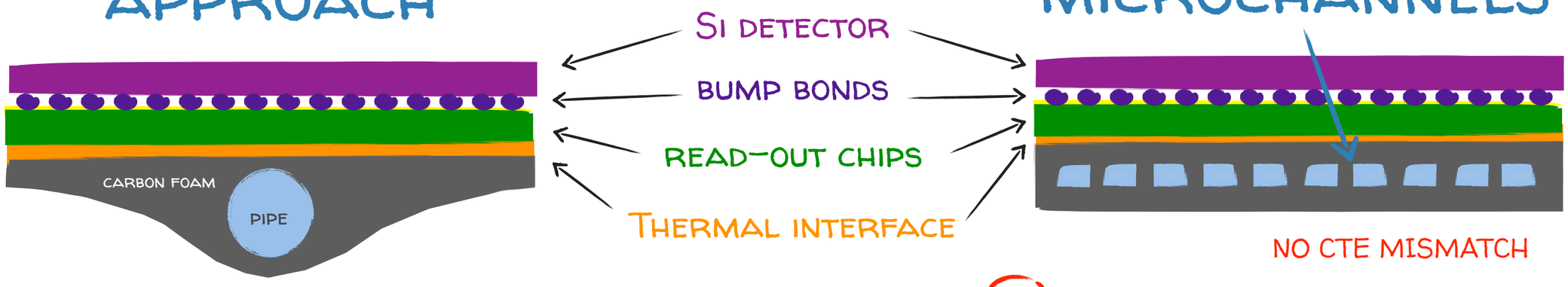
ALICE ITS Upgrade Outer Barrel Stave

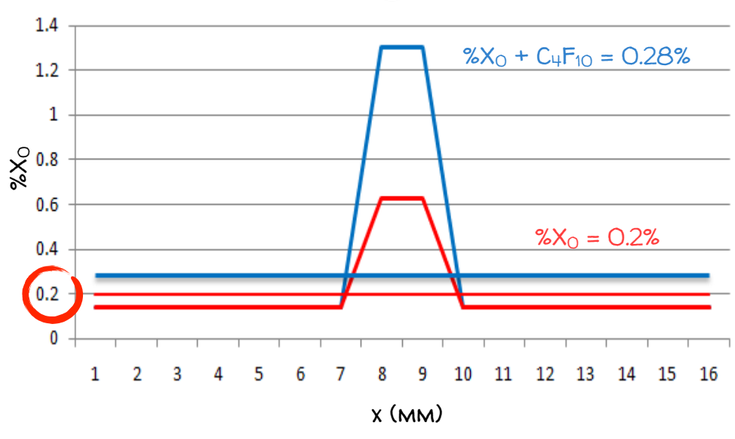


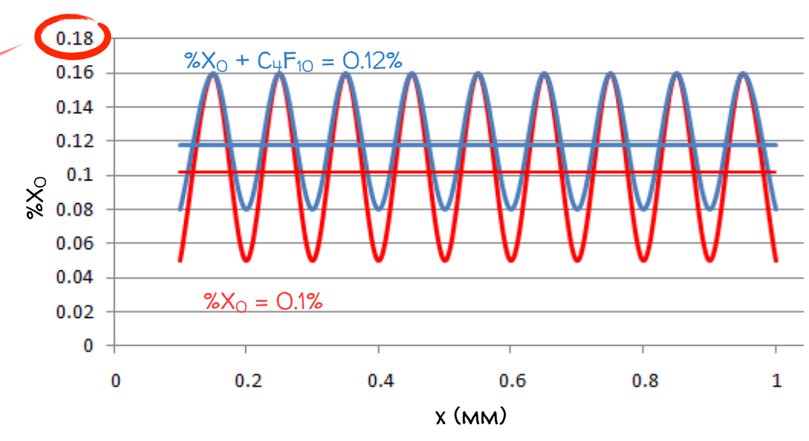
D.B. Tuckerman and R.F.W. Pease, IEEE Elec. Dev. Letters, Vol. 2, 5, 1981

IN-MECHANICS APPROACH

SILICON COOLING MICROCHANNELS







X_0 calculations by Claudio Bortolin

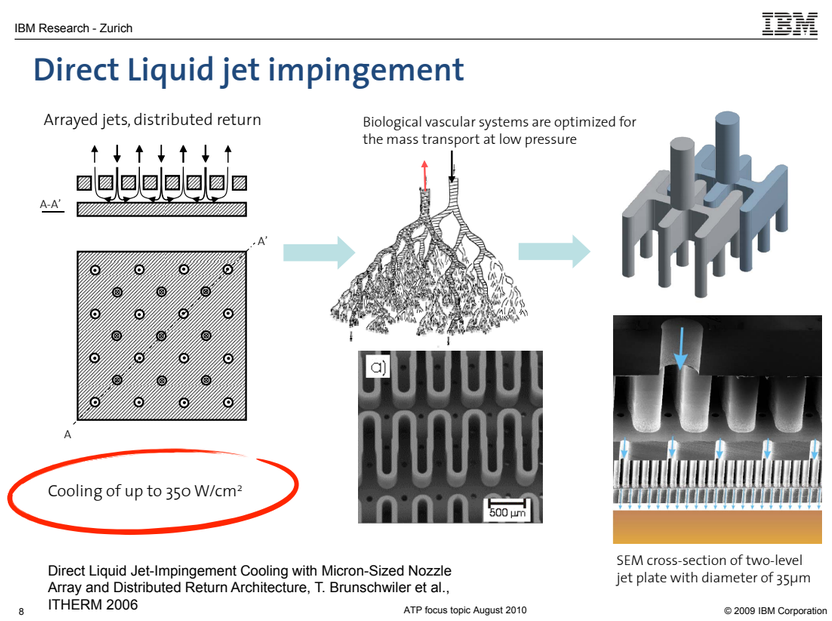
10°C

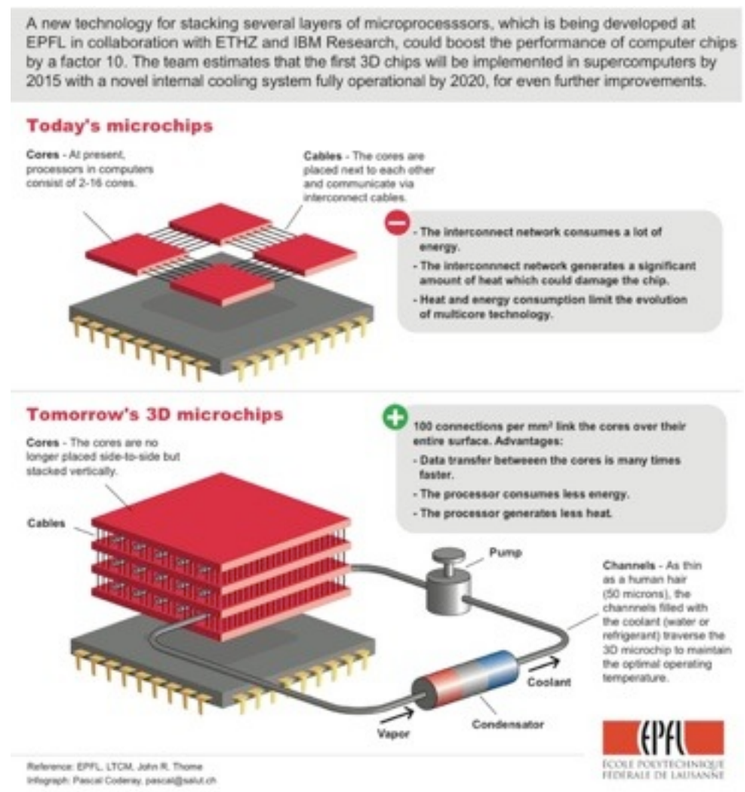
ΔT between heat source and heat sink for power dissipations of ~1W/cm² (currently installed systems ~15°C)

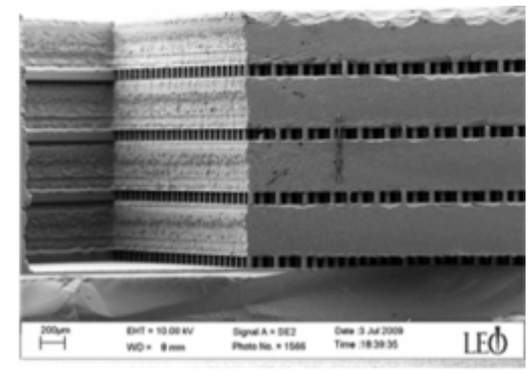
5°C

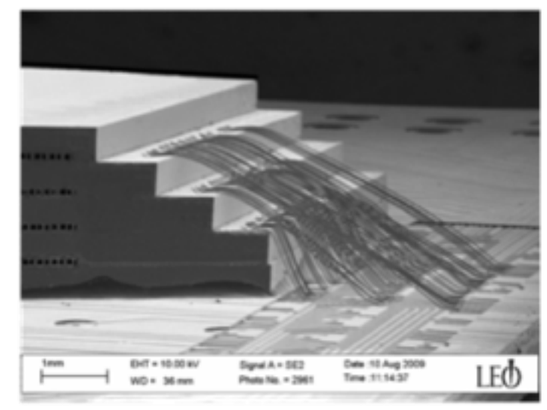
Silicon Microfluidic Cooling

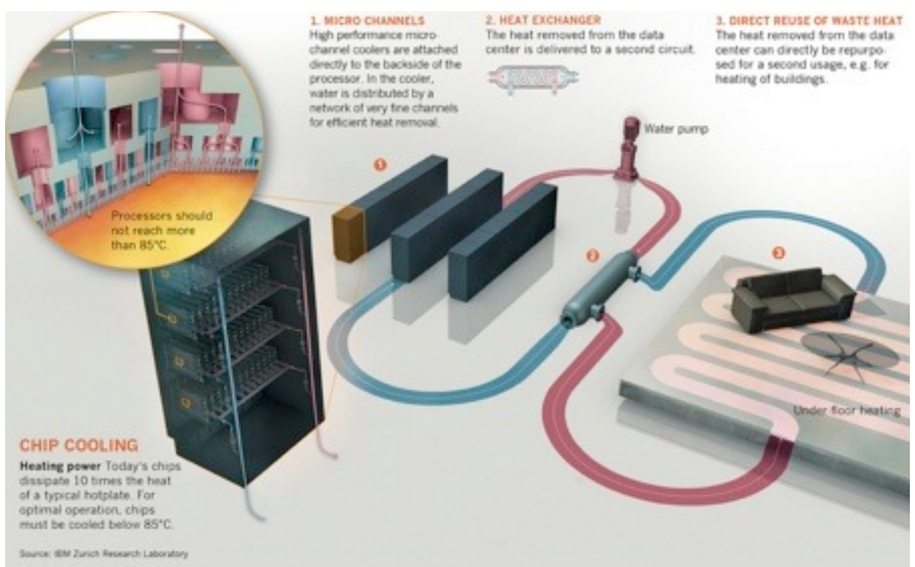
out of the HEP world

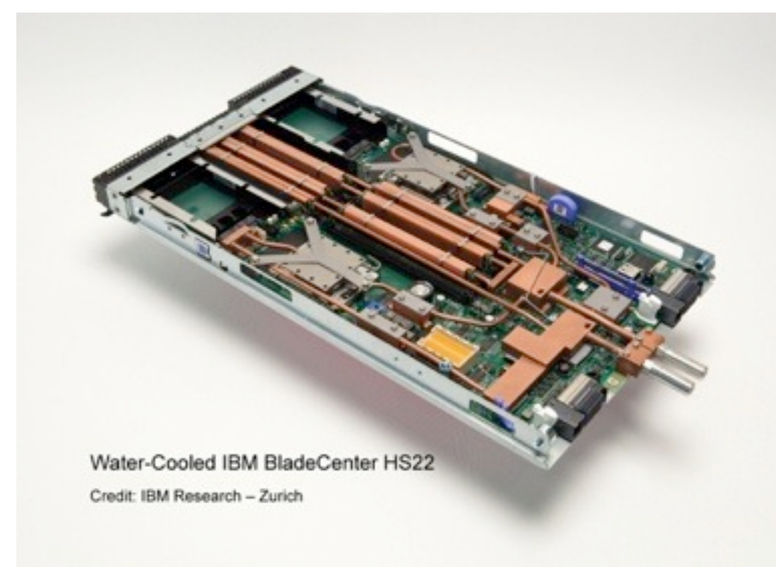












CERN PH-DT Microfabrication @EPFL

http://cmi.epfl.ch/

class 100 MEMS cleanroom

4" wafers

(6"wafers)

operation on 50 machines

Photolithography

Etching

Thin Films

Bonding

Thinning

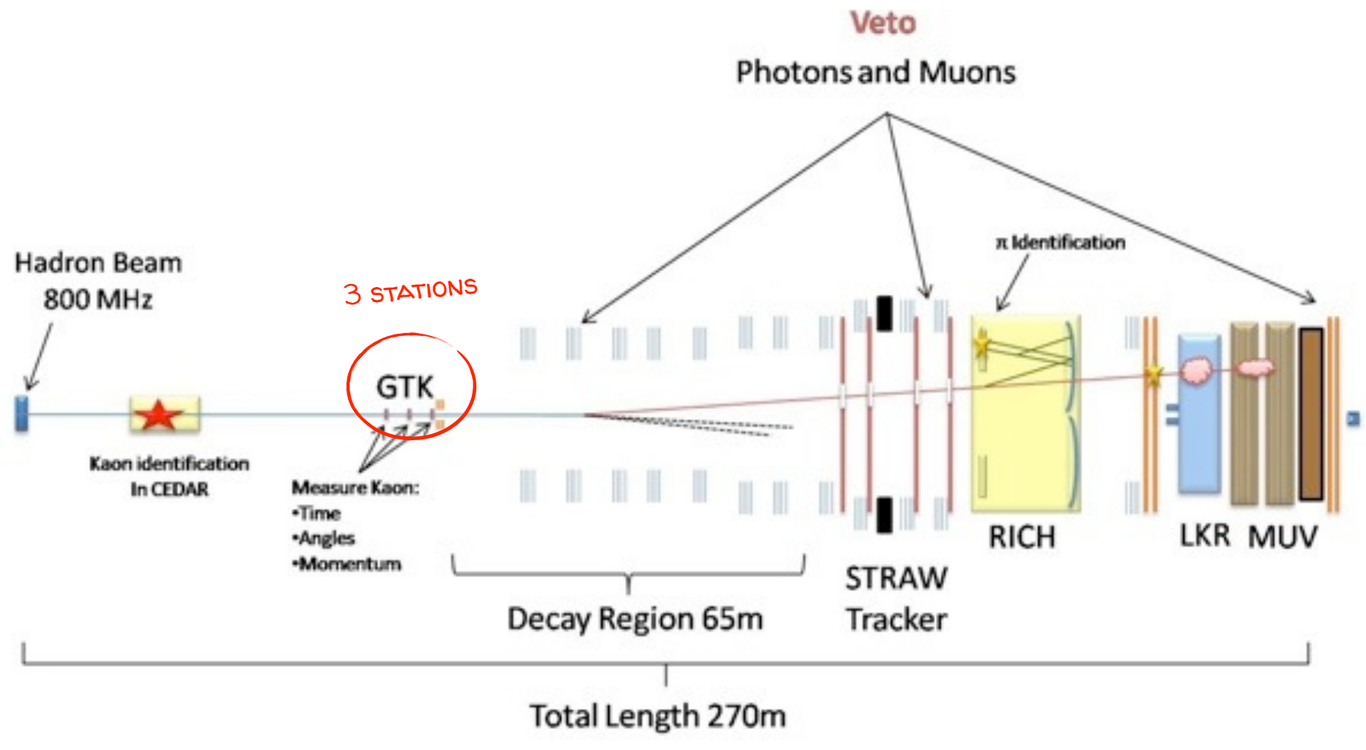
Metrology

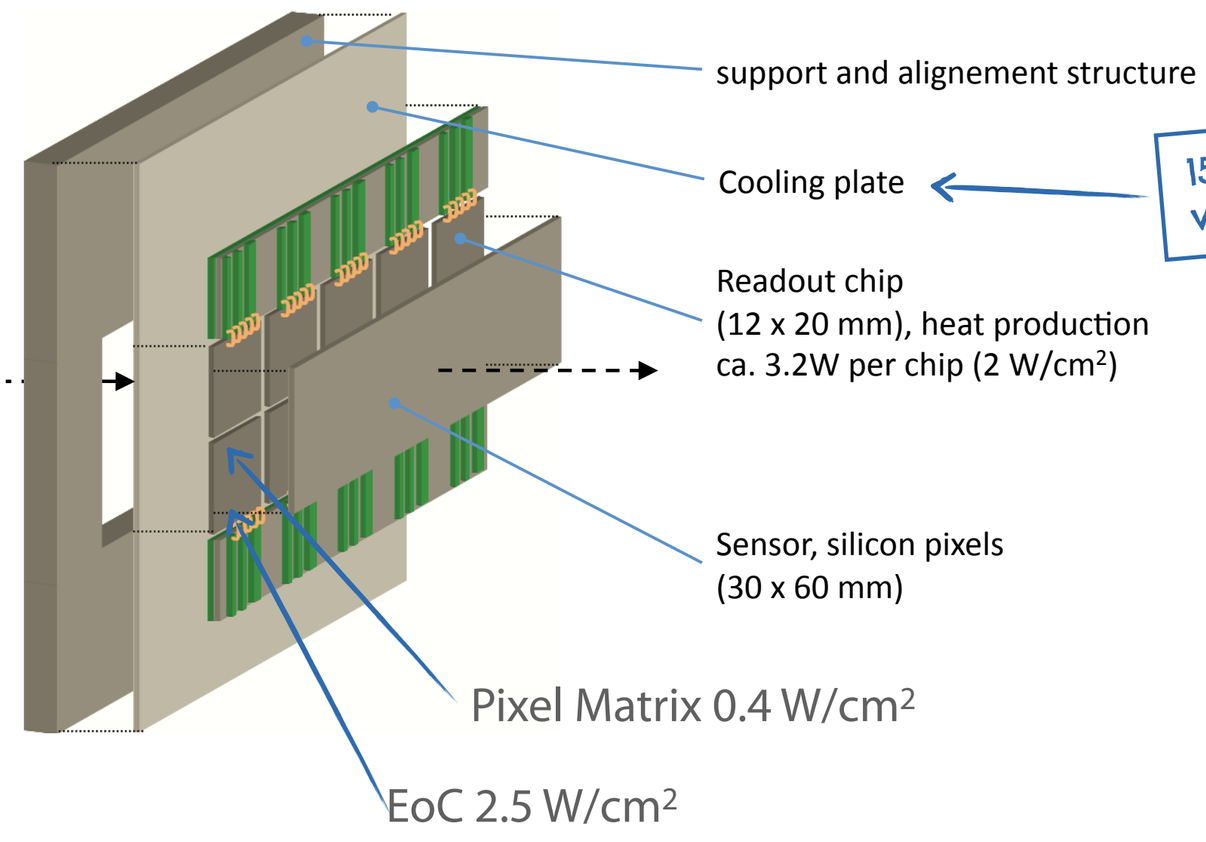
output

120 photolithography masks

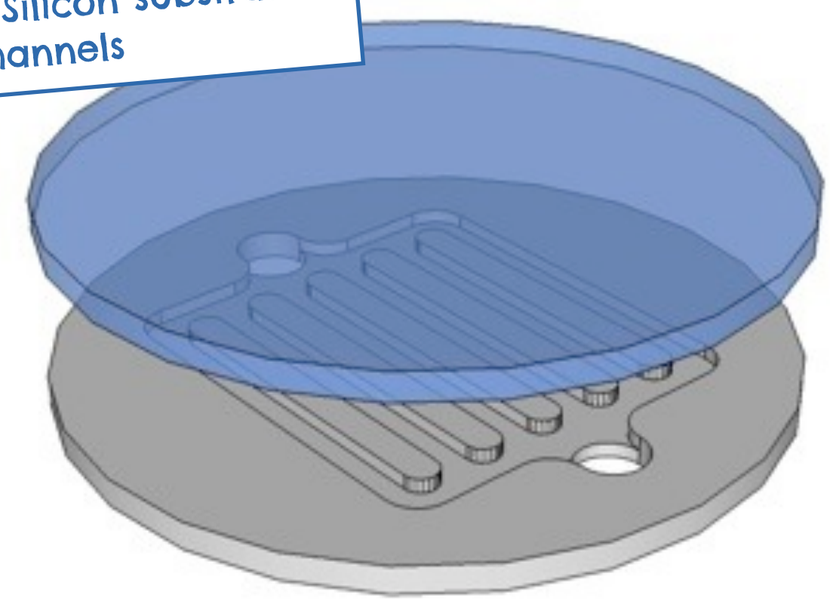
1000 processed wafers

NA62-GTK

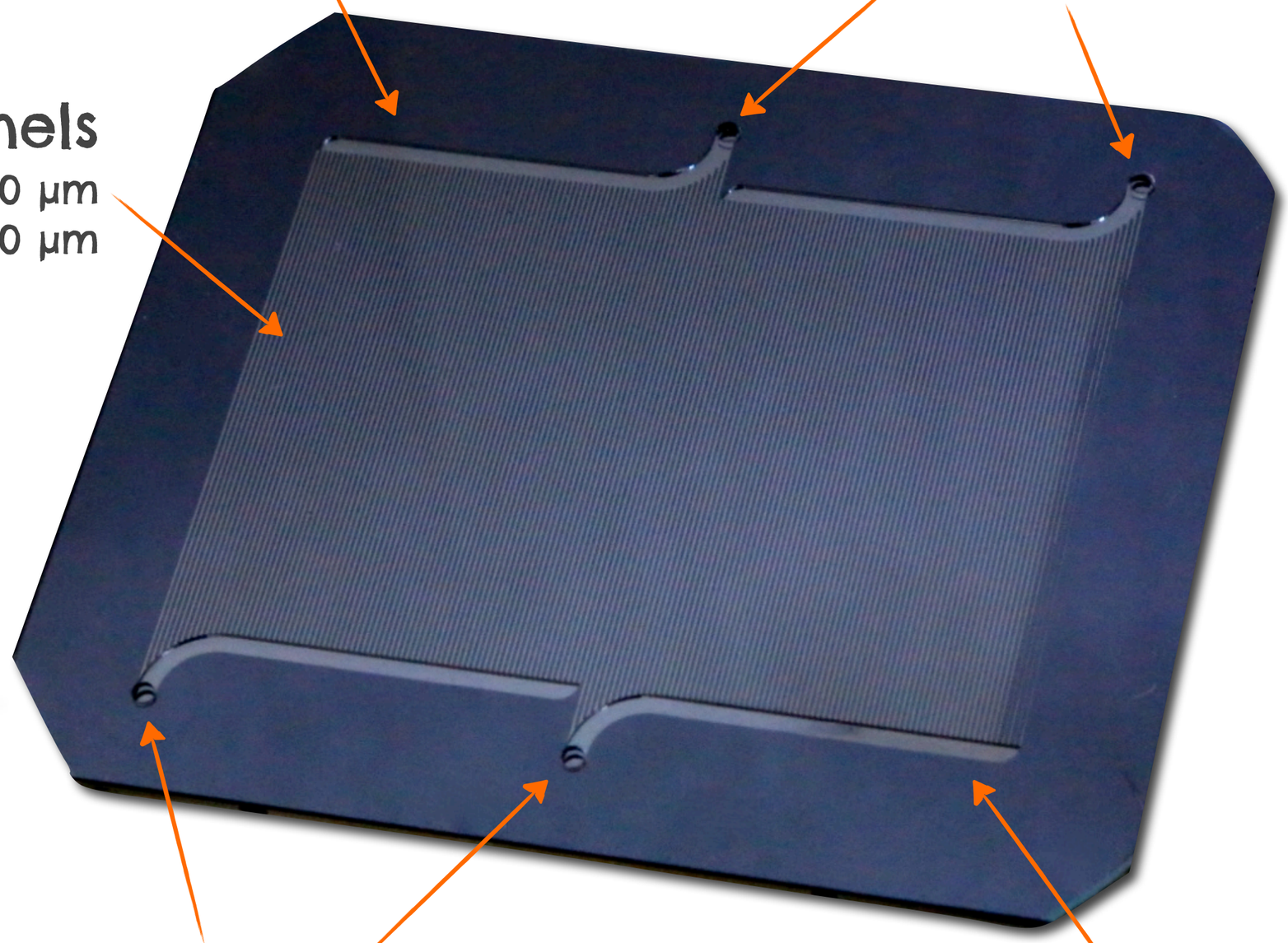




150 µm thick Silicon substrate with microchannels



Silicon Cooling Plate

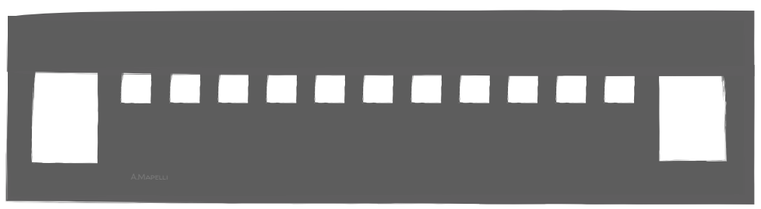


Microfabrication

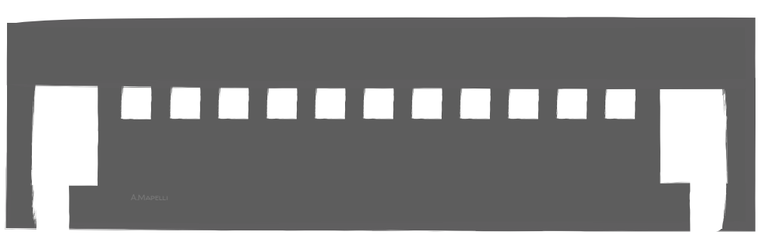
Prototypes fabricated at EPFL by PH-DT.
Six pre-production modules outsourced to IceMOS.

Si wafer

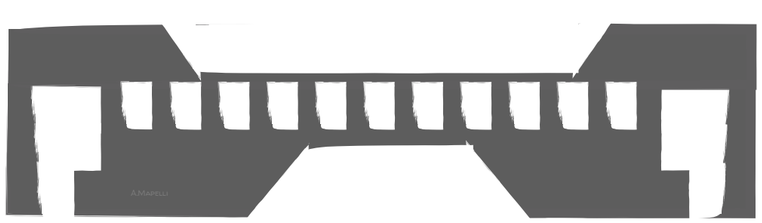
Plasma etching of channels & manifolds



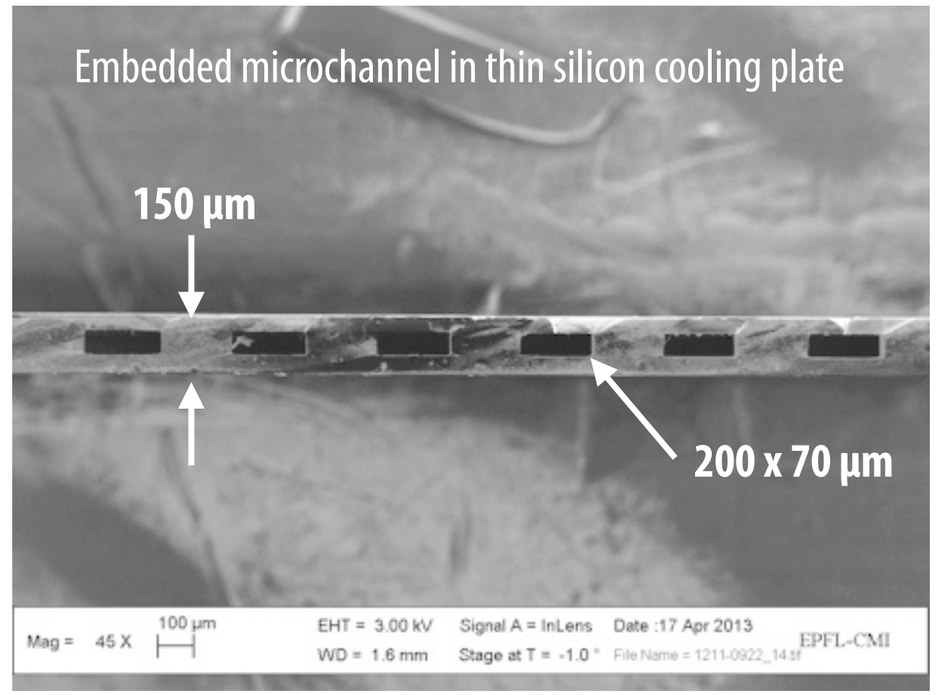
Bonding of Si cover

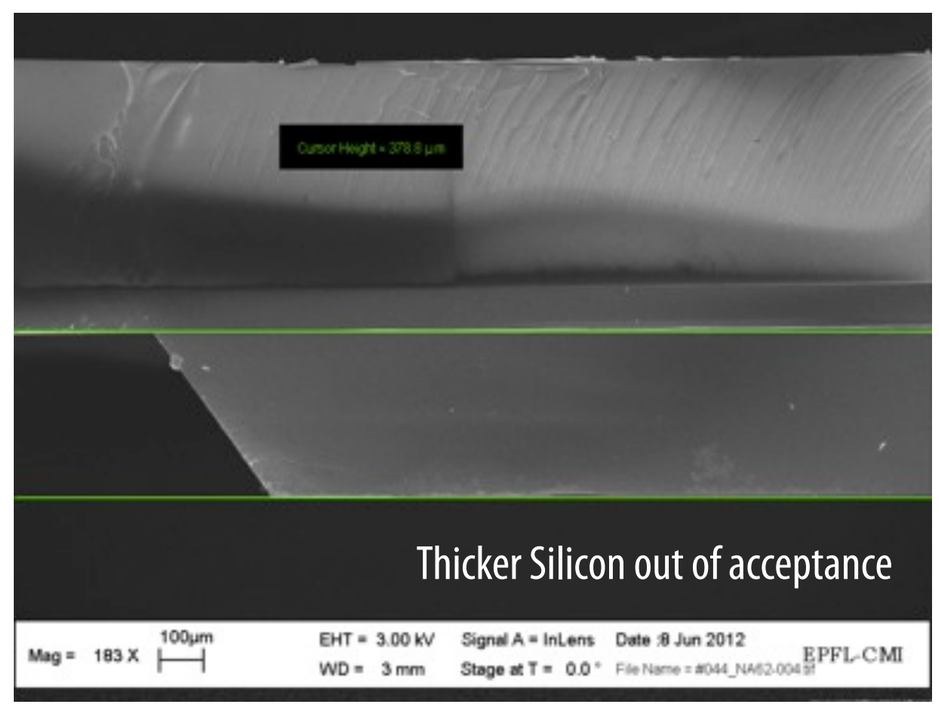


Plasma etching of fluidic openings



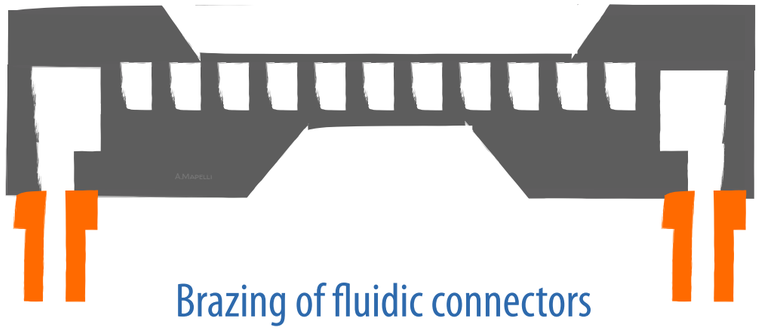
Wet etching of acceptance

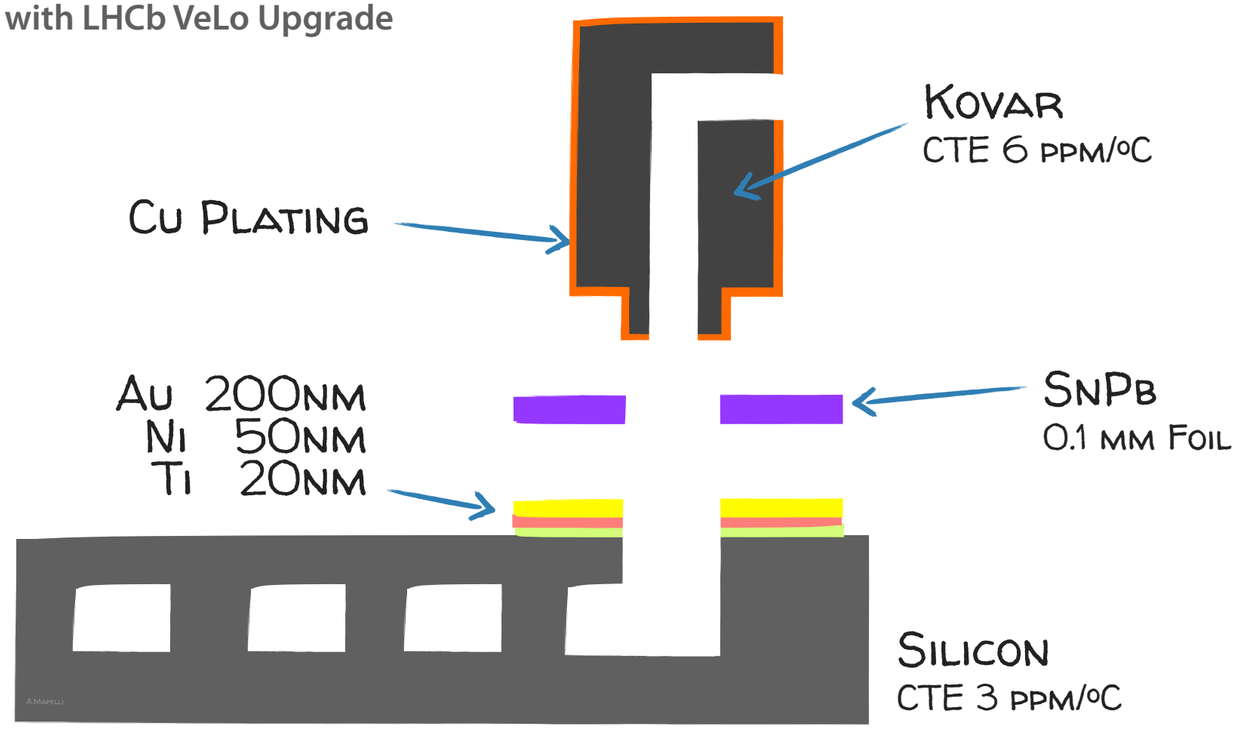


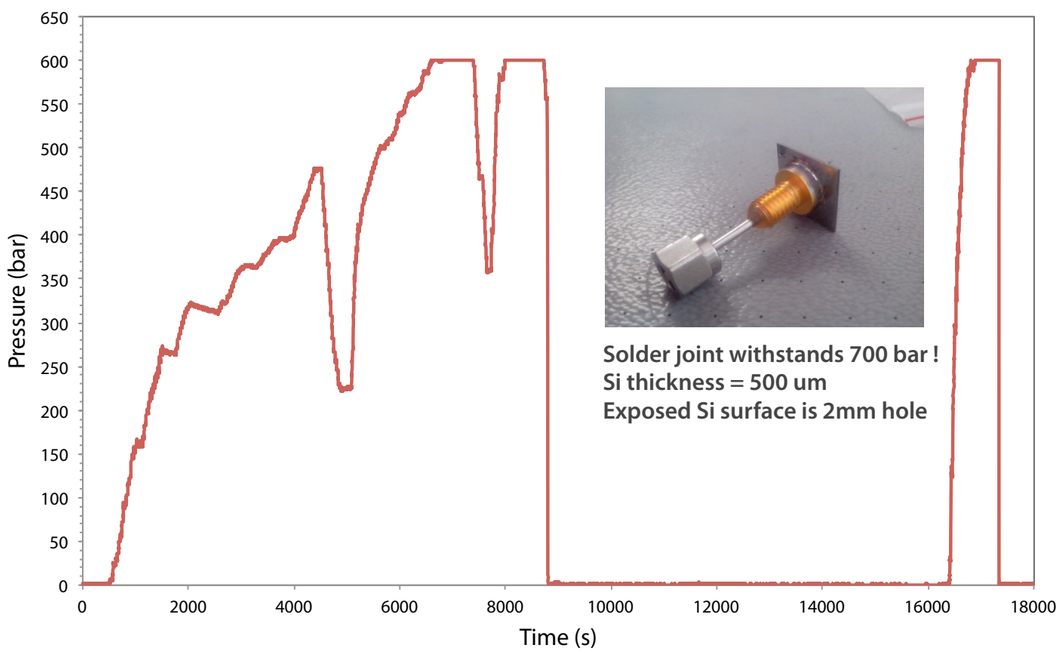


Fluidic Connectors

Common development with LHCb VeLo Upgrade

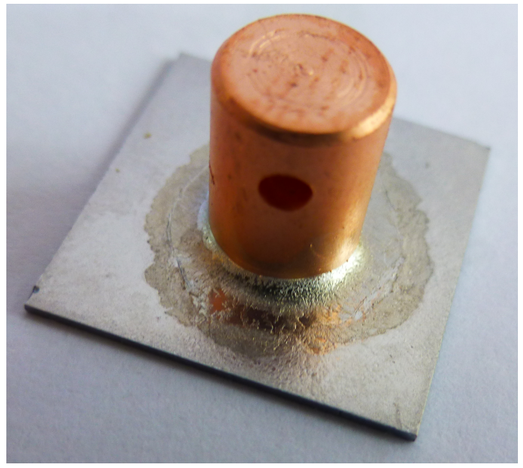






Limitation of the test set-up read-out at 600 bars
Limitation of the pump **700 bars**
No failure of the soder joint

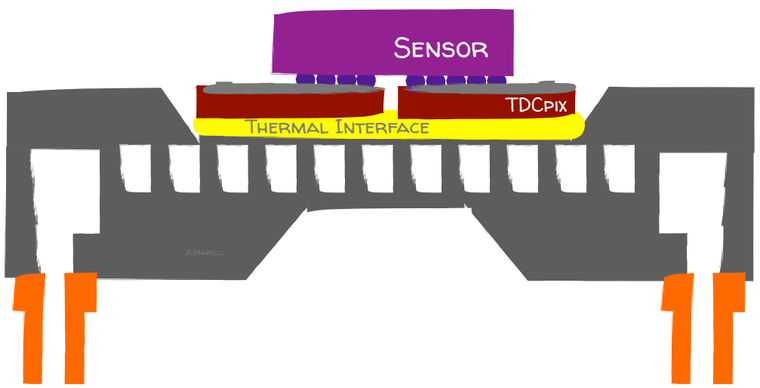
Inner diameter 1.6 mm

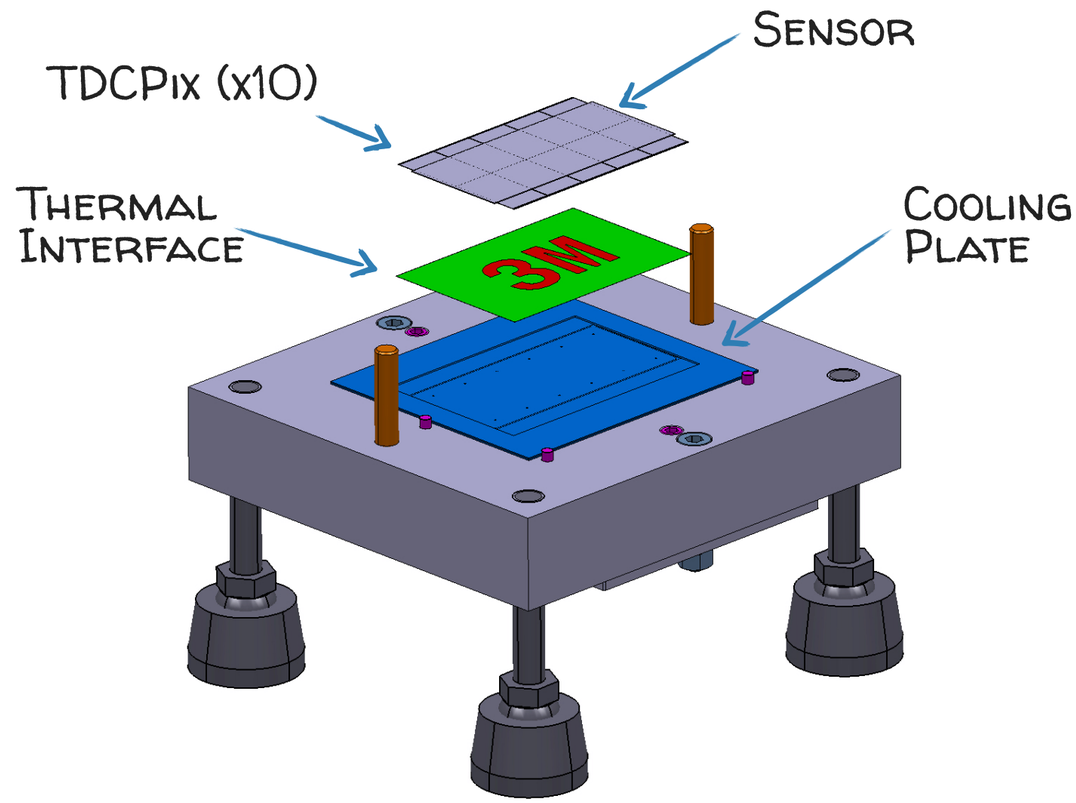


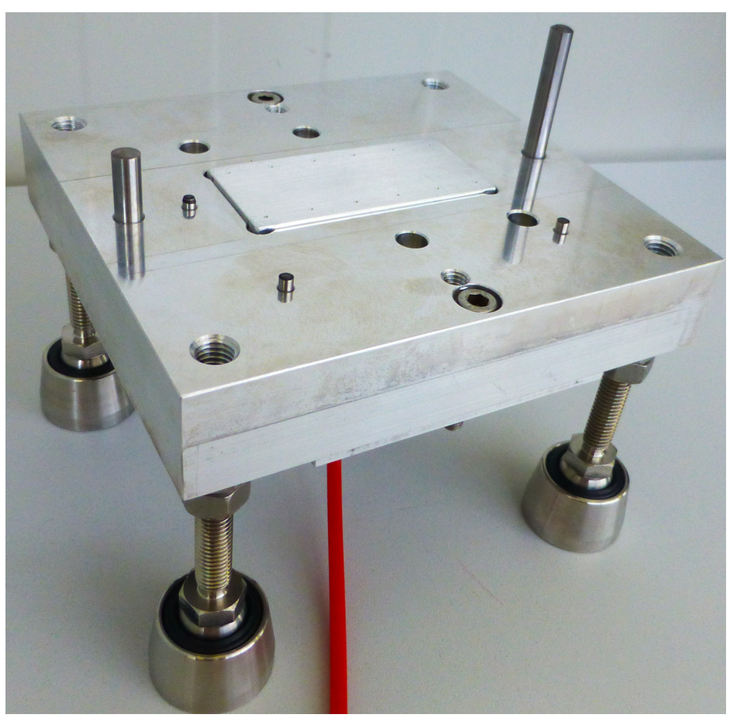
Silicon thickness 525 µm

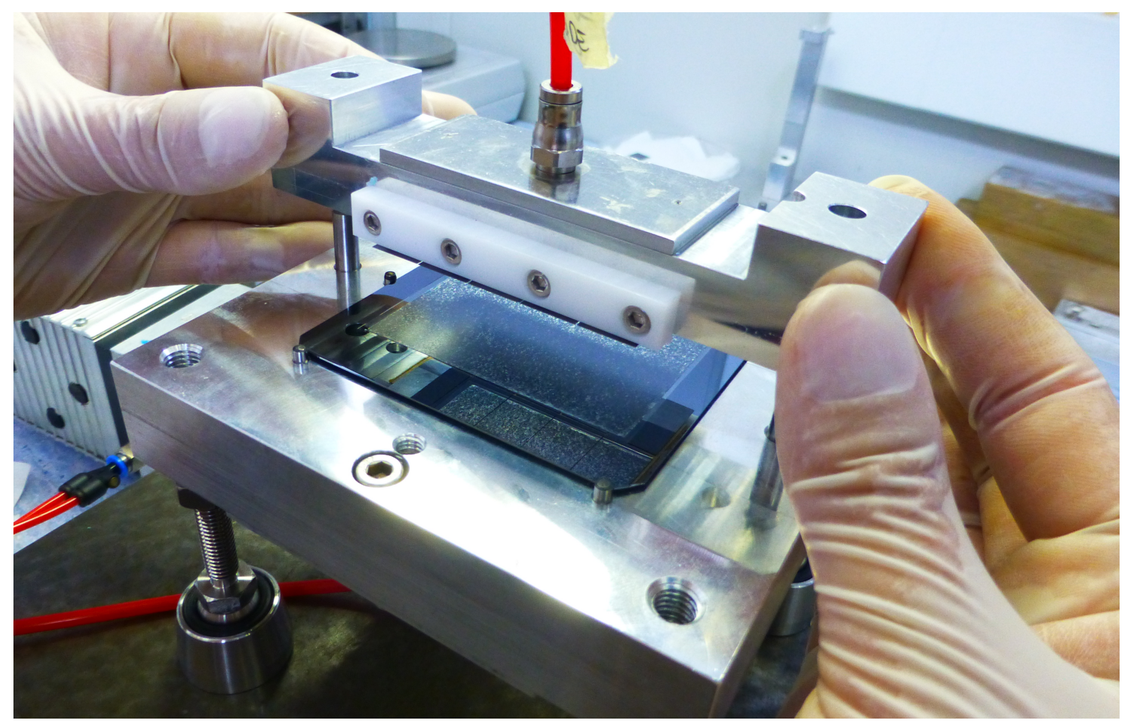
preliminary prototypes
size reduction and different geometries under study

Assembly to Sensor/TDCPix







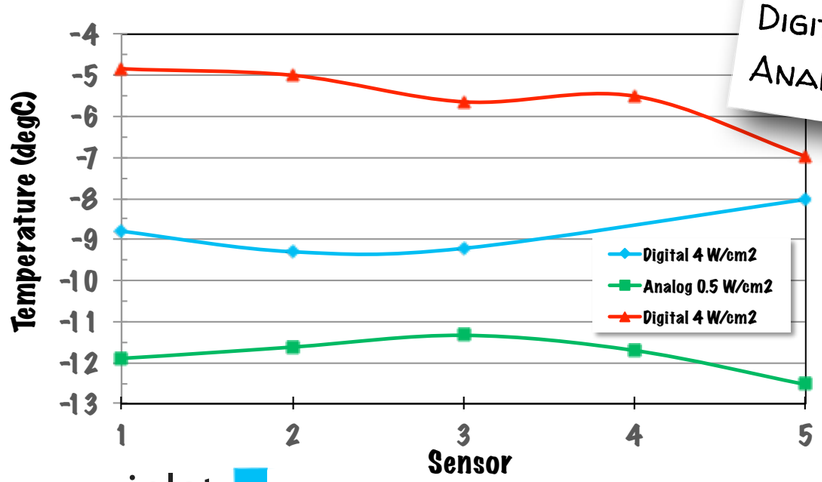


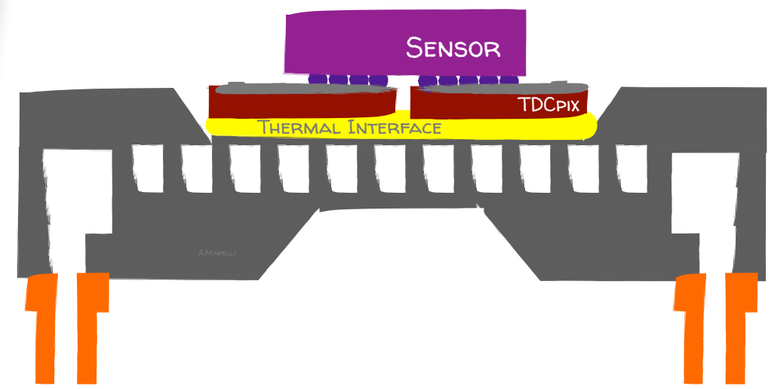
Experimental Validation

Liquid Cooling C_6F_{14}

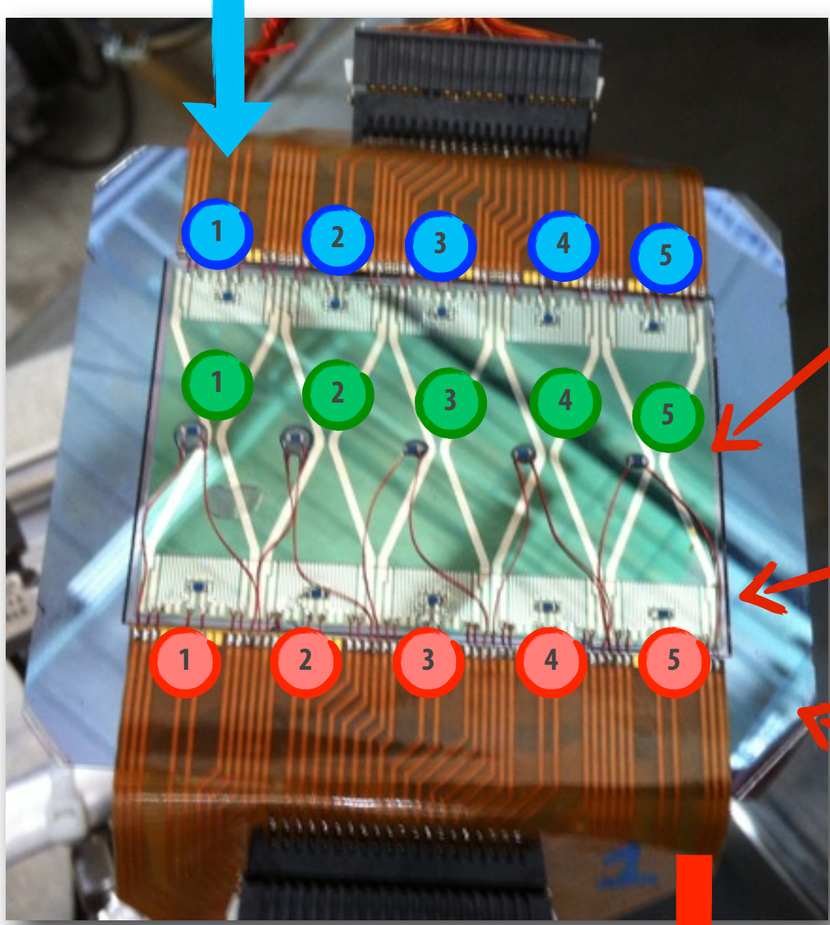
Nominal Power Dissipation 24 W
Results presented for extreme scenario 48 W

C_6F_{14}: 7G/S, −19°C AT INLET
DIGITAL POWER 38 W
ANALOG POWER 10 W





inlet



outlet

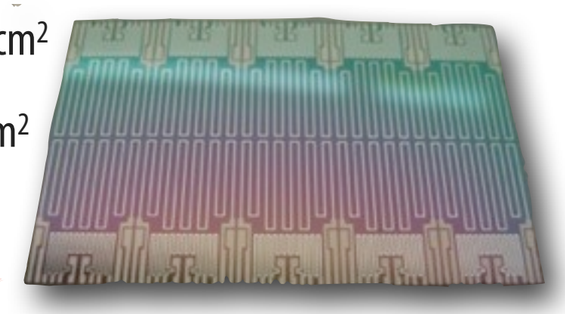
Sensor Dummy

200 µm thick Si

4 W/cm²

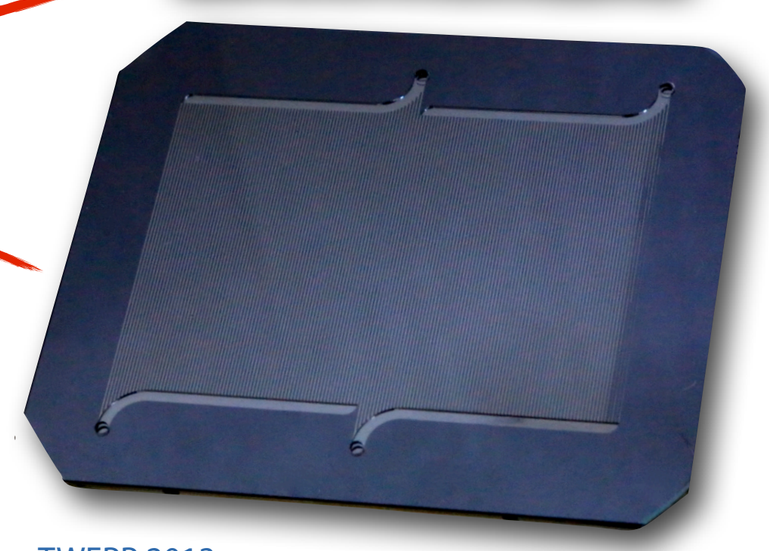
0.5 W/cm²

4 W/cm²



TDCPix Dummy

100 µm thick Si
20 metal lines to simulate power dissipation of analog and digital parts of 10 TDCPix chips

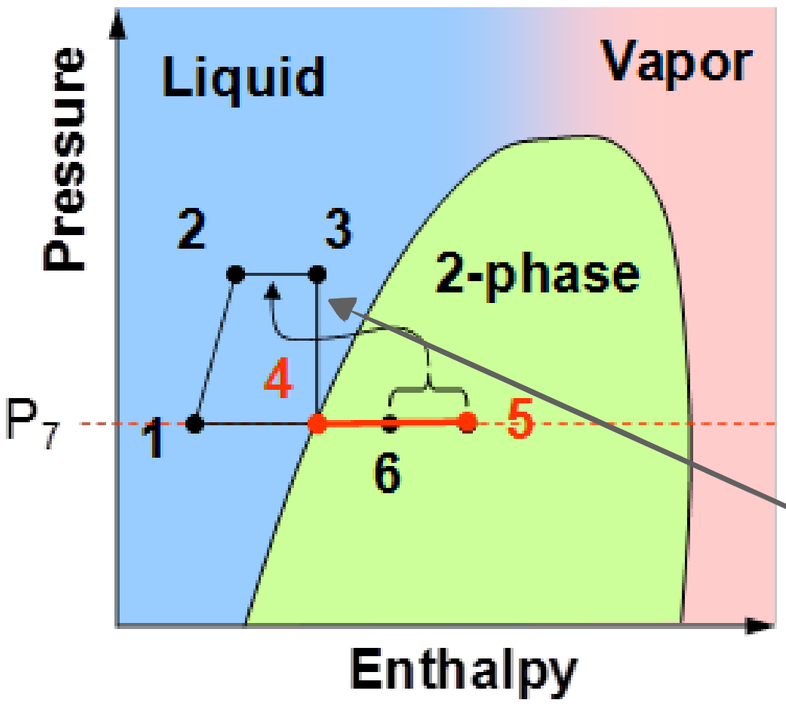


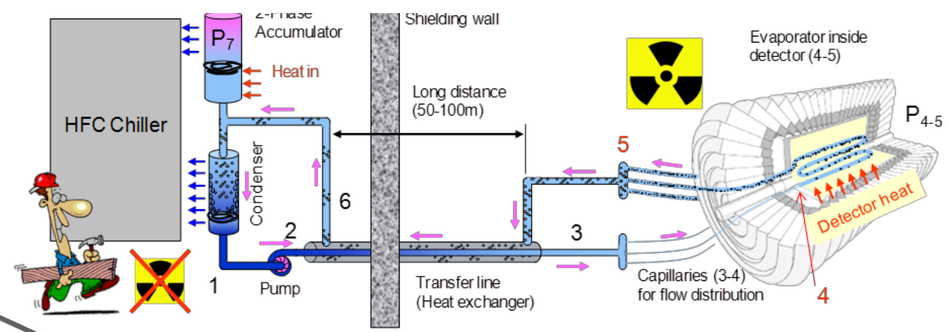
Cooling Plate

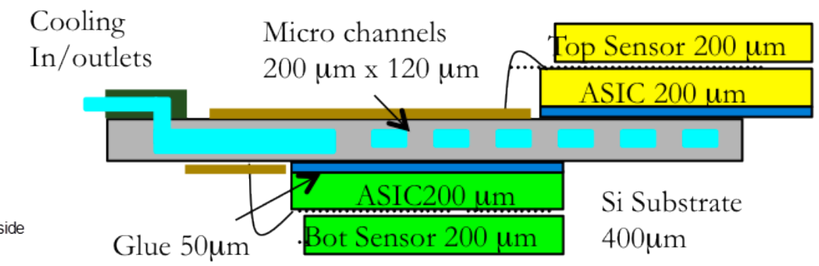
150 µm thick Si

LHCb VeLo Upgrade

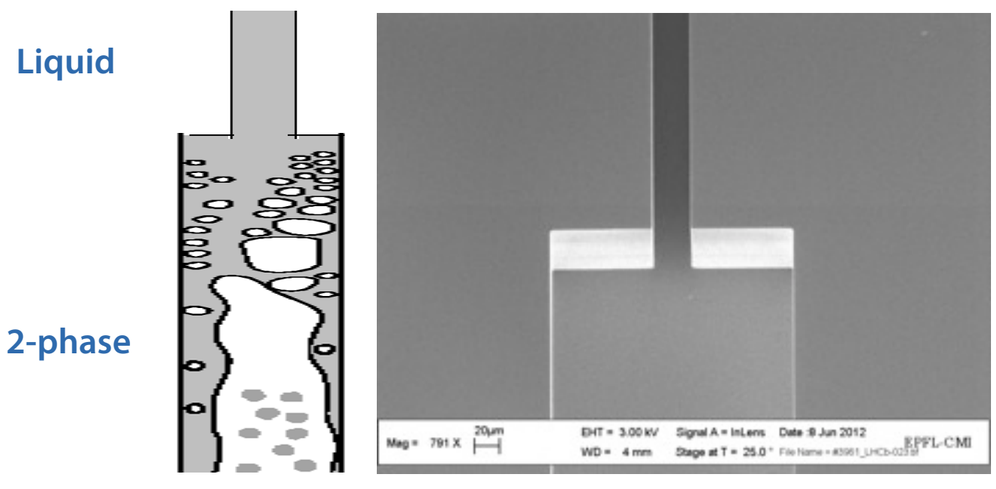
Evaporative CO_2 in silicon microchannels







Inlet restrictions
30 x 60 µm



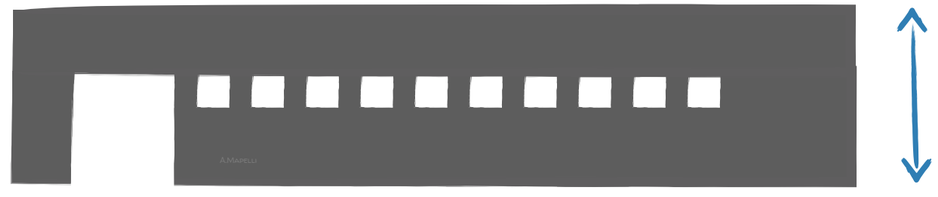
Transition from inlet restrictions
to evaporative microchannels

Microchannels
200 x 60 µm

LHCb VeLo Upgrade

1. operating pressure at low temperature ~15 bar
2. pressure at room temperature start-up ~60 bar
3. validation pressure with safety factor ~150 bar

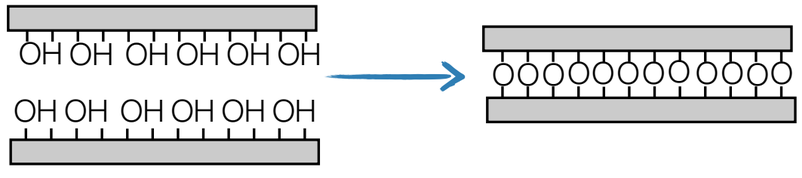
Si 165 µm

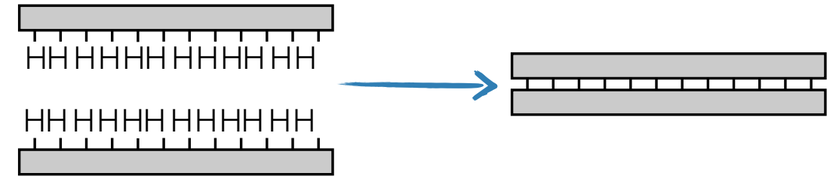


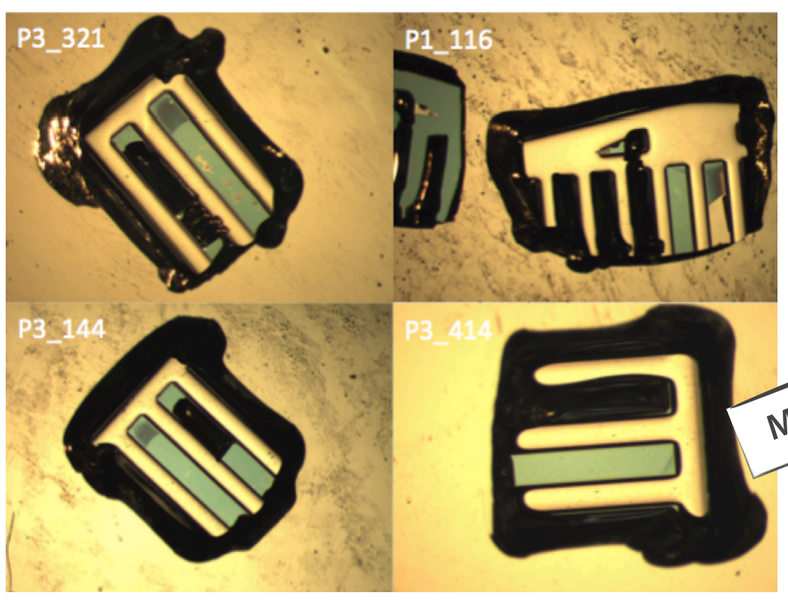
Si 400 µm

Samples produced by Leti-3s

Hydrophilic Bonding vs. Hydrophobic Bonding

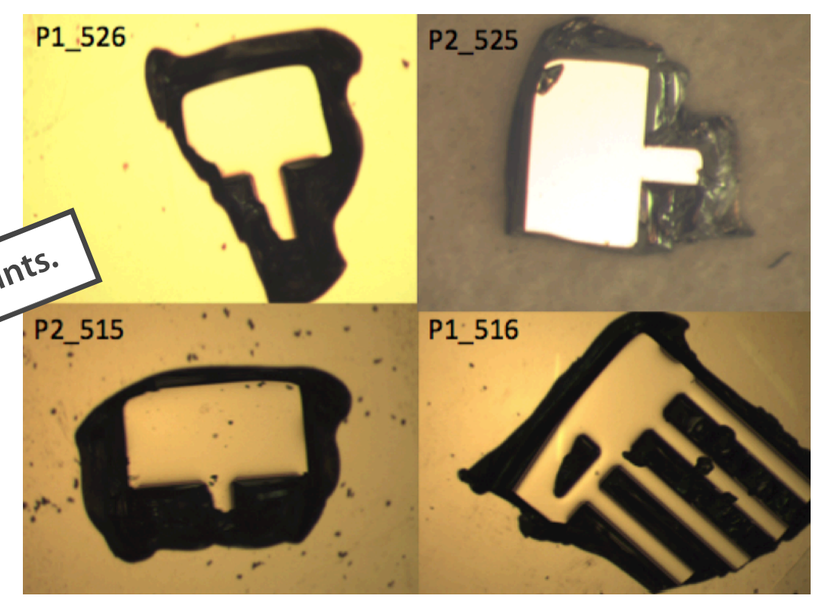






Round 1

Manifolds are the weak points.



Delamination + Si Rupture

No Delamination

Round 2

Rupture at 400 bars due to delamination

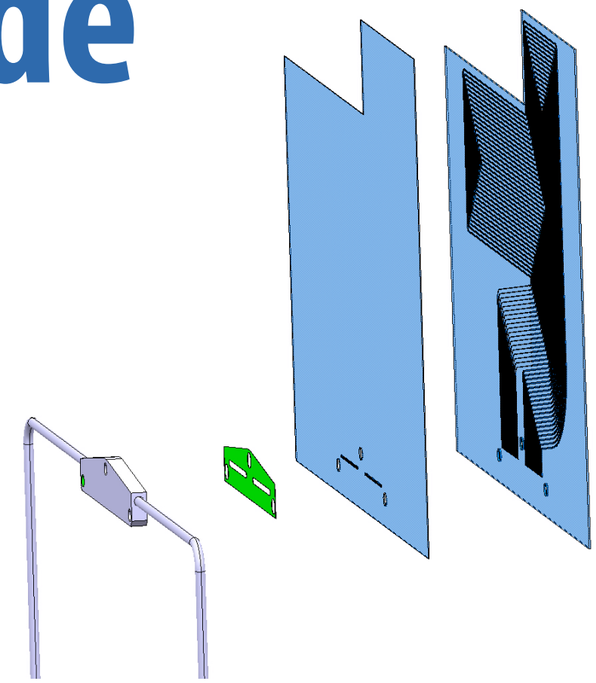
with improved connector (R. Dumps)

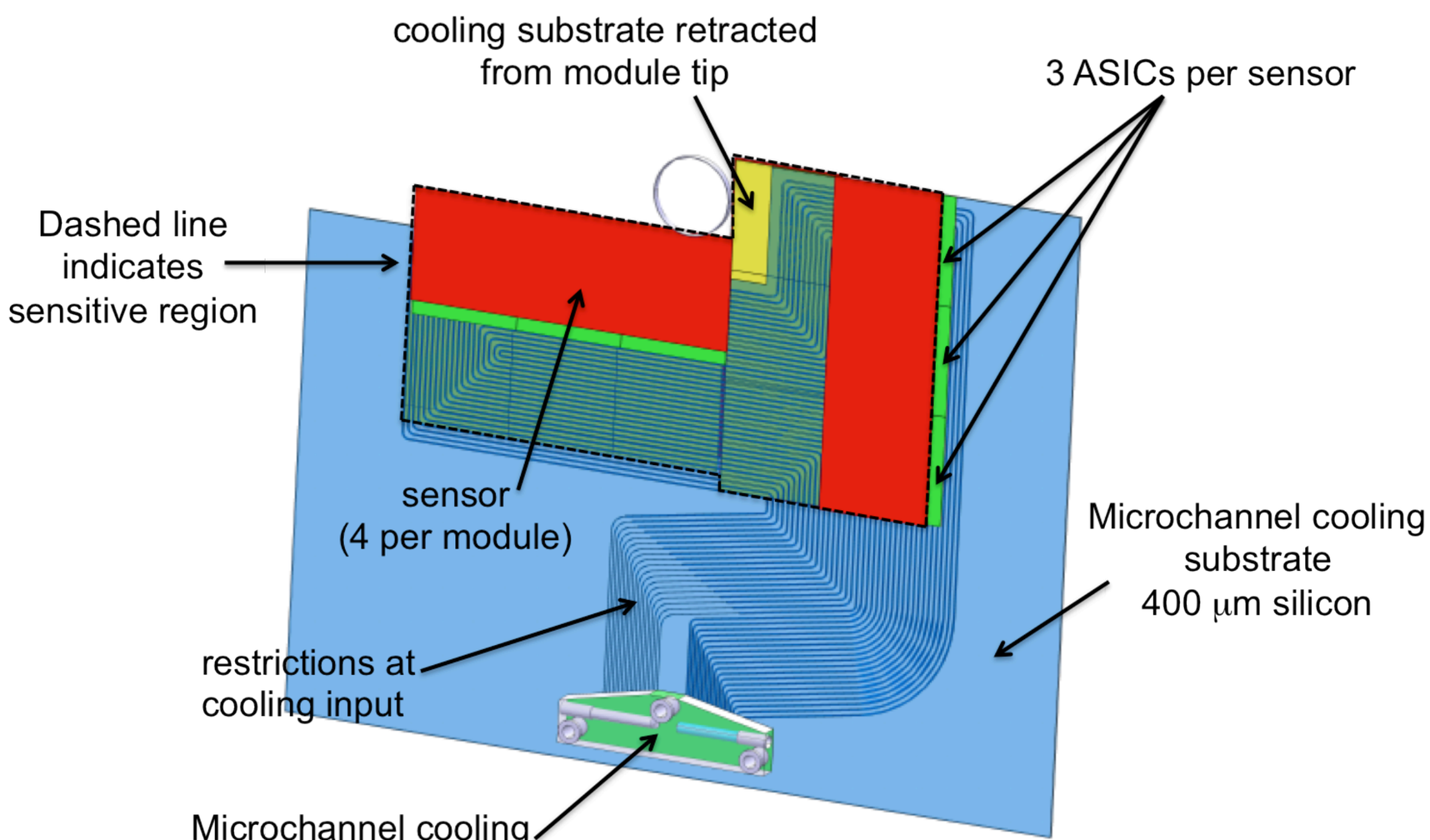
Hold 700 bars

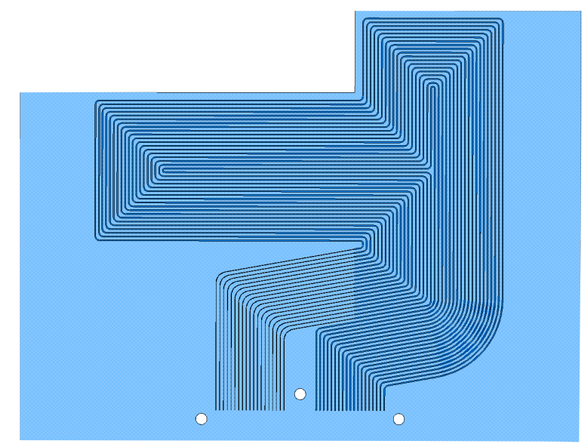
Limitation of pump

LHCb VeLo Upgrade

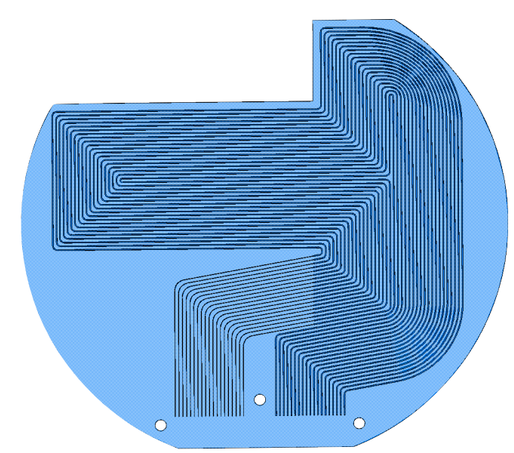
final design







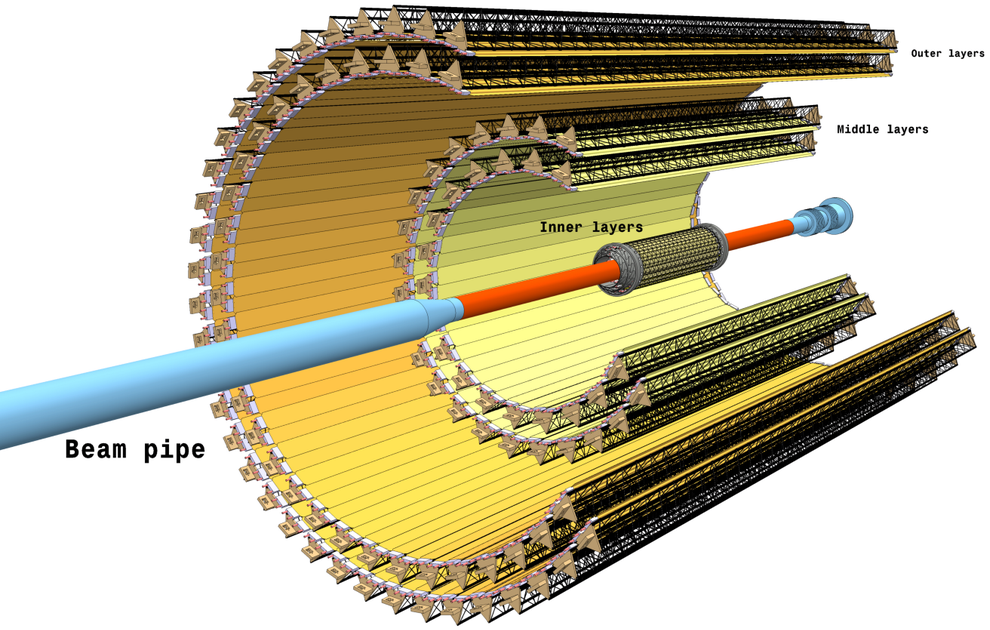
Fabrication by CEA Leti-3s



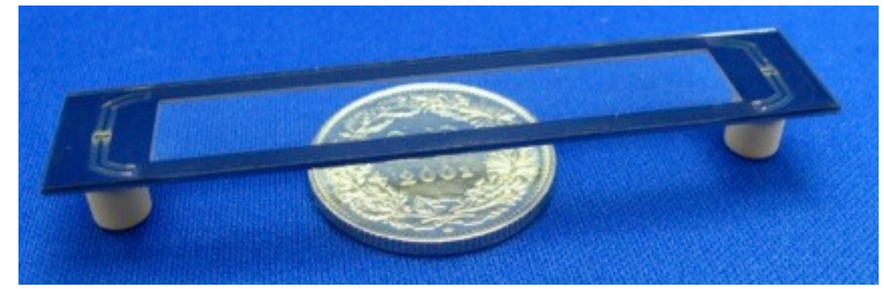
Prototyping at EPFL on 4" wafers

ALICE ITS Upgrade

Inner Layers

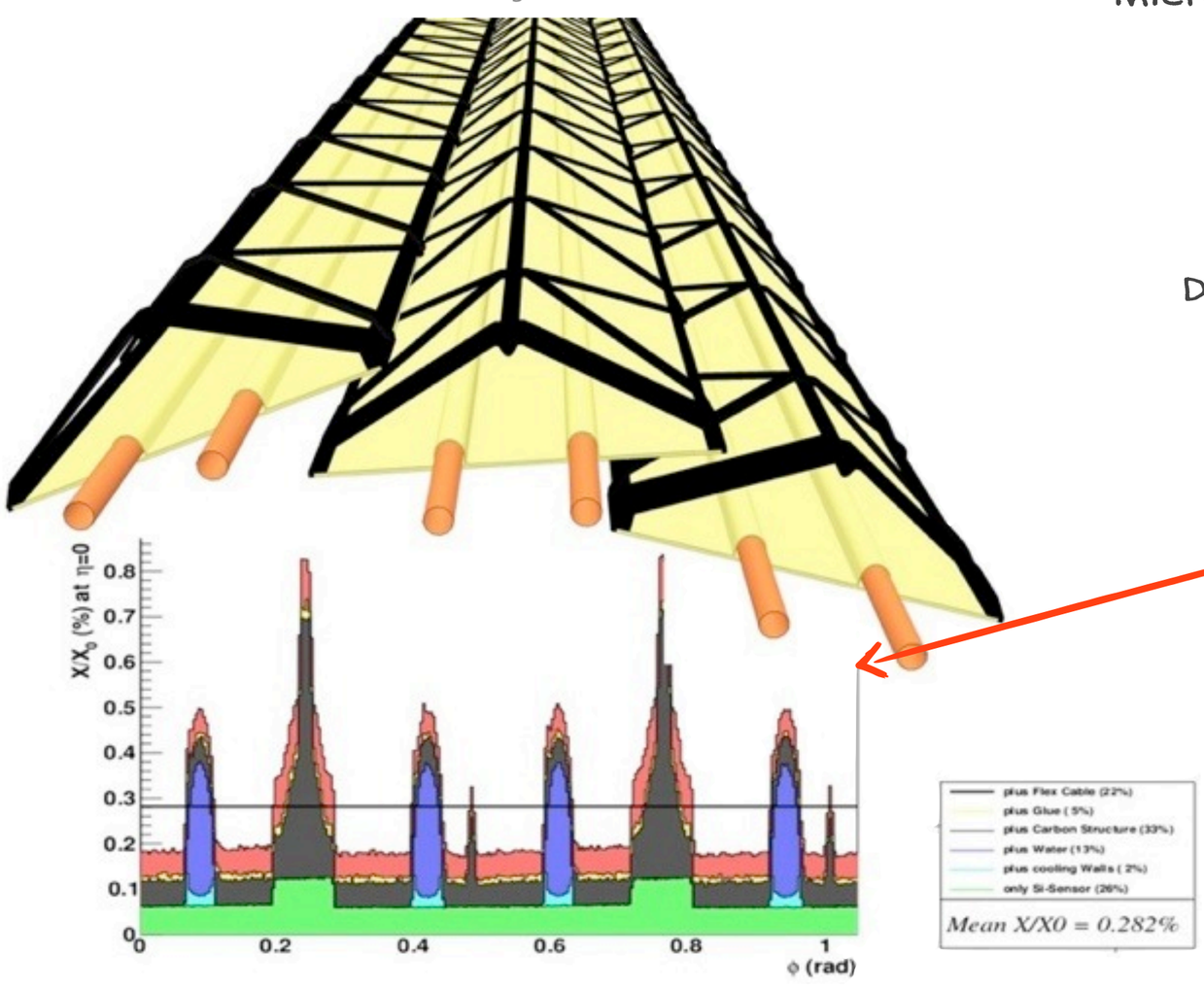


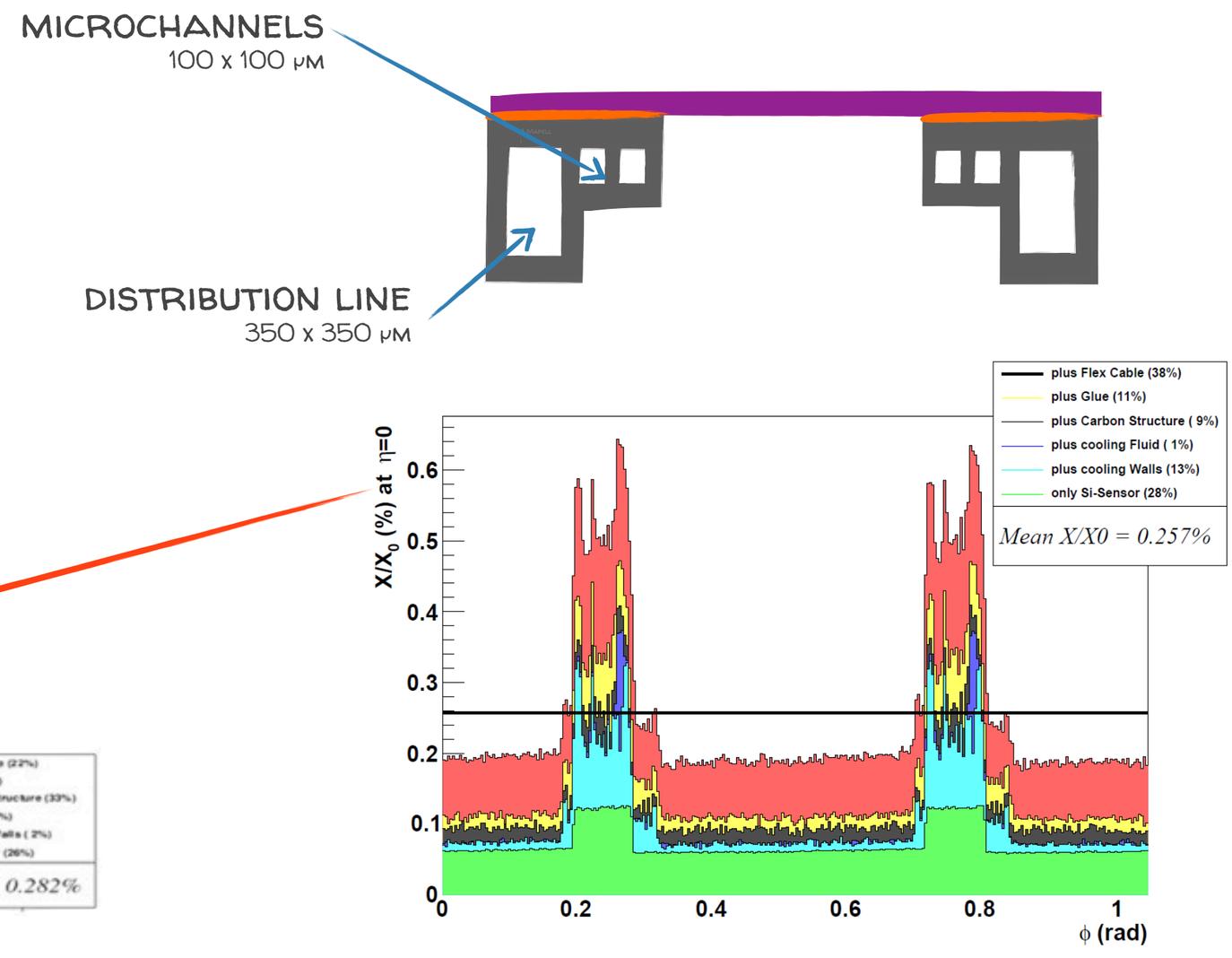
Silicon Alternative



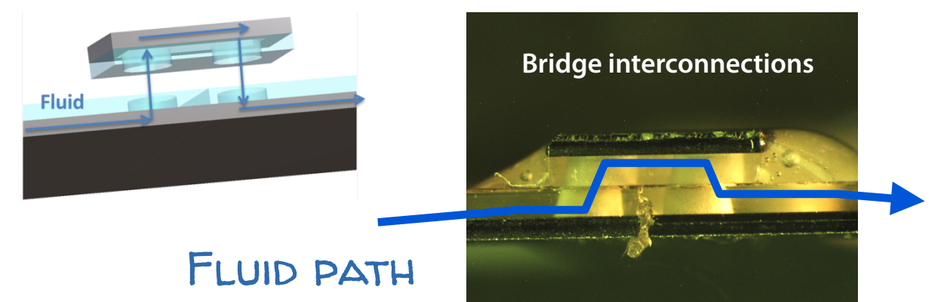
Baseline Solution

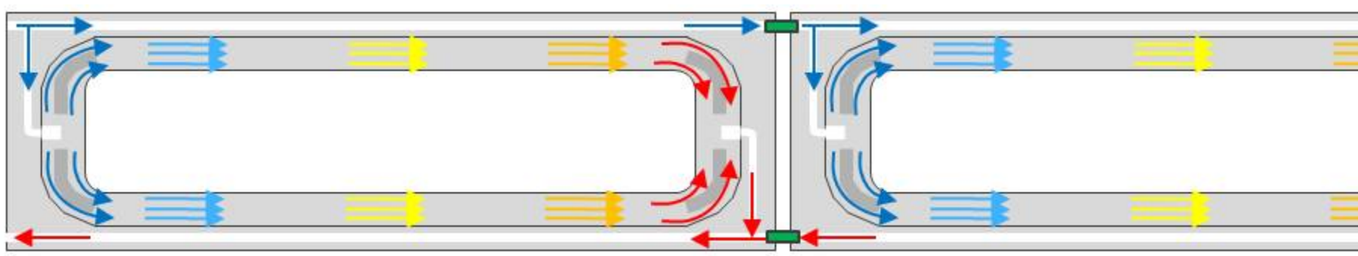
C. Gargiulo et al.

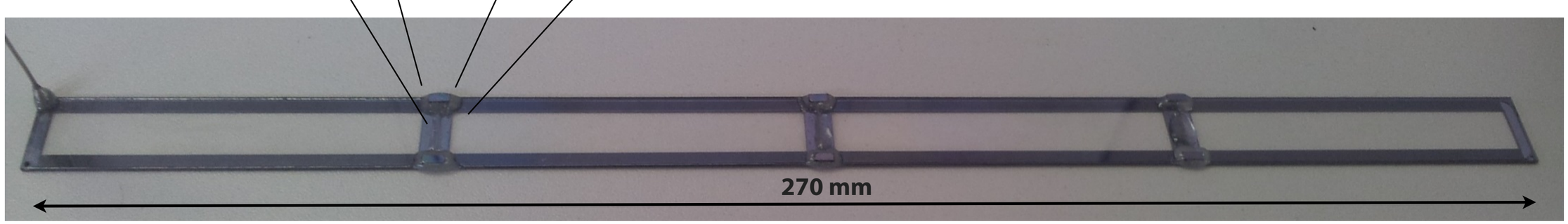




ALICE ITS Upgrade







4 frames are required for a stave from 4" wafers.
Only 2 frames required with single interconnection from 6" wafers (TMEC, Thailand).

9x silicon dummy chips with thin metal film (heater) glued on top of the stave.
Thermo-fluidic preliminary tests have started demonstrating the principle of operation.

Conclusions

Low-mass on-detector cooling systems can be integrated in light support structures and in silicon.

Silicon Microchannel Cooling has been selected as the baseline solution for

- the NA62 GigaTracker with liquid C_6F_{14}
- the upgrade of the LHCb VeLo with evaporative CO_2

A great effort is currently undertaken at CERN to study and develop reliable connectivity solutions both in-plane and out of plane