A counting pixel readout chip for imaging applications ⋆

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Abstract

A pixel readout chip for imaging applications has been designed and tested. It consists of an array of 12×63 pixels with an active pixel cell area of $50\,\mu\mathrm{m} \times 350\,\mu\mathrm{m}$. Every pixel contains a low noise charge sensitive amplifier, a CMOS comparator including individually adjustable thresholds, and a 15 bit counter realized using a linear feedback shift register. During data accumulation, every pixel independently counts the number of signal hits above threshold. After accumulation all counters in a column are sequentially read out, all columns in parallel. Thresholds can be set globally with the possibility of an individual threshold adjust in every cell. The chip can be operated with threshold settings in every cell well below equivalent noise charges (ENC) of 1000 electrons. The dead time of a pixel after being hit is $\sim 500\,\mathrm{ns}$. The chip is alive for data accumulation in $> 99.9\%$ of the total data acquisition time. For photon counting in biomedical or material science applications, a suitable sensor with high Z material can be bump bonded to the counting chip.

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Introduction

Pixel detectors based on silicon diode sensors flip-chip connected to dedicated front-end electronics chips (hybrid pixel detectors) are presently being developed for high rate and low noise applications in particle physics experiments [1]. In contrast to silicon strip sensors pixel detectors provide truly two-dimensional spatial information, an important feature in environments with high particle flux and large hit rates such as in very high energy proton-proton collisions. In hybrid pixel detectors, sensor cell and electronics cell precisely match in area. Contact between them is obtained using the metal bump bonding technique adapted for very small pitch sizes.

Also in imaging applications high rate capability and low noise performance are very important. This applies to medical X-ray imaging using sensors with high Z material and to material analysis using X-ray diffraction as well as to beta imaging used in biomedical autoradiographic applications. The imaging aspect is most directly approached by simply counting the number of hits by means of a dedicated chip circuitry in every pixel cell. The advantages of hit counting with real time processing compared to traditional film based methods are: linear and in principle infinite dynamic range, very good contrast performance and intensity analysis, intensity independent detection efficiency (no hazyness), multiple exposing capability and time resolved detection (film sequence), low dose capability and fast imaging turn around. In connection with semiconductor pixel sensors of high Z material (e.g. GaAs or Cd(Zn)Te) a counting pixel sensor with good X-ray absoption will be obtained.

The limitations of such devices mainly lie in (a) the spatial resolution, – at present of the order of several $10\,\mu$m – constrained by the pixel cell dimensions, and (b) the total active area of a device which - due to chip yield limitations - is difficult and expensive to fabricate in dimensions of $\mathcal{O}(0.1\mathrm{m}^2)$.

In this paper we report on the realization of a 12×63 pixel CMOS readout chip (MPEC) with counting capability in every cell. The chip has been designed adopting from the *BIER&PASTIS* chip [2] developed for the ATLAS pixel detector [4] at the Large Hadron Collider (LHC) at CERN [3]. A pixel cell consists of a high speed, low noise charge sensitive amplifier with current feedback followed by a fast discriminator [5], a control shift register, and a dedicated 15 bit shift counter [6]. The electronic design of the MPEC chip and its performance are described.

The MPEC pixel readout chip

The MPEC (Multi Picture Element Counter) chip contains a matrix of 12×63 individual pixel elements and is designed in the AMS $0.8\,\mu$m CMOS technology. The active electronic circuitry in every cell covers an area of $50\,\mu\text{m} \times 350\,\mu\text{m}$. For reasons of geometrical compatibility with existing detectors, the actual size is stretched to $50\,\mu\text{m} \times 433\,\mu\text{m}$. Every pixel cell consists of an analog part (a low noise charge sensitive amplifier and a discriminator), a control section and a 15 bit counter. The pixel cells are arranged column-wise as schematically shown in fig. 1. The sensor pixel will be connected to the chip pixel by bump bonding to the bond pad.

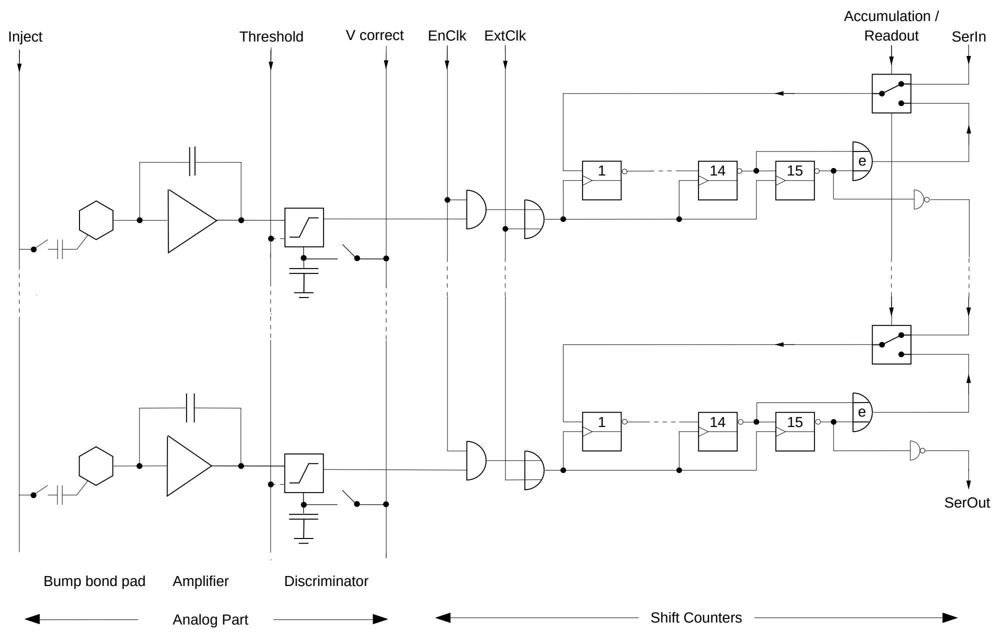

Fig. 1. *Schematic diagram of one column of the MPEC pixel readout chip.*

Data acquisition is done in two cycles: hit accumulation and readout. During hit accumulation, charge signals produced at the amplifier inputs due to the absorption of radiation in the corresponding sensor elements are amplified and detected by the discriminator, if their amplitude crosses a given threshold; the corresponding counter is then incremented. Accumulation is performed autonomously and asynchronously in all 756 pixel cells.

At the end of the accumulation cycle, the counters consisting of linear feedback shift registers of the type discribed in ref. [7] are switched to daisy chain operation (switch *Accumulation/Readout*) behaving as a single shift register in every column (clocked by *ExtClk*). The twelve columns of the chip are read out in parallel. The cells are not sensitive to radiation during the readout cycle. After readout the shift registers are switched back into counting mode and the accumulation cycle is restarted.

In the following sections, the different parts of the pixel cell are described in more detail. Fig. 2 shows the layout of one cell.

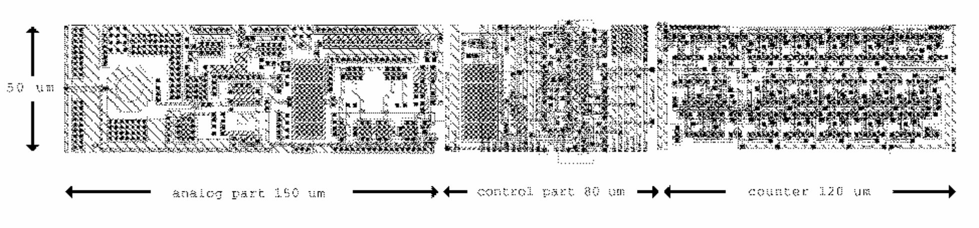

Fig. 2. *The layout of a single pixel cell. The analog part has a length of* 150 μm, *the control part of* 80 μm *and the counter of* 120 μm.

The analog part

The analog amplifier and discriminator part of the circuit is a full CMOS version of the circuit used in the *BIER&PASTIS* chip [2] developed for the ATLAS pixel detector [4]. It consists of a charge sensitive amplifier in folded cascode configuration and a discriminator to detect the signal. The amplifier uses a 1.7 fF feedback capacitor and an adaptive DC-feedback scheme, similar to the one proposed in [5], and is buffered by a pMOS source follower. The feedback circuit is designed to be insensitive to transistor mismatch and provides a fast return to baseline ($\sim 300 - 600$ ns for an input charge of $20.000e$ and feedback current dependent) with very high stability. Via the bump bond pad at the input of the amplifier connection to the sensor element is established. The design is made for positive polarity signals at the input.

The AC–coupled discriminator is a differential pair configuration. In order to reduce the threshold spread to a few electrons, two threshold controlling inputs are implemented. A global threshold value can be set for the entire chip. Individual thresholds can be applied by using the second high impedance input to every discriminator which is connected to a small capacitor on which a threshold correction charge can be stored. To avoid time dependent threshold drifts caused by charge leakage from the capacitor the control voltage ($V_{correct}$) must be periodically refreshed at low rate which has no effect on the data taking.

The control part

A control section has been implemented to provide good chip testability before ball bumping to the sensor. The control section contains a shift register with several functions: analog test pulses can be sent to selected cells via internal capacitors, digital test pulses can be fed to the counter part and threshold tuning can be performed in a selected cell. The shift register information can also be latched to mask off individual noisy cells. A wired-OR signal of all selected cells is available to test the analog part without the need to operate the readout.

The readout part

A shift register of N bit length can be configured with a single exclusive–OR gate to generate periodically $2^N - 1$ different states. As each state is directly related to the number of clock pulses, such a circuit can be used as a counter [7]. The circuit schematic of the counter cells is included in fig. 1. Every pixel cell contains a 15 bit shift register and some additional logic. The $14th$ and $15th$ shift register bits are tapped off, XOR-ed and fed back to the input of the shift register via a multiplexer. The multiplexer decides the mode of operation, either configuring the shift registers as individual counters, or daisy chaining them for the readout of the entire chip. The *ExtClk* signal clocks all shift register cells simultaneously and the contents of all counters appears serially at the *SerOut* pin (see fig. 1). The dynamic range is 15 bit without overflow detection. The principle can be easily extended to more then 15 bit without increasing the circuit complexity.

The counting shift register has been designed using dynamic logic for a very compact design. Regular refresh pulses are therefore needed. They are injected with a rate <1 kHzin parallel to all counters during the accumulation phase using the *ExtClk* input. Upon readout, the counter values must be corrected for the number of refresh clock pulses given during accumulation.

The advantage of the linear feedback counter circuit is its simplicity and small size. It allows a very regular and compact layout and reaches a high counting speed. A minor disadvantage is the fact that the generated counting sequence is a pseudo-random bit pattern. But for the moderate length of 15 bit, decoding can be easily done by means of a look–up table.

Chip performance

Performance measurements are presented with emphasis on the detection efficiency for the smallest detectable signals as well as the dead time of the readout chip. All measurements have been obtained without a sensor connected to the cell inputs and have been carried out using a dedicated PC-controlled chip test-system [8].

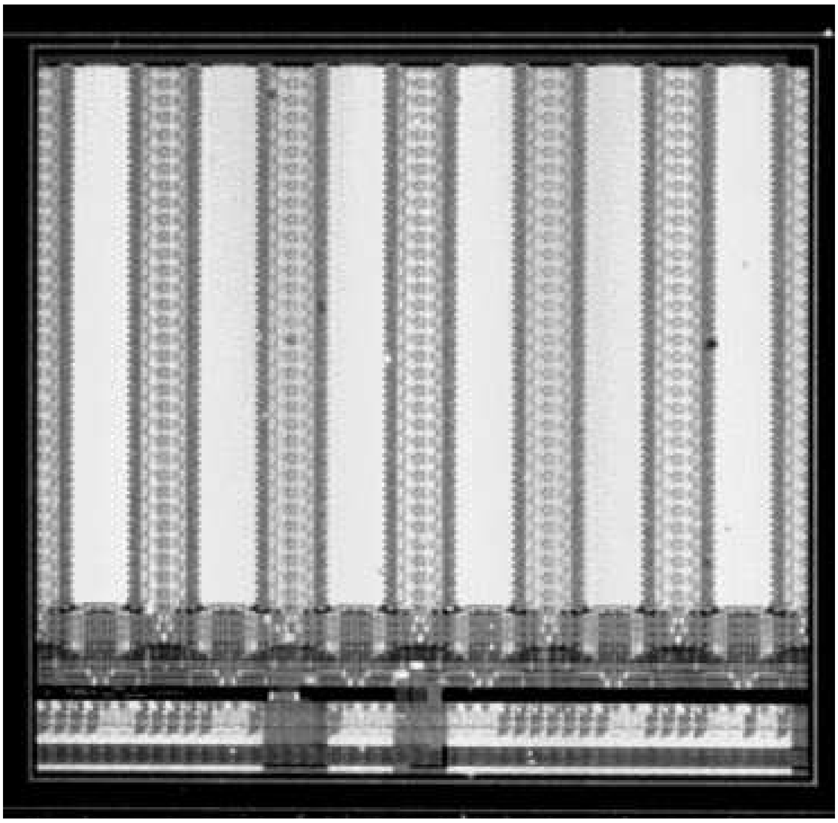

Fig. 3. *Microphotograph of the MPEC pixel readout chip. The active area is* 3.2 mm × 5.2 mm*. The bright part of the columns are the shiftregister counters. The cells are mirrored to avoid coupling from the digital to the analog part.*

For many biomedical applications such as autoradiography it is important to be able to detect signals with low amplitudes. For example, electrons from tritium beta decay generate on average only about 1500 electron–hole pairs in a silicon pixel sensor when they are absorbed. Therefore, one major goal is to operate the chip at a low and stable discriminator threshold. Reliable operation of the chip is possible for threshold voltage settings corresponding to equivalent input charges between 500 and 15000 electrons. Even at the lowest thresholds, quiet data accumulation without excessive noise hit rates has been observed.

To minimize the noise hit rate, the threshold should be set well $((4-5)\times\sigma_{noise})$ above the average effective noise amplitude which is the quadratic sum of the *amplifier noise* and the *cell-to-cell threshold dispersion*. Both contributions have been measured separately using the analog injection capability. The value of the *injection capacitor*, which usually is a major source of calibration uncertainty, is (12.5 ± 1.5) fF deduced from a measurement on a large array of identical capacitors implemented on the same chip.

Figure 4 shows the distribution of the noise measurements obtained from threshold scans using the charge injection capability of every pixel cell. The average

ENC is $\sigma_{amp} = 40\,e^- \pm 15\,\mathrm{e}^-$. The input capacitance of about 200 fF introduced by the sensor pixel and its bump connection to the bond pad is estimated to increase σ_{amp} to about 100 electrons.

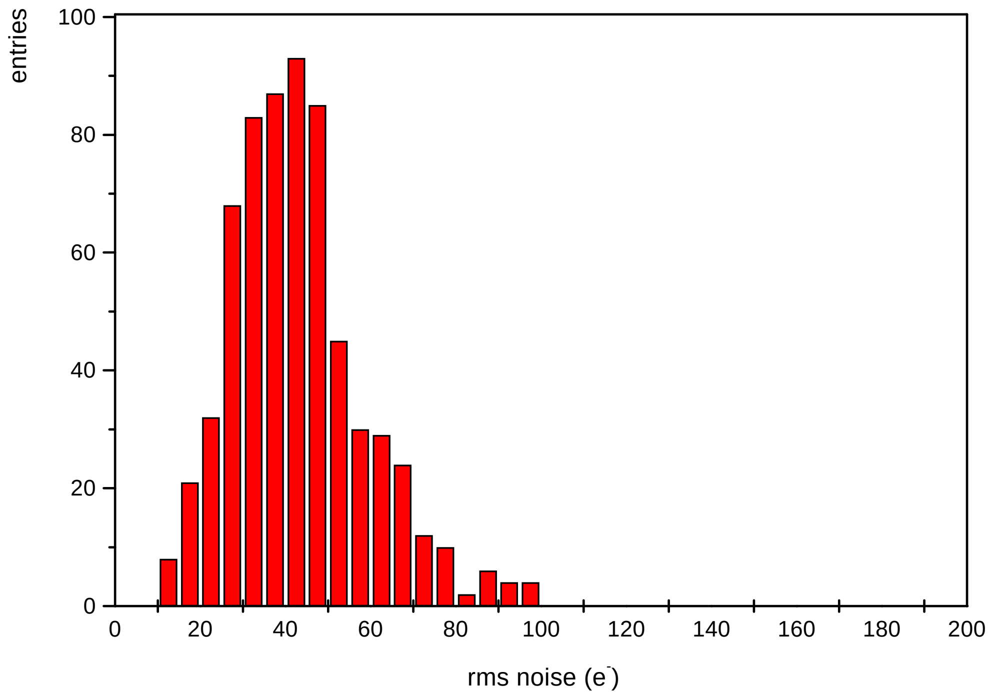

Fig. 4. *Distribution of noise measurements (ENC) obtained from threshold scans in every pixel cell. The average ENC is* (40 ± 15) *electrons.*

The cell-to-cell *threshold dispersion* depends on the actual threshold settings. It decreases with decreasing threshold value and increasing gain. No systematic variations have been observed. At threshold settings of 1000 (4000) e^-, dispersions of $\sigma_{thr} = 100\,(200)\,\mathrm{e}^-$ are observed. Introducing *threshold adjust* in every pixel cell by means of the dedicated circuitry reduces σ_{thr} to negligibly small values (less than $10\,\mathrm{e}^-$). Figure 5 shows the measured thresholds for all pixel cells of one chip before and after threshold adjust. The measurement also demonstrates that threshold scans can be performed at very low threshold settings. For the scans with threshold adjust the nominal setting was chosen to be $500\,\mathrm{e}^-$.

The *count rate capability* of one cell during accumulation is limited by the time the analog front end needs to recover after a hit was detected. This depends on the feedback current discharging the feedback capacitor and on the signal amplitude. A maximum counting frequency of 2 MHz has been measured implying a *pixel cell dead time* of 500 ns after accepting a hit. The counter itself is able to operate up to clock frequencies of 10 MHz in its present design, which has not been optimized for speed.

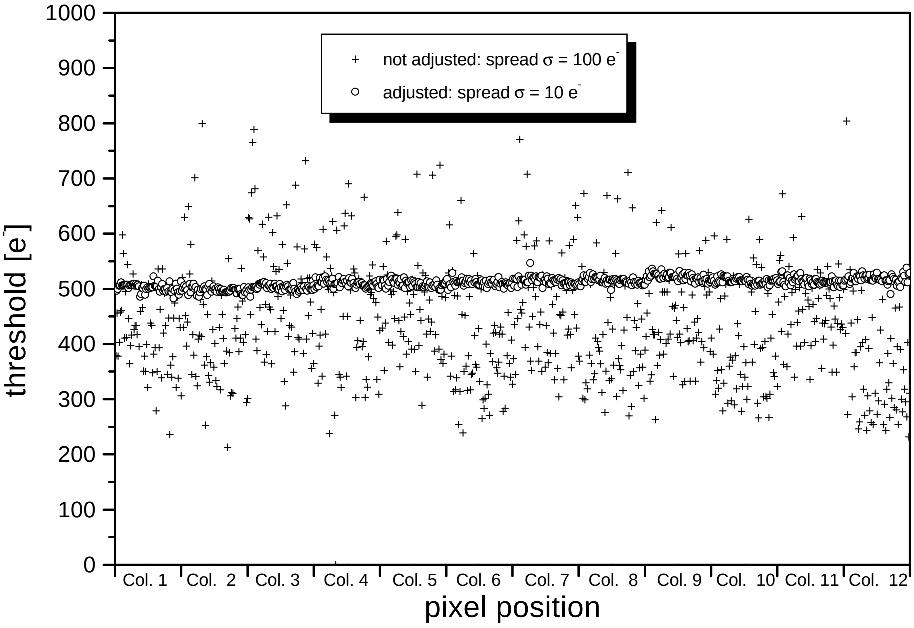

Fig. 5. *Threshold dispersion of the MPEC pixel readout chip before and after individual adjustment of the discriminator thresholds. The nominal threshold in the scan with adjusted thresholds was set to* $500\,\mathrm{e}^-$.

The readout time is determined by the shift clock frequency in daisy chain configuration. In this mode 15 bits times 63 cells in one column are serially transmitted. For a clock frequency of 10 MHz the minimum readout time thus is $\sim 100\ \mu$s. In order to assess the relative life time of the device during operation we compare the readout time to the duration of an entire data acquisition cycle. An arbitrary (i.e. infinite) dynamic range is obtained by repeated accumulation/readout cycles, the duration of which is determined by the counter depth. The readout must be started before a counter overflow occurs. Assuming a hit rate into one pixel of 100 kHz, which is already considered very high for typical imaging applications, the accumulation time can last at most 0.33 s. Thereafter a $100\,\mu$s readout cycle interrupts the accumulation. The relative accumulation fraction thus corresponds to 99.97% for 100 kHz pixel hit rate decreasing to 99.85% at 2 MHz.

The necessary refresh rate for the dynamic shift register depends on the digital supply voltage and on the temperature. At 300 K and for $V_{\mathrm{Digital}} = 3\,\mathrm{V}$ a refresh rate of 10 Hz is sufficient.

The power consumption of the analog part is about $40\,\mu$W per cell, while that of the shift counter depends on the counting rate. At the maximum achievable count rate of 2 MHz the total power consumption of the entire chip is 60 mW.

The following table summarizes the main features of the chip. The performance shown is obtained without sensor elements attached to the inputs. With a sensor connected the performance figures will deteriorate due to the additional input capacitance of about 200 fF per pixel.

threshold range (whole chip)	500 e^- – 15000 e^-
amplifier noise	$\sim$ 40 e^-
threshold spread (w. global setting)	$\sim$ 100 e^- at threshold = 1000 e^-
threshold spread (adjusted)	$<$ 10 e^-
pixel cell dead time	500 ns for $Q_{in} \approx 20.000e$
readout time (per image)	100 μs
dyn. refresh frequency	10 Hz
accumulation fraction	$>$ 99.9 % for 100 kHz pixel hit rate

Summary of the main features of the MPEC chip

The perfomance decribed here has been obtained using a prototype version of the MPEC chip. In a next generation we plan to add improvements such as the implementation of an overflow bit which can be read out or can start the data transfer, an expansion of the shift register length to 17 bit or more and the use of a faster shift register cell. The present cell geometry (50 μm $\times$ 433 μm) has been inherited from developments carried out for operation in particle physics environments. For imaging applications a more quadratic pixel cell geometry would be favourable which may also ease the connection to the sensor by allowing a wider bonding pitch.

Summary

A pixel readout chip with individual counting elements using linear feedback shift registers suitable for imaging applications has been designed, fabricated and tested. The detection threshold of the discriminator is tunable and can be set over a range from 500 electrons to 15000 electrons. Operation at very low thresholds has been found possible due to the very low noise performance of the amplifier (43e ENC) and tunable discriminator thresholds in every cell. The maximum rate capability per cell is 2 MHz. The dead time per image acquisition cycle is about 100 μs constituting an accumulation life time of 99.97% at a pixel hit rate of 100 kHz.

Acknowledgements

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