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1. EXECUTIVE SUMMARY

In the design of upgraded trackers for the SLHC experiments, the HEP community is facing a technological challenge that imposed a full review of the power distribution schemes used so far. The increasing density and number of front-end readout channels, associated with the use of today's microelectronic technologies, can be solved with the introduction of DC to DC converters. Those must however be compatible with the radiation and magnetic field environment to what they will be exposed to, while at the same time minimizing the amount of material that they introduce.

In view of enabling these DC to DC conversion based schemes, different topologies have been selected by different detectors and systems. On the basis of the resulting material budget and efficiency, two optimal conversion stages have been selected: a buck converter as main stage, capable of serving a full detector module, and an embedded on-chip switched capacitor voltage divider serving as second stage in some applications. The implementation of such schemes requires the qualification of a microelectronics technology that is compatible with the harsh radiation levels expected in the environment of the trackers at the sLHC, enabling the design of ASICs. The CERN expertise in this domain allowed qualifying two different technologies, although the radiation tolerance qualification is a long term process that requires an ongoing and tight interaction with the manufacturers.

Similarly, the required tolerance to intense magnetic field imposes the use of non ferromagnetic materials, which is an unusual constraint in power electronics. This is particularly demanding for the buck converter inductor that needs then to be based on an air core topology. The selected topology needs at the same time to introduce the minimum material and volume in the front-end system. The manufacturability of this component is now being addressed with magnetic components manufacturers.

The switched DC to DC converters are potentially a source of electromagnetic noise. The trackers front-end systems are very sensitive, and they are most likely susceptible to electromagnetic couplings. On the other hand, the use of an air core inductor results in higher radiated fields when compared with those emitted by ferromagnetic based coils. The noise sensitivity of currently available front-end systems at CMS and ATLAS was put in evidence, justifying the introduction of filters and shields. The noise optimization, the customization of coils and the design of a low mass but effective (and manufacturable) shield is a complex process, whose results are systematically evaluated on prototype boards and with system tests.

Several prototypes have been produced, using either radiation tolerance ASIC converters or commercial chips at CERN and at RTWH-Aachen. The noise properties are first characterized on dedicated test stands under standardized test conditions, enabling the validation of new layout techniques, of coil geometries and of shields. The characterized performance is also evaluated on front-end systems that put in evidence the suitability of the characterization procedure to predict the electromagnetic compatibility between given converters and systems. System tests have been successfully performed in this way on the CMS tracker endcap modules and on existing ATLAS barrel tracker staves and modules.

Similarly to the development of the buck converter ASIC, the second stage switched capacitor charge pump ASIC needed in ATLAS was developed. The first designs and studies carried out at PSI resulted in the design at CERN of a switched capacitor ASIC implemented in the now known radiation tolerant technology. The validation of this design will however occur once it is embedded in the final front-end ASICs.

2. INTRODUCTION

Today's high energy physics experiments at LHC embed large and very sensitive front-end electronics systems that are usually remotely powered through long cables. The innermost region of the experiments, the trackers, are those providing the largest density of channels, that must be powered with the minimal mass of cables and with reduced heat dissipation to avoid complex and massive cooling systems.

With the upgrade of the accelerator and its physics experiments already being planned, the detectors will require an increased number of electronic readout channels, which will demand more power. This increase of delivered power should be achieved without the addition of material in the detector volume, because of lack of physical space to run more cables and because material in this volume is detrimental to the physics performance of the detector. A solution to deliver more power without increasing the cable volume and mass relies on the distribution of power through on-detector DC–DC converters [1]. These converters must be capable of reliable operation in high radiation (total ionizing dose of 250 Mrad(SiO2) and neutron fluencies of 2.5×10^{15} n/cm^2, 1 MeV neutron equivalent, based on the simulated environment in the central tracker detector over its projected lifetime) and strong DC magnetic field environment (up to 4 T) of the detector.

To be compatible with this harsh environment, the electronic devices need to be designed in specific technologies that have been qualified for the required doses and fluencies. Together with the high degree of miniaturization required, this fact imposes the development of a custom ASIC for the implementation of the power controller and switches in a known, radiation qualified technology.

The LHC trackers operate with magnetic fields up to 4 T to measure the momentum of the particles. The DC-DC converters will be exposed to this DC magnetic field. This forbids the use of conventional ferromagnetic cores, since they saturate at flux densities below 3 T. Coreless (air-core) inductors have to be used instead, limiting the accessible values of inductance below 700 nH in order to maintain affordable size and mass for the large current that will pass through it [3].

A comparative study indicated that the buck converter is one of the most suitable converter topology for the intended application [2]. Given the range of available coreless inductors, the switching frequency has to be set beyond 1 MHz in order to limit the current ripple.

A typical tracker front-end system is made of strip detectors that are bonded to front-end hybrid circuits. These hybrids are fitted with several front-end chips. Several hybrid and detector modules are then mounted together to form a stave or a supermodule [3]. Based on this and on the estimated power requirements of the hybrids, an optimal powering scheme based on DC-DC converters (Figure 1) has been proposed for ATLAS [1], that relies on an input voltage bus (10V) distributed along the stave to all the hybrids. Each hybrid circuit would be equipped with one Buck DC/DC converter delivering an intermediate bus voltage (2.5V) that brings the power to each front-end chip with a conversion efficiency of 80%. Each front-end chip would then convert the intermediate voltage down to the levels that it requires (1.2V and 0.9V) through integrated switched capacitors point-of-load DC/DC converters, whose efficiency is expected to be around 95%. The need for switched capacitor converters depends on the technology used for the front-end ASICs. Schemes based on the use of buck converters without switched capacitors were also adopted for the CMS tracker and pixel detectors.

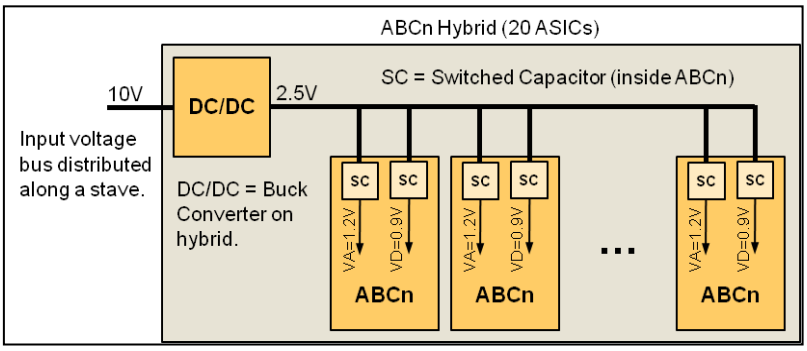

Figure 1: Powering topology.

Beyond the environmental constrains that are set to this powering scheme, the electromagnetic compatibility between the tracker electronics and the DC-DC converter used to power it is essential. The sLHC tracker powered from DC/DC converters in close proximity of the front-end electronics must be able to achieve levels of performance equivalent to those obtained when using remote, regulated power supplies in the present system. The proximity of switching converters with the strips and front-end ASICs (less than 5 cm) expose the front-end electronics to conducted and radiated couplings that could compromise the tracker performance. The compatibility can be achieved by appropriate design of the converter, together with an adequate integration in the front-end system. In order to succeed, the susceptibility of the front-end system to conducted and radiated noise needs to be explored. On the other hand, the conducted and radiated noise properties of the converters need to be characterized in a standard manner, enabling their EMC optimization for the targeted system.

The qualification of radiation tolerant technologies enabled in the early stage of the project the development of buck converter ASIC samples that were themselves qualified for radiation tolerance. However the availability of such technology in the long term is a critical issue and therefore the evaluation of new technologies is constantly carried on. The converter board development issues have been addressed in parallel to the ASIC development, first using commercially available (but not radiation tolerant) devices, and in a later stage using the ASIC samples. The knowledge acquired with these prototypes in controlling the emission of electromagnetic noise has now resulted in very low noise power converters that are compatible with tracker front-end electronics. Actually the focus is given on the integration and manufacturability of these converter boards: contacts have been established with the industry for the design and production of very compact custom air core inductors needed by the converter. Studies are also being carried on for the design and production of low mass shield cases.

3. POWER ASIC DEVELOPMENTS

This section discusses the development of the building blocks necessary for the implementation of the distribution scheme proposed in Figure 1, starting (3.1 and 3.2) from the more challenging buck converter performing the conversion stage 1. This converter should be capable of converting an input voltage of 10-12 V, far exceeding the voltage rating of the mixed-signal CMOS technologies typically used for FE ASICs. The mixed requirements of high voltage capability and radiation tolerance render the choice of the technology for the design of the converter a crucial enabler for a successful development.

3.1. TECHNOLOGY SELECTION

The need for a magnetic field tolerant converter imposes the use of an air-core (or coreless) inductor, limiting the available inductance value to below about 700nH [1]. This imposes a switching frequency of 1-4MHz, which is beyond typical converter implementations. To efficiently drive the switches at this frequency, and to achieve the highest miniaturization, the full converter should be integrated in a single Application Specific Integrated Circuit (ASIC) with only the inductor and capacitors off-chip. The appropriate semiconductor technology for this ASIC should therefore offer both “core” low-voltage transistors (for the control circuitry) and high-voltage transistors (to be used as power switches and wherever direct connection to the input voltage is needed, such as for the internal regulators).

For a converter with an input voltage of 10-12 V, the high voltage transistors shall be rated to withstand a drain-source voltage (Vds) of 14-20 V at least. Several technologies offering this combination of core and high voltage devices exist in the marketplace, based on standard mixed-signal CMOS technologies (0.35-0.13 µm nodes) to which a high-voltage module extension has been added. The radiation effects affecting the low-voltage devices in these CMOS nodes are well known. In particular, these circuits are not sensitive to displacement damage up to the fluence levels of interest for our target application. Hardness-By-Design (HBD) techniques allowing to eliminating TID-induced leakage currents are also well known and have been extensively used in the past. The radiation tolerance of high-voltage transistors is instead considerably less known, and required a dedicated study.

The available high-voltage transistors included vertical or, more frequently, lateral (LDMOS) transistors rated at drain-source voltages of 14-80 V. These devices are available for integrated circuits whose applications range from automotive to RF, with large use in power management. The response of these high-voltage devices to cumulative radiation effects was systematically studied on samples from five different technologies in the 0.35 to 0.13 µm nodes [9]. Wide variability in TID response was observed. If threshold voltage shifts correlated with the gate voltage ratings of each device, hence with gate oxide thickness, no systematic correlation was instead observed for the source-drain leakage currents in n-channel transistors. The leakage increase seems hence to be determined mainly by details in the construction of the device that are not necessarily linked to voltage ratings or technology node. It is noticeable that significant leakage occurs in all cases starting from a TID above 100 krd(SiO2) in the worst case bias condition. Given the very limited threshold voltage shift observed in all samples at this TID (with possibly only one exception), it is reasonable to expect that commercial off the shelf (COTS) components in these technologies could be suitable for a wide range of applications in Space – at least for cumulative effects. For our application, instead, the TID requirements exceeding the 100Mrad dose exclude the use of technologies with gate oxide thickness above about 7-10nm.

When irradiated with high fluence of particles introducing displacement damage, both vertical and lateral transistors evidence serious electrical degradation. In particular, a large increase of the on-resistance is observed in all devices from a fluence that can vary considerably between technologies, but always above $5 \cdot 10^{14}$ p/cm^2 (hence this is not an issue for typical Space applications). Measurements on LDMOS transistors also reveal a relevant deformation in the output characteristics, probably indicating that defects introduced by displacement damage affect the intimate structure of the device [9][14].

HBD layout techniques inspired from those commonly used in low-voltage transistors were experienced for the first time in n-channel high-voltage devices to increase their resilience against TID effects (leakage currents). In vertical and LDMOS transistors, they successfully extend the natural TID radiation tolerance, eliminating or (in one case) considerably reducing the TID-induced leakage current. These techniques can nevertheless be invasive in LDMOS transistors. Although all HDB transistors perform correctly before irradiation, an Enclosed Layout Transistor (ELT) LDMOS failed systematically to stand high Vds voltage after proton irradiation [9].

In view of the target development of a custom DC-DC converter for the upgraded detectors at the LHC collider, two of the five technologies studied were selected at the end of this study, in September 2009: a 0.25 µm technology, appearing to better satisfy the requirements in terms of both TID (250 Mrd(SiO2)) and displacement damage ($2.5 \cdot 10^{15}$ n/cm^2, 1 MeV neutron equivalent) was selected as the mainstream substrate for the DCDC ASIC. At the same time, a 0.35 µm technology proved to be an excellent backup [14].

Other than the TID and displacement damage effects addressed by this first phase of the study, high voltage transistors might be prone to other radiation effects whose consequences might lead to permanent damage of the transistor: Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR). Testing to assess the devices' sensitivity to these effects requires dedicated test structures, and the availability of a heavy ion beam as radiation source. This makes the test more time consuming and expensive, and for this reason we decided to perform it only after the first selection, and focussing only on the two selected technologies, in 2010 [25]. At that time, the manufacturer of the 0.25 µm technology had decided to introduce a new LDMOS design that replaced the design successfully tested for radiation in 2009, and also TID and displacement damage tests had to be repeated.

The new transistors in this technology proved to be much less radiation tolerant than what had been measured for their older counterparts [25]. Additionally, the test for Single Event Effects revealed that the N-channel LDMOS are very sensitive to SEB – effect that can be induced even at a Vds of 8 V at low Linear Energy Transfer (LET) of the heavy ion used in the test. The PMOS transistors appeared instead to be insensitive up to the maximum LET used in the test, and up to the largest applied Vds of 13 V. These more recent tests disqualified the use of the new transistors in the 0.25 µm technology for the design of our DCDC converter ASIC. We are at present working in collaboration with the manufacturer to explore the full range of radiation effects (TID, displacement damage and SEB-SEGR) on both the older LDMOS design and of alternative designs custom-developed at the foundry to improve the SEB resilience.

At the same time, radiation tests of the 0.35 µm 'backup' technology have been completed, including SEB sensitivity [25]. The devices proved to be very tolerant against SEB, since during heavy ion irradiation up to the maximum LET available (31 MeVcm^{2}mg^{-1}) no event was observed even when the applied Vds was raised to 12 V. These tests were completed at the beginning of September 2010, and as a consequence this technology has become now the streamline semiconductor process for the DCDC ASIC development, and further circuit prototyping will be moved to this technology [25].

3.2. BUCK CONVERTER ASIC

The prototyping of DCDC converter ASICs progressed in 4 steps, each successive prototype integrating more functions and more sophisticated features to improve the electrical performance. The layout of these ASICs is shown in Figure 2. The first 2 prototypes were designed in the 0.35 µm technology in 2008, before the completion of technology selection process described in 3.1. At the time, the radiation performance in terms of TID and displacement damage was known only for the 0.35 µm technology, and was found to be adequate to our target. Two ASIC prototypes were designed, the second of which integrating the full control loop, the bandgap reference voltage generation, and a relatively simple handling of the dead times (this is an important detail determining the overall efficiency of a converter switching at high frequency). This prototype, named AMIS2, still required an off-chip voltage regulator to provide the low-voltage (3.3 V) powering the on-chip control logic and did not include any protection feature (over-current, over-temperature or under-voltage) [4].

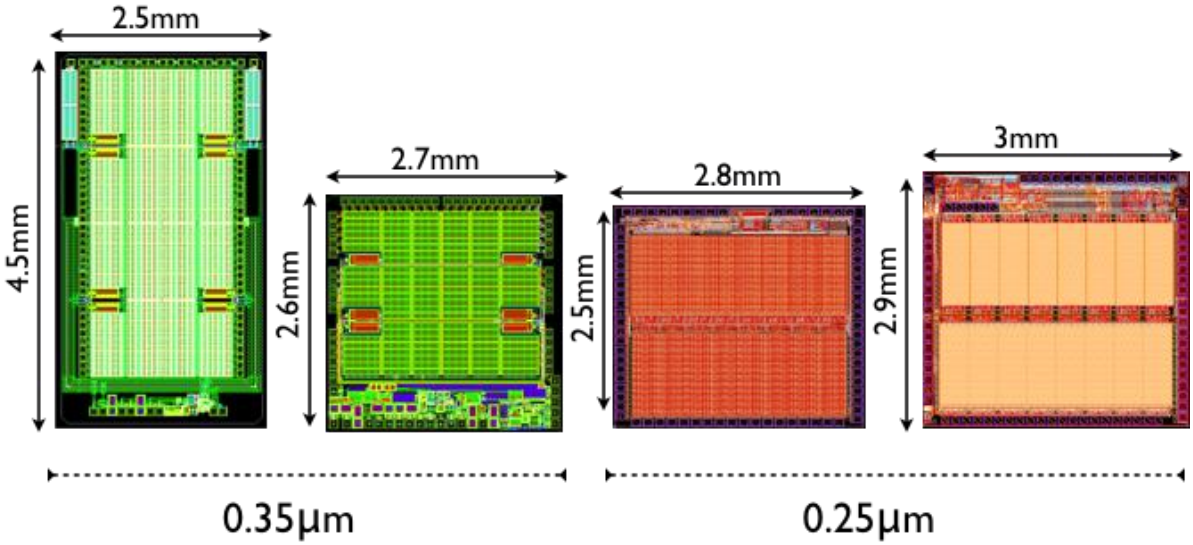

Figure 2: Layout view of the four prototype DCDC converter ASICs in the two technologies used in this work. Chronological order is from left to right.

The performance of the AMIS2 prototype was good, and the converter turned out to be very robust to radiation effects. Efficiency of 75-80% was measured, for samples mounted in QFN32 packages, when an output current of 1 A was provided as a regulated output voltage of 2.5 V from an input voltage of 10 V. TID irradiation at very high dose rate, making a very worst case test for TID effects, decreased the efficiency by a maximum of about 8%. As shown in Figure 3, this happened at a TID of 3 Mrad and correlated well with radiation-induced leakage current in the high-voltage LDMOS transistors used as power switches. In the radiation environment of the real application, with a much lower dose rate, this effect is expected to be much less noticeable.

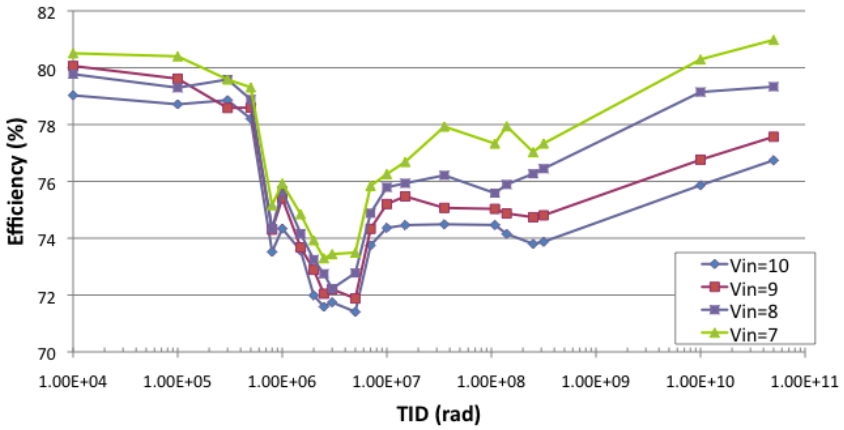

Figure 3: Evolution of the efficiency of the AMIS2 DCDC prototype as a function of the Total Ionizing Dose during X-ray irradiation, for different applied input voltages.

Proton irradiation, aimed at qualifying the resilience against displacement damage, showed very marginal effects in the converter's performance. The efficiency plot versus input voltage of fresh and proton-irradiated samples is shown in Figure 4. These measurements were made up to an accumulated fluence of about $5x10^{15}$ p/cm^2. On top of these tests, heavy ion irradiation was performed to test possible sensitivity to SEB and/or SEGR. During this test, run at the Heavy Ion accelerator of UCL (Louvain-la-Neuve, Belgium), the converter was providing a regulated output voltage of 2.5 V from an input voltage of 6-12 V. The Linear Energy Transfer of the ions was increased up to the maximum of 31 MeVcm^{2}mg^{-1} without observing any disruption to the functionality of the converter. The heavy ion flux was gradually increased during the test to improve the statistical significance of the measurement, and we evaluated that more than 200,000 ions hit the high-voltage transistors embedded in the converter when an input voltage of above 10 V was applied to the two irradiated samples. Figure 5 shows the evaluated number of heavy ion hits to the transistors for all the different conditions explored (input voltage, heavy ion LET).

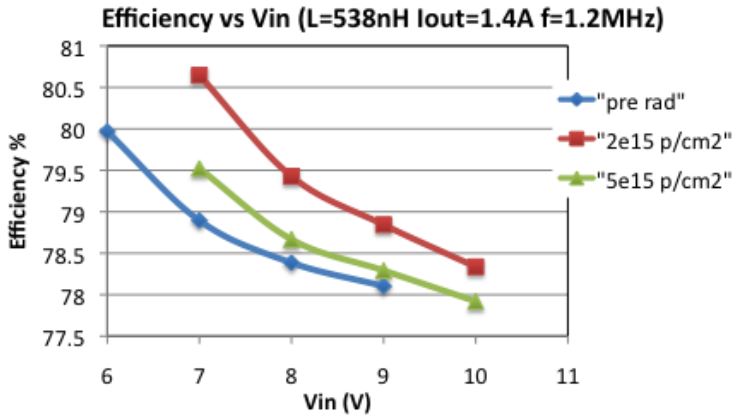

Figure 4: Efficiency of the AMIS2 prototype for fresh or irradiated samples (proton test). The fresh device was mounted in a different package with larger parasitic resistance, hence its efficiency is lower. The comparison indicates that displacement damage does not introduce significant penalty in efficiency.

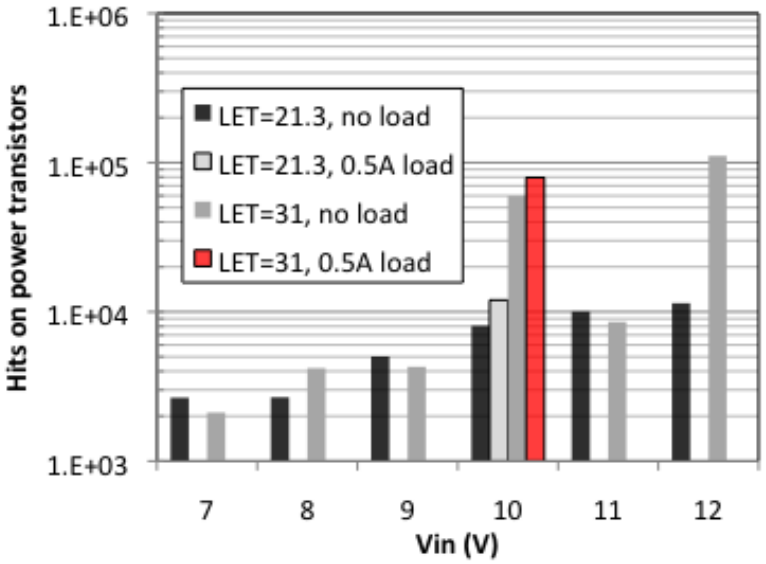

Figure 5: Number of heavy ions hitting the two power transistors of the AMIS2 prototype chip during the Heavy Ion irradiation test

After completion of the technology selection process reported in 3.1, the design activity was shifted to the selected 0.25 µm process [4]. A first converter prototype was developed, which integrated the control loop and a more sophisticated handling of the switching dead times. Also this first prototype in the 0.25 µm technology did not contain specific protection features, neither the required regulators on-chip. Upon delivery, the ASICs were packaged in QFN48 packages and electrically tested with excellent results. All integrated functionalities turned out to work correctly, including the adaptive logic circuitry in charge of a cycle-by-cycle automatic handling of the switching sequence (handling of the dead times). A detailed analysis of the different sources of losses, determining the converter's efficiency, was done. The contributions of conduction, switching, driving and control circuit's losses were disentangled and a predictive model enabling the a-priori estimation of the efficiency in any operational condition was developed (Vin, Vout, Iout, switching frequency, inductance value). This allowed the choice of the appropriate switching conditions, for any set of required input-output voltages and load current, to achieve the highest efficiency. The result of the prediction was very comparable to the measurements, as shown in Figure 6. From an input voltage of 10 V, the converter can achieve an efficiency of about 84% to provide 2 A at 2.5 V at its ouput, an excellent result for a converter using an air-core inductor [4]. The converter was also capable of a larger conversion ratio with good efficiency, since we measured a 69% efficiency for an output voltage of 0.9 V from the 10 V input.

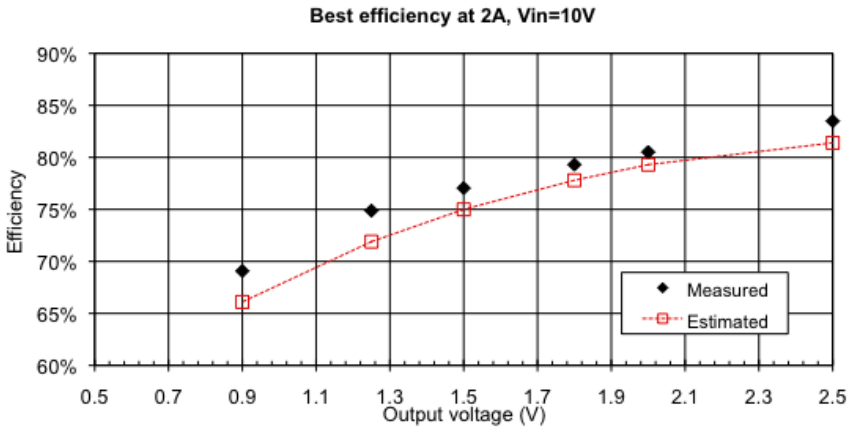

Figure 6: Predicted and measured efficiency of the first prototype converter in the 0.25 µm technology.

After the excellent results of this first converter, a second and more sophisticated design was completed in the same technology. At that time, the technology provider had decided to introduce 'new' LDMOS transistors with a different design increasing their electrical performance (in particular tailored for RF applications). These transistors had not been tested for radiation effects before, but it was not possible to avoid their use in the new prototype (the 'old' tested transistors were not available in an MPW run, which is the normal type of runs used for prototyping – via the Europractice IC services). Another type of LDMOS not used in the first prototype was also needed, namely the isolated N-channel LDMOS. This second prototype included improvements in the handling of the dead times, full on-chip generation of all the necessary voltages, and an over-current protection circuit. A first set of measurements on the manufactured prototypes confirmed the good design choices for the dead time handling, and the converter had an improved efficiency with respect to the first design. Figure 7 shows the efficiency of this new prototype for different combinations of inductances and switching frequency. A noticeable improvement in the efficiency has been observed by comparison with data for the first prototype, especially at small inductor values. Unfortunately, all tested samples failed destructively after a short while, in particular when the output current or input voltage was changed during operation. After a long series of studies, it was possible to trace the origin of the failures to the activation of a latch-up path in the circuit [25]. This is a real risk in synchronous DCDC converters, where (by default) a parasitic diode in the substrate gets forward biased at every switching cycle. This diode acts as a forward-biased emitter-base junction of a parasitic bipolar NPN transistor, injecting current to neighbouring n-type diffusion. This current injection is heavily dependent on the technology: architecture of the LDMOS transistor, resistivity of the substrate and of the wells, etc. Moreover, the circuit layout can have a strong influence on the collected current. If the current injection is sufficiently large, and in the absence of very efficient well contacts in the diffusion region, a parasitic PNP transistor might turn on. The combination of the two parasitic NPN and PNP transistors gives origin to a thyristor structure that maintains the current between the input voltage and ground. Given the size of the parasitic transistors, this current is very large (several Amperes) and can easily destroy the circuit – the evidence of failure can be seen by visual inspection at the microscope, often as fused metal lines. It should be noted that these failures were not observed for the first prototype, which used very similar layout for the main power parts, indicating that the introduction of the 'new' LDMOS transistors can contribute in a relevant manner to the appearance of the latch-up.

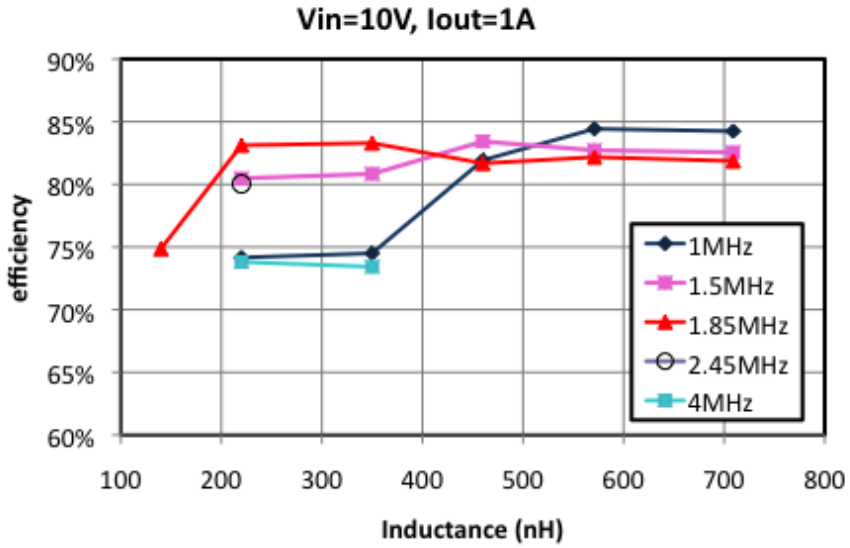

Figure 7: Efficiency of the second prototype converter in the 0.25 µm technology in different conditions (switching frequency and inductor value).

As reported in section 3.1, the 'new' transistors were considerably more damaged by displacement damage. Irradiation of 5 samples of the second converter prototype with a proton source confirmed that weakness, since none of the samples was operational after irradiation (even after the smallest fluence of 10^{15} p/cm^2).

After the complete characterization of both prototype DCDC converters and of individual transistors in the 0.25 µm technology, we concluded that the 'new' LDMOS design adopted by the manufacturer is not adequate for our application [25]. Radiation resistance to displacement damage and SEB was not sufficient, and the current injection in the substrate could induce destructive electrical latch-up (this latter effect can be attenuated or even removed by appropriate layout mitigation techniques, that have to be carefully evaluated since their efficiency is technology dependent). The technology provider is now aware of that, and we are collaborating in view of characterizing fully the 'old' transistors' design, including SEB sensitivity, as well as new LDMOS designs specifically developed by the foundry to increase SEB resilience. In the meanwhile, the successful full characterization of the 0.35 µm technology that was selected as backup indicates a safe path to produce in a short time a DCDC converter ASIC satisfying all our requirements. Therefore, we have just started the design of a full converter in this technology, including all protection features and sophisticated dead time handling [25].

4. SWITCHED CAPACITOR CONVERTER

An essential component of the powering scheme based on DC-DC power conversion on the detector modules is a switched capacitor converter to be implemented in the front-end chips [1]. A prototype circuit has been developed in the same 130 nm CMOS technology as the prototype front-end chip [5][28]. A simplified circuit diagram is shown in Figure 8. The core of the circuit consists of four switching transistors and two capacitors. Given the requirements for the output power the capacitors have to be in the range of hundreds of nF and so have to be implemented as external SMD components with low effective series resistance. Given the progress in miniaturisation of the SMD components the external capacitors can be accommodated on the front-end hybrids without affecting significantly the material budget.

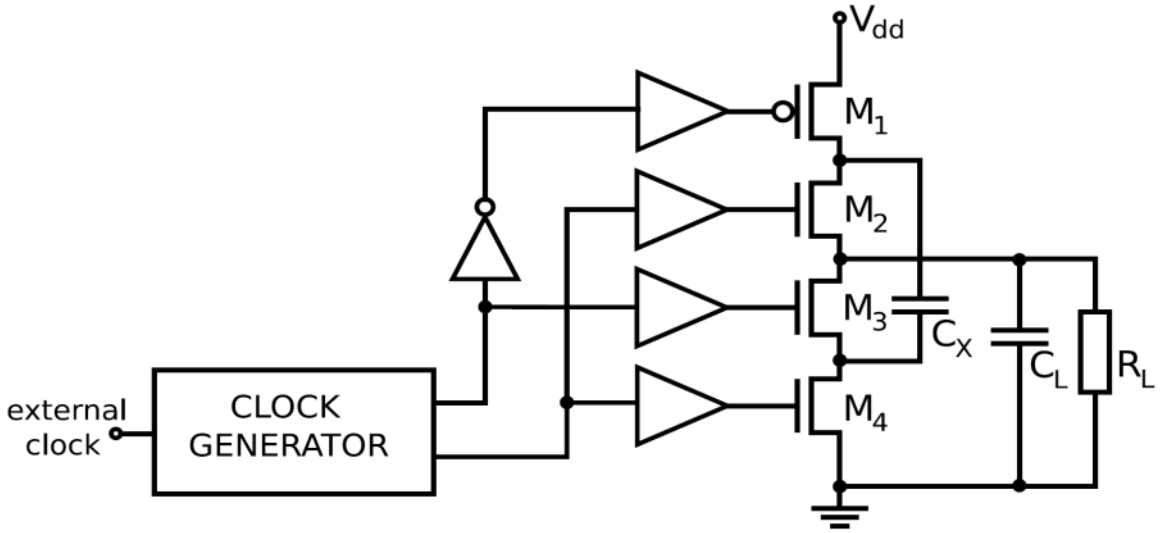

Figure 8: Schematic diagram of the switched capacitor DC-DC step-down converter.

The parameters driving optimisation of this circuit are: power conversion efficiency, output resistance and amplitude of output voltage ripples, which all depend strongly on the output current. Thus, the design should be customised for the given output current. The demonstrator chip has been designed assuming a nominal output current of 40 mA, input voltage of 1.9 V, and output voltage of 0.9 V. A power conversion efficiency of 97 % has been achieved for external capacitors C_X = 1000 nF, C_L = 200 nF and clock frequency of 1 MHz.

The mask layout of the demonstrator circuit is shown in Figure 9. One can notice that the area of this block is dominated by the four transistors working as switches, which have to be large in order to minimise their resistances as they are the main source of power loses. Nevertheless, the total area of the block is below 0.12 mm^2 and it is perfectly feasible to implement one or two of such blocks on the front-end chip.

The expected performance of the design is illustrated in Figure 10, which shows two fundamental characteristics of this circuit.

The design has been submitted for manufacturing in May 2010, and prototype chips are expected by early October 2010 [28].

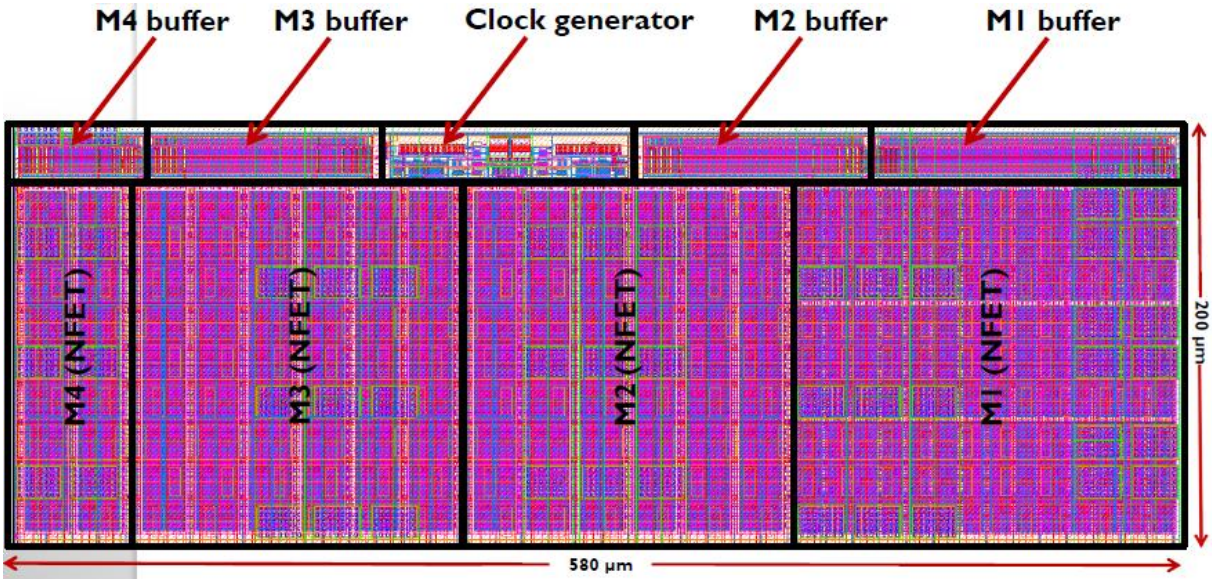

Figure 9: Mask layout of the demonstrator switched capacitor step-down converter.

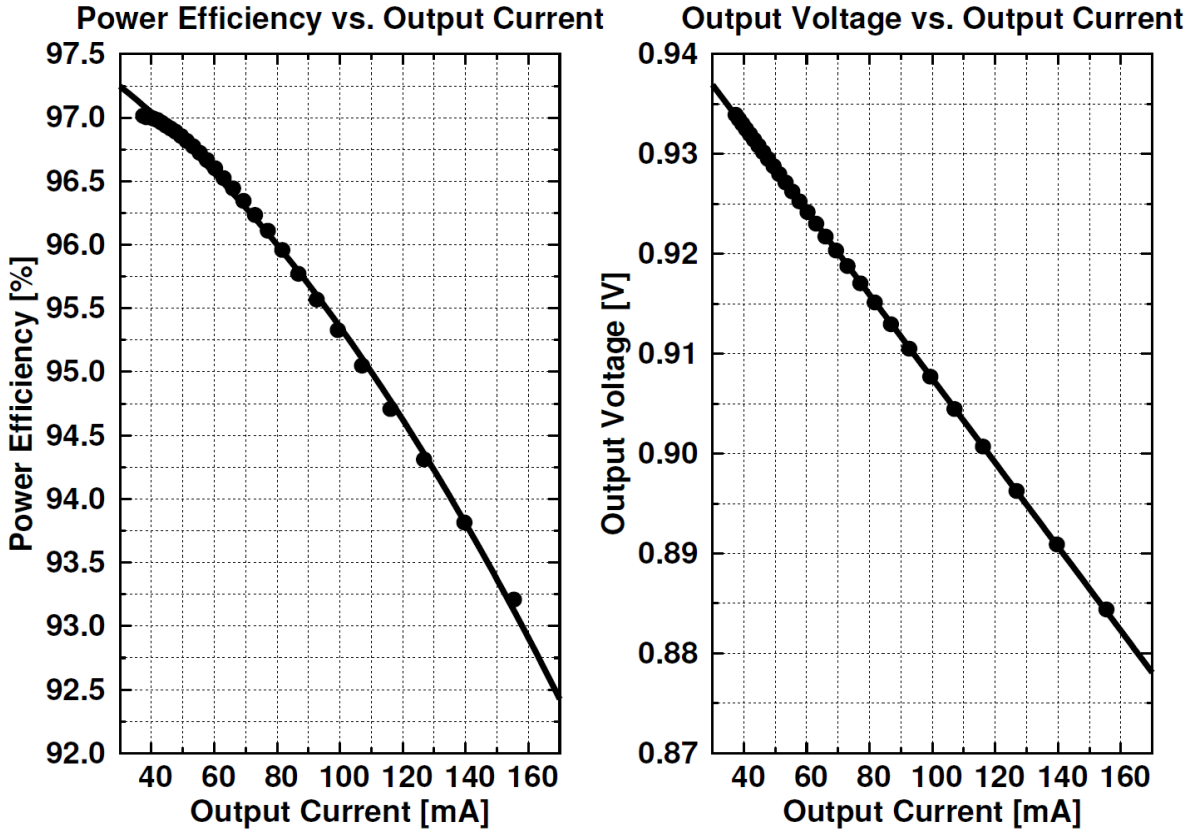

Figure 10: Simulated characteristics of the demonstrator design: power efficiency vs. output current and output voltage vs. output current. The expected output resistance of the circuit is about 0.4 Ω.

5. BUCK CONVERTER PROTOTYPES

5.1. CONVERTER PROTOTYPES AND OPTIMIZATION

5.1.1. Buck converter topology.

Different DC to DC conversion technologies applicable to the trackers at sLHC have been studied in detail during the first year of activity. In particular, the impossibility of using ferromagnetic materials for the inductors in the large magnetic field in SLHC experiments, together with the low-volume and low-mass requirements for the converter, imposed strict boundaries to the usable technologies. The Buck converter (Figure 11) topology was selected because of its low parts count, with the possibility to integrate most of it in an ASIC, excepting the main coil. This topology offers efficiencies above 80% that are acceptable for the intended application [1].

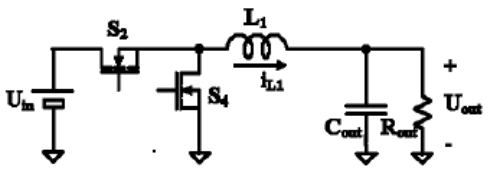

Figure 1: Topology of the buck converter

Figure 11: Buck converter topology.

5.1.2. Noise characterization.

The DCDC converters will be used to power front end systems very sensitive to electronic noise. System tests performed by CERN with ATLAS tracker modules and by the RWTH Aachen University with the CMS Tracker Endcap petals have very soon put in evidence their susceptibility to conducted noise, and to radiated magnetic and electric fields [3]. The mitigation of the noise emissions became then a critical aspect of the project. The test stations (Figure 12) and methods developed during the first year of the project for the characterization of the functional and electromagnetic compatibility properties of the converters enabled the comparison between different prototypes. These methods were adopted by the labs involved in the development of boards, and test stations were replicated.

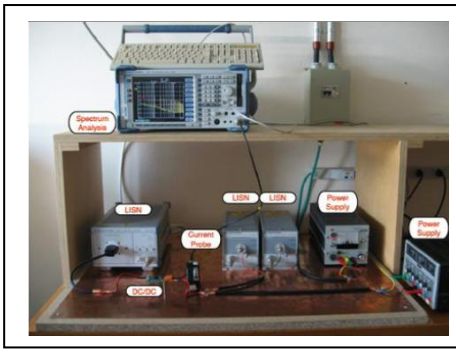

Figure 12: Characterization test stand.

5.1.3. Prototypes and noise optimization.

The development of generic converter prototypes was carried out at CERN and at the RWTH Aachen University aiming at the following objectives:

- To get expertise in the design and layout of buck converters using commercially available buck controller chips.
- To understand the way that electromagnetic noise gets generated at the board level and how to mitigate it.
- To evaluate the front-end systems susceptibility to the noise emitted by the converters.
- To work out the packaging of the power ASIC and its optimized integration on DC to DC boards.

Several boards were designed with significant improvements for every new design (Table 1). The first prototypes developed at CERN used an Intersil ISL6540A power controller that required many passive components and external power transistors on the board (Figure 13). The device was operated at 1 MHz of switching frequency and its noise properties were significantly reduced from 60 dB down to 25 dB by first improving the layout and afterwards by adding specific input and output filters. The noise improvement was linked to the board size reduction too, but limited anyway because of the quantity of external components needed that constituted many noise spots on the board.

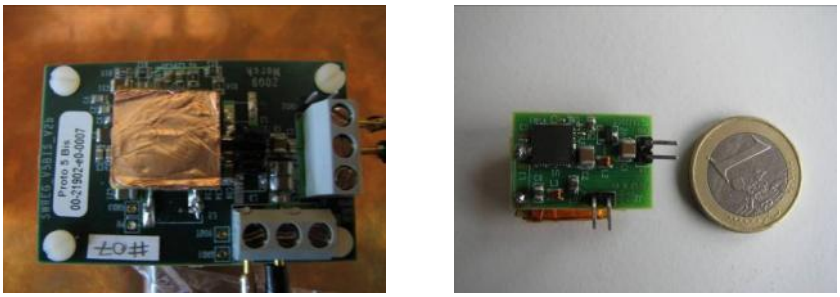

Figure 13: Proto5 with shielded PCB inductor (left) and AMIS2V1 with PCB coil at bottom (right)

Once the first functional radiation tolerant AMIS2 ASIC got delivered [4], a prototype board was designed for it (Figure 13). The AMIS2 ASIC includes the power transistors and requires a reduced amount of passive components. Packaged in a QFN48 plastic case, a maximum common mode noise current of 20 dB was obtained, which is comparable to the level achieved with the last ISL6540A based prototype. System tests revealed however some susceptibility to radiated noise from the converter, and this motivated further studies in noise mitigation that are described later on in this report [27]. With this new level of optimization and understanding, a new prototype using the same AMIS2 ASIC but in a more compact QFN32 package was produced, namely the AMIS2 EMC prototype [27]. Apart of implementing optimized placement topologies and layouts, it included a shield case for the first time (Figure 14). The level of noise achieved is outstanding at -5dBµA, a level never observed so far in any converter tested at CERN (Table 1). System tests using this new prototype showed a good level of compatibility with front-end systems even in worst case

conditions of placement. The AMIS2 EMC prototype confirms the viability of the proposed powering scheme for noise sensitive front-end systems to be used at the sLHC.

Figure 14: AMIS2 DC/DC converter prototypes with 500 nH coil (left) and with shield (right).

Table 1: Noise properties of CERN DC/DC converter prototypes

	Prototype	Designed at	Controller	CM noise estimation
1	Proto 2	CERN	ISL6540A	60 dBµA at 1MHz
2	Proto 3	CERN	ISL6540A	50 dBµA at 1MHz
3	Proto 5	CERN	ISL6540A	25 dBµA at 1MHz
4	AMIS2 V3	CERN	AMIS2	20 dBµA at 1.5 MHz
5	AMIS2 EMC	CERN	AMIS2	-5 dBµA at 6 MHz
6	SM01B	CERN	LT3605	15 dBµA at 4 MHz

At RWTH Aachen University several buck converter prototype boards, both with commercial and custom ASICs (AMIS1 & AMIS2), have been developed. The first boards used the Enpirion EQ5382D chip with a switching frequency of 4MHz, a maximal input voltage of 5.5V and a maximal output current of 1A. These boards were used in system tests with CMS silicon strip modules, where in particular different filtering options were explored. It was shown that the Differential Mode noise at the converter's output can be reduced drastically with the usage of pi-filters at the output of the converter (Figure 15) [18].

Later, once the AMIS prototype ASICs were available, converters with these chips were developed, studied in system tests and optimized. These two-layer boards allow for an input voltage of 12V and an output current of 3A and operate at a switching frequency of 1MHz. They are equipped with a custom compact air-core toroid (500nH inductance), whose geometry has been optimized with analytical calculations, pi-filters at the input and output, and a cooling contact (Figure 16) [19]. Based on measurements of the noise spectra and on results from the system tests and taking into account the experience from the converter development performed at CERN the board layout was further optimized, which resulted in a significant improvement of the Differential Mode noise at the converter's output (Figure 17).

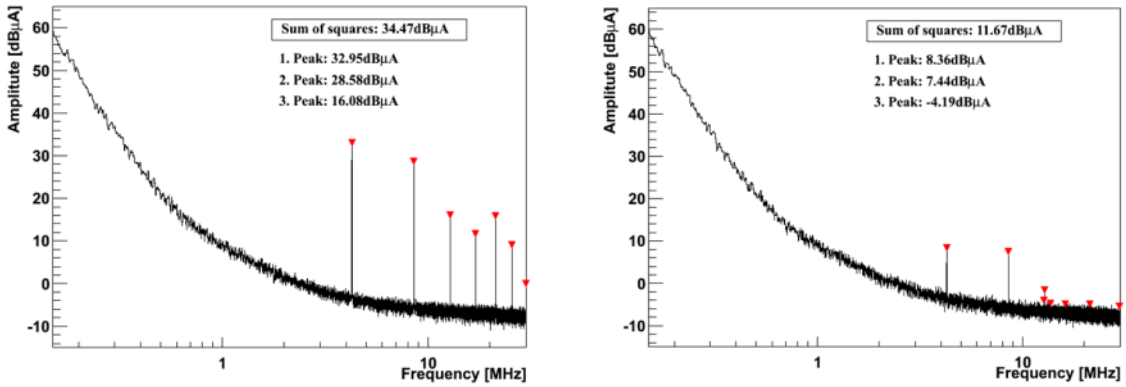

Figure 15: Measured Differential Mode output noise spectra of the buck converter prototypes with a commercial chip, developed at RWTH Aachen University. The right picture shows the drastic reduction of the Differential Mode output noise due to the usage of an additional optimized pi-filter.

Figure 16: Buck converter prototypes from RWTH Aachen University, all equipped with the AMIS2 ASIC. The optimized board is on the very right.

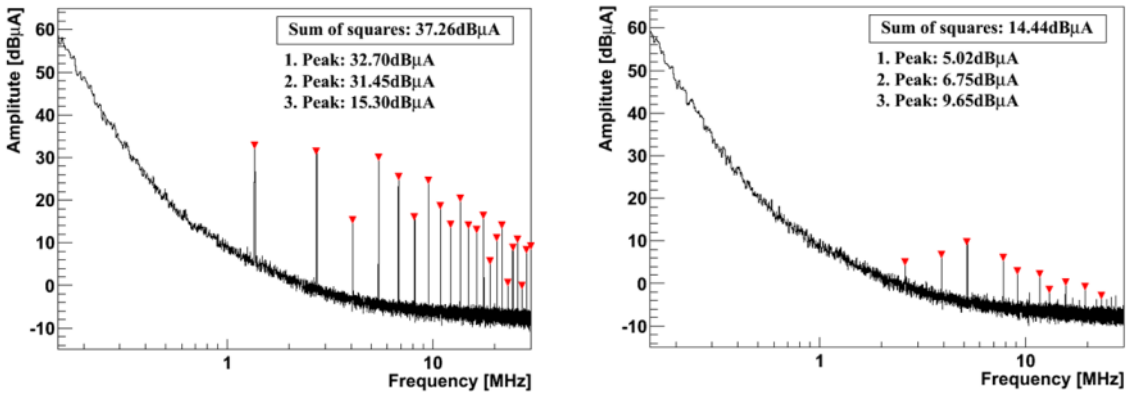

Figure 17: Measured Differential Mode output noise spectra of two buck converter prototypes developed at RWTH Aachen University. Both are equipped with the AMIS2 ASIC. The left picture shows the first design, the right picture the optimized layout. Both measurements have been performed without any shield.

The mechanisms at the origin of the emission of noise at board level have been systematically investigated at CERN and allowed achieving the low noise properties of the AMIS2 EMC prototype [27]. The optimization required an accurate insight in the electromagnetic couplings within the converter that is closely linked to parasitic effects induced by the choice of passive components and the board layout.

Initially Pspice and Matlab simulation model that included the main parasitic parameters of passive devices allowed putting in evidence the importance of selecting capacitors with low series inductance and resistance. The obtained model was validated with the converter Proto5 on the test stands for frequencies up to 10 MHz approximately. Beyond that frequency unidentified effects were becoming dominant.

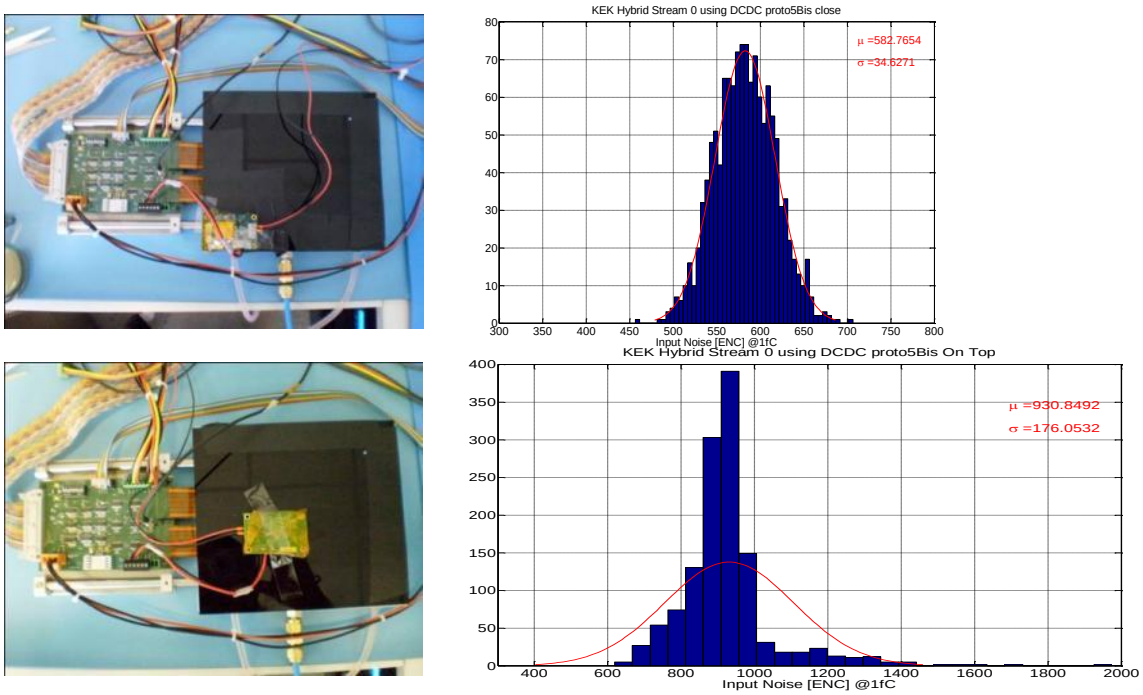

Figure 18: System tests using Proto5 on the University of Geneva prototype front-end module showing low susceptibility to conducted noise (top) and high susceptibility to radiated fields (bottom).

System tests carried out on an ATLAS tracker module with Proto5 modules at the University of Liverpool and on modules of the University of Geneva revealed the strong sensitivity to radiated electric and magnetic fields using Proto5 in close vicinity of the front-end ASICs (Figure 18). The addition of a shield allowed improving significantly the system performance. The shield case must be designed in a way that minimizes the material budget without compromising its shielding effectiveness. Molded plastic cases are under development now, and copper deposition on their surface will be exercised with different thicknesses in 2011.

Looking for a further reduction of the radiated noise, the board layout model has been pushed one step further, aiming to identify secondary mechanisms that originate the emission of fields. For this purpose, inductive coupling effects that take place locally within the converter have been added to the first simulation model. The mutual inductance between

passive components and traces at board level and stray capacitance parameters have been extracted using electromagnetic simulation tools such as Ansoft Q3D and FastHenry. By means of parametric simulations using Ansoft Simplorer, the passive components and the couplings that dominate the contribution to the conducted and radiated noise were identified. The electromagnetic coupling properties of specific placement topologies have been analyzed in this way for components and traces identified to be critical, and electrical simulation models have been obtained. The optimized placement topologies (Figure 20) have been implemented in the AMIS2 EMC prototype boards that showed an outstanding low level of conducted noise that in turn resulted in a significant reduction of the radiated noise too. Adding a shield case on top of this (Figure 21) resulted at the end in negligible radiated electric and magnetic fields, and a reduction of the conducted noise down to -5 dBµA (Figure 19). The size of this converter was significantly reduced with respect to Proto5, down to 26 mm X 13.5mm.

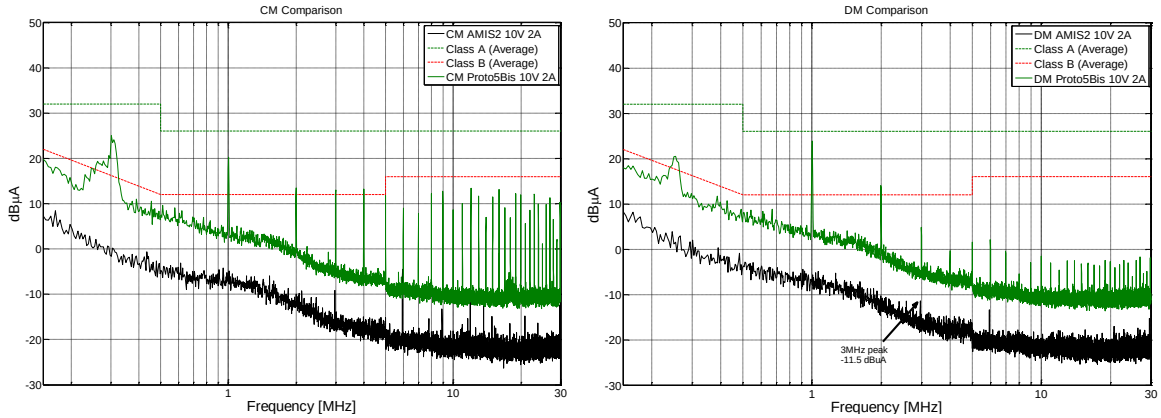

Figure 19: Common Mode (left) and Differential Mode (right) emissions of the AMIS2_EMC prototype (in black) compared to those of Proto5 (in green).

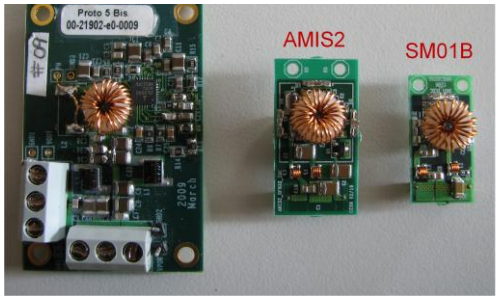

Figure 20: DCDC converter prototypes developed at CERN, Proto5 (left), AMIS2_EMC (center) and SM01B (right).

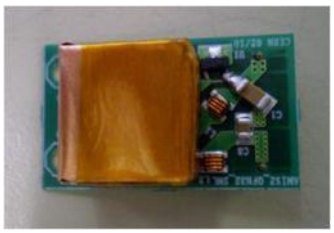

Figure 21: AMIS2_SML prototype converter with shield.

The AMIS2 DC to DC ASIC is designed to power front-end chips made on a 130 nm technology, with reduced power consumption. However, most of the systems currently available for tests lack of the targeted version of front-end ASICs, and this result in a current consumption beyond what the AMIS chip can deliver. To enable the tests on these systems, a DC to DC module has been designed using the LT3605 buck controller: this commercially available device offers a topology very similar to the one of AMIS2, excepting the bootstrap circuitry that remains external and imposes a multilayer layout opposed to the double sided layout of the AMIS2 converter. This module, identified as SM01B (Figure 20), delivers 2.5V with an output current up to 5A; it is slightly more compact than the AMIS2 EMC, but is pin to pin compatible with it. This board is not noise optimized as the AMIS2 EMC board, resulting in larger conducted noise (Figure 22) and radiated fields (Figure 23). However the addition of the shield brings theses fields to levels that are similar to those measured with AMIS2. The SM01B can then be used as a direct replacement of the AMIS2-EMC board for systems requiring large currents.

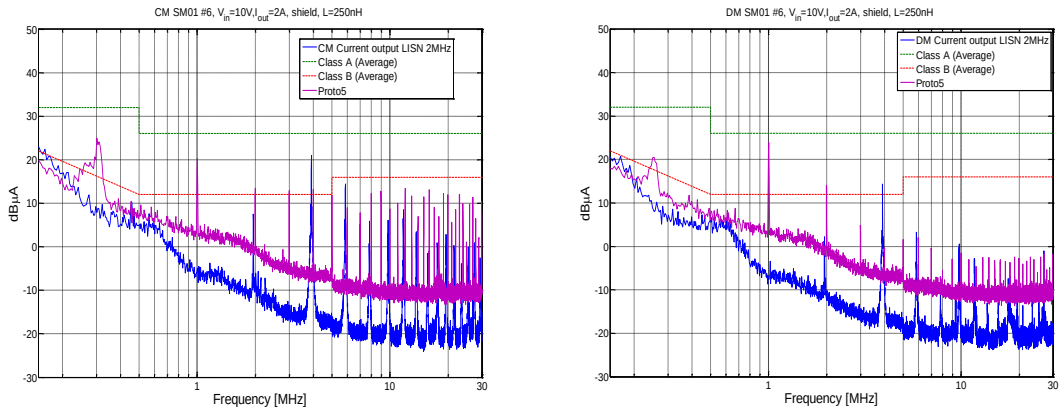

Figure 22: Common Mode (left) and Differential Mode (right) emissions of the SM01B prototype (in blue) compared to those of Proto5 (in pink).

Both the AMIS2 and SM01B converter boards are designed specifically to enable their integration onto the front-end systems of the ATLAS upgraded tracker, and are referred to as “plug-in-boards” (PIB). The implemented PIB format and pin assignment will enable the tests on the systems that will have been specially designed to receive them.

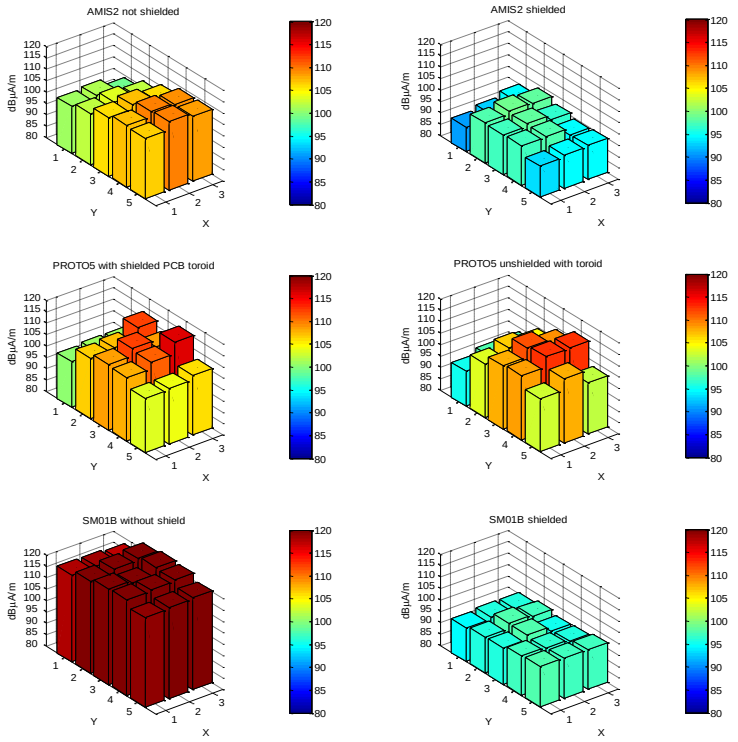

Figure 23: radiated fields measured on AMIS2_EMC (top), Proto5 (center) and SM01B (bottom) in their unshielded (left) and shielded (right) configurations.

5.2. AIR CORE INDUCTORS

The buck converter topology requires a low mass, low resistance air core power inductor to deliver a DC output voltage. Solenoid, wrapped toroid and custom PCB toroid structures were evaluated at CERN and at the RWTH Aachen University (Figure 24).

Figure 24: Solenoid, hand wrapped and PCB toroid inductors.

Electromagnetic simulations and measurements showed that the toroidal topology allows containing the emission of magnetic field significantly, compared with the solenoidal topology (Figure 25). Prototypes of a PCB based toroid were produced at CERN [10]. The difficulty to build reliable copper filled vias forced us to discard this topology, in favor of the more classic wrapped toroid inductor. Different handmade wrapped toroidal coils were produced and tested at CERN and at RWTH Aachen University. They were used for the assembly of the DCDC prototype boards.

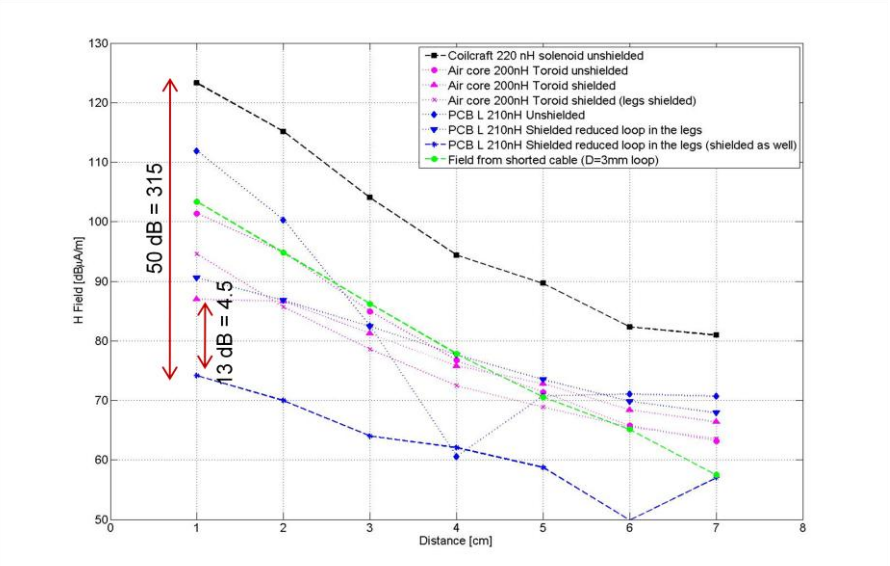

Figure 25: radiated magnetic field of different coil topologies as function of the distance.

At RWTH Aachen University a scanning table set-up equipped with a magnetic field probe is used to measure the magnetic emission of various air-core inductors along the three axes (Figure 26). These measurements are accompanied by Finite Element simulations using the Comsol Multiphysics package, which lead to a detailed understanding of the shape of the emitted field and its dependency on manufacturing details.

Both methods as well as analytic calculations are exploited to optimize the coil design. In Figure 27 the measured z-component of the magnetic field in the xy-plane in a distance of 1.5mm from the top of the inductor is shown for various prototype inductors. All coils have approximately the same inductance (500nH). The latest optimized toroid has a much more compact magnetic field together with a reduced DC resistance (38mOhm compared to 80mOhm for the so-called “Mini Toroid”), which leads to an improvement in power efficiency of the order of 5%.

The scanning table set-up shown on the left of Figure 26 was further used to study the coupling of magnetic near-field emissions into silicon strip modules. For this purpose the set-up was equipped with a tiny coil that was operated from a sinus wave generator with a frequency typical for DC-DC converters (1MHz). This probe was moved across a silicon strip module of the CMS Tracker End Caps and the module’s noise was recorded as a function of the coil position. The measurement (Figure 28) shows clearly that the z-component of the magnetic field couples into the pitch adapter region of the module, which enables a current loop that is closed via capacitive coupling between silicon strips and the sensor backplane. Such results are very valuable to optimize the future module design in a way that minimizes the vulnerability to magnetic emissions.

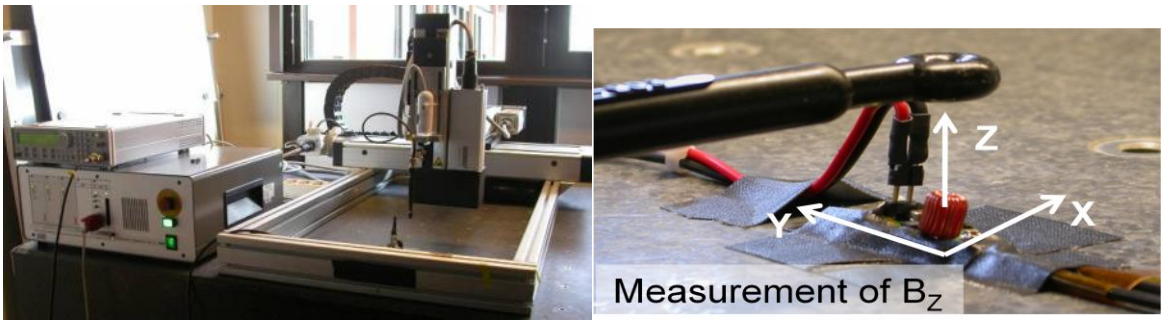

Figure 26: Scanning table set-up at RWTH Aachen used to characterize the magnetic emissions of air-core inductors.

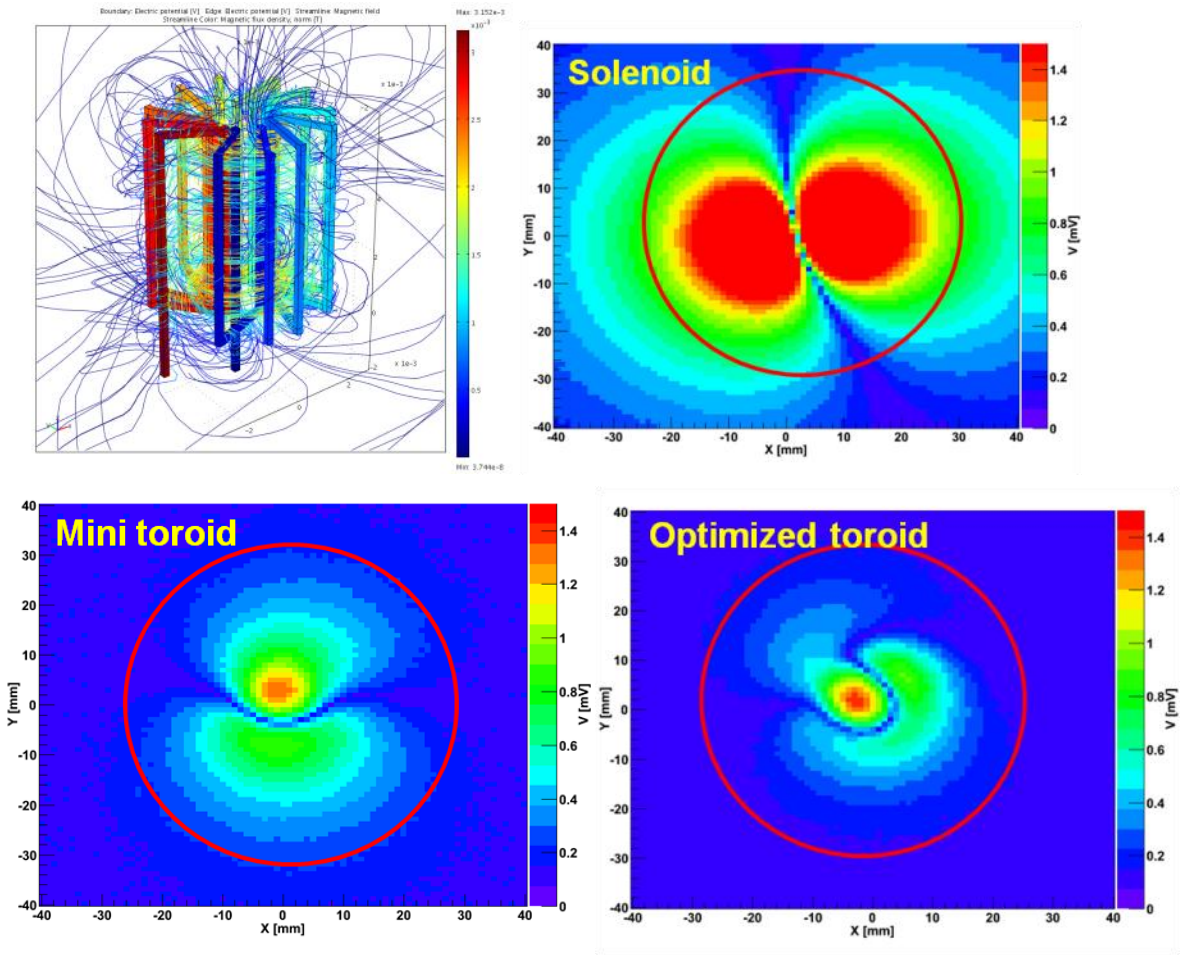

Figure 27: Simulation (top left) and three measurements of magnetic emissions of air-core toroids. The measurements illustrate the evolution from a commercial solenoid to an optimized custom-made air-core toroid, with much reduced magnetic emissions.

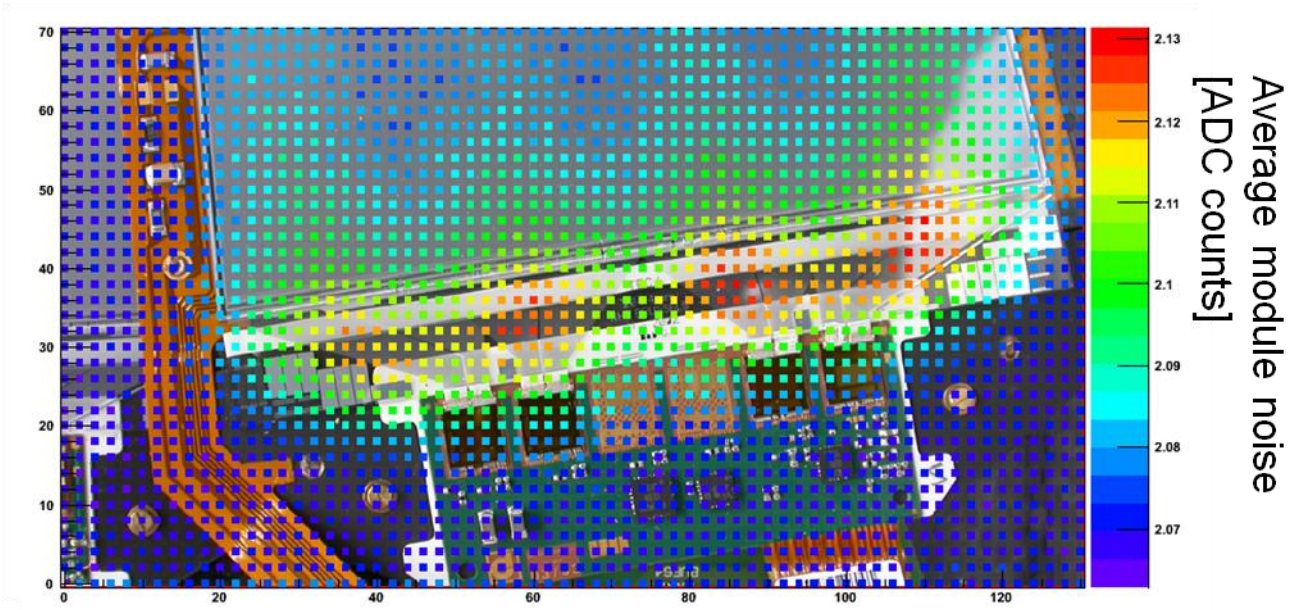

Figure 28: Overlay of a photograph of a CMS Tracker End Cap module and the noise recorded when a magnetic probe was positioned above the module. Each square shows the average module noise colour-coded for the case when the magnetic emitter was on the position of the square. The red regions, above the pitch adapter, correspond to the regions with the largest coupling.

The manufacturability of these coils is an important issue to enable the mass production of converters. Industrial solutions have been explored by CERN and finally a custom coil was produced in collaboration with Coilcraft (Figure 29), obtaining an inductance value of 200 nH and a series resistance of 30 mΩ in DC, parameters that match very well the optimized buck converter design. The coil is fit with a miniature plastic standoff that will allow the placement of the coil straight on top of the power ASIC.

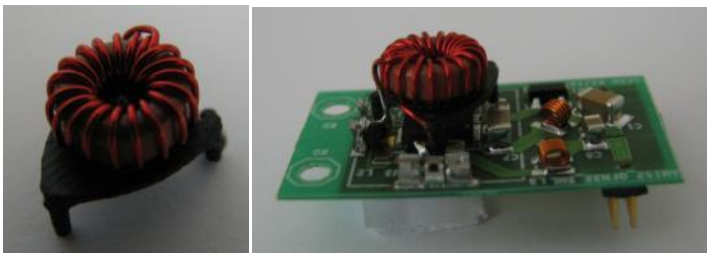

Figure 29: Custom made inductor as designed and produced by Coilcraft (left), mounted on an AMIS2_SML board (right).

5.3. SHIELDING

The strong susceptibility of front-end systems to electric fields was put in evidence through system tests made with the early Proto5 converter. Despite the significant improvement in terms of noise mitigation by proper layout, the radiated fields can't be fully cancelled. The addition of a shield enclosing the noise emitting parts and board areas was found to be a very effective way to enable the placement of the converters in the close vicinity of the sensitive front-end circuits.

Initially, shielding cases have been manually assembled using a 200 µm thick copper foil [27], which was the thinnest foil easily available. In order to limit the material budget introduced by the shielding material in the detector volume, plastic based cases have been developed, and the coating of copper onto them is currently being evaluated. This method will allow the implementation of copper shield layers ranging between 10 µm and 100 µm on low mass rigid structures: the required copper thickness will be determined through electromagnetic measurements and system tests.

Alternative designs are going to be evaluated too, such as micro machined copper structures that might allow getting rid of the plastic support on which it is difficult to apply the copper coating.

6. SYSTEM TESTS

The DCDC prototype boards were used to power different front-end systems, to explore the coupling mechanisms and the susceptibility figures. In 2009, the noise susceptibility of the ATLAS short strips tracker prototype was studied at many occasions, first using DCDC prototypes, and later on using near field antennas [3][27]. This system was found to be sensitive to electric and magnetic fields, while conducted noise had negligible impact, justifying the need of small shield box on top of the DCDC converter board. Similar tests were carried out on the CMS Tracker Endcap petals putting in evidence different noise susceptibility properties [11]. The system tests confirmed the need for a careful integration of the DCDC ASICs onto a DCDC board optimized in terms of board layout, selection and placement of passives and with adequate shielding.

6.1. SYSTEM TESTS ON THE CMS TRACKER END CAP MODULES

The noise effects of DC-DC buck converters on silicon strip modules of the CMS Tracker End Caps have been studied extensively at RWTH Aachen University. For this purpose both buck converters with commercial chips as well as converters based on the AMIS2 ASIC have been developed at Aachen. The silicon strip modules were powered via those DC-DC converters and the effects of conductive and radiated noise emissions as well as various shielding and filtering options were explored.

Commercial converters based on the Enpirion EQ5382D buck converter chip were used to optimize the filtering such that the noise effect of these converters on the silicon modules was negligible.

Measurements with buck converter prototype boards based on the AMIS2 ASIC resulted in the same low module noise when the boards were operated with the same parameters than the commercial boards in terms of switching frequency, input voltage and filtering (Figure 30). However, the noise increased when the AMIS2 boards were operated at their design switching frequency and with a larger input voltage, as required by the foreseen application within CMS [15]. Due to this result the board layout, filter design and coil position were studied and optimized, leading to a much improved AMIS2 prototype board, whose evaluation is still ongoing.

A set-up with CMS pixel modules is currently under preparation at RWTH Aachen University. It will allow for the evaluation of the noise effects of DC-DC converters on the PSI46 readout chip, which will be used (with minor modifications) in the upgrade of the CMS pixel detector, for which the usage of DC-DC buck converters is foreseen.

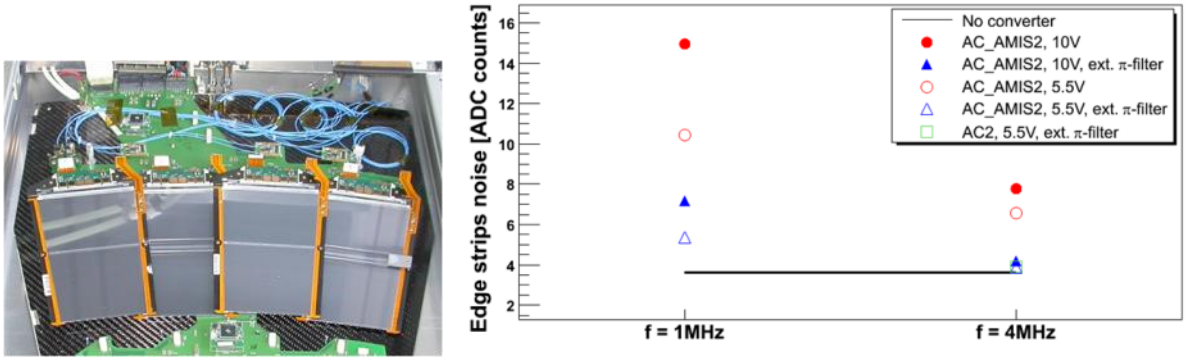

Figure 30: CMS system test set-up with silicon strip modules (left) and measurements of the module's edge strip noise (right) for conventional powering (black line) and when powered with a commercial converter (AC2) or with the AMIS2 converter board (AC_AMIS2), for various conditions.

6.2. SYSTEM TESTS ON THE ATLAS TRACKER MODULES.

Two ATLAS tracker front-end systems (from the University of Liverpool and from the University of Geneva, respectively) have been used to evaluate their compatibility with the DC to DC converters produced. Although both are using the same ABCN front-end ASICs in 0.25 µm technology [6][7][8], their assembly onto hybrids, modules and detectors follow different technical implementations. Each hybrid hosts 20 ASICs arranged in two rows, each ASIC handling 128 strip channels. The input signals are amplified and discriminated to deliver a binary output for every channel. The noise properties of the channels are obtained with the measurement of the output efficiency when varying the discriminating threshold, obtaining a typical error function curve so called S-Curve. Each curve is fitted and its slope is representative of the noise of that channel.

The setup at Liverpool was initially used to explore the compatibility with the Proto5 converter. Although it appeared to be insensitive the common mode and differential mode currents emitted by the converter, the front-end noise increased very significantly once the converter got placed very close to it. Two effects were then observed (Figure 31):

- The noise of all the channels was globally increased very significantly.
- Odd channels close to the converter were developing larger noise than even channels.

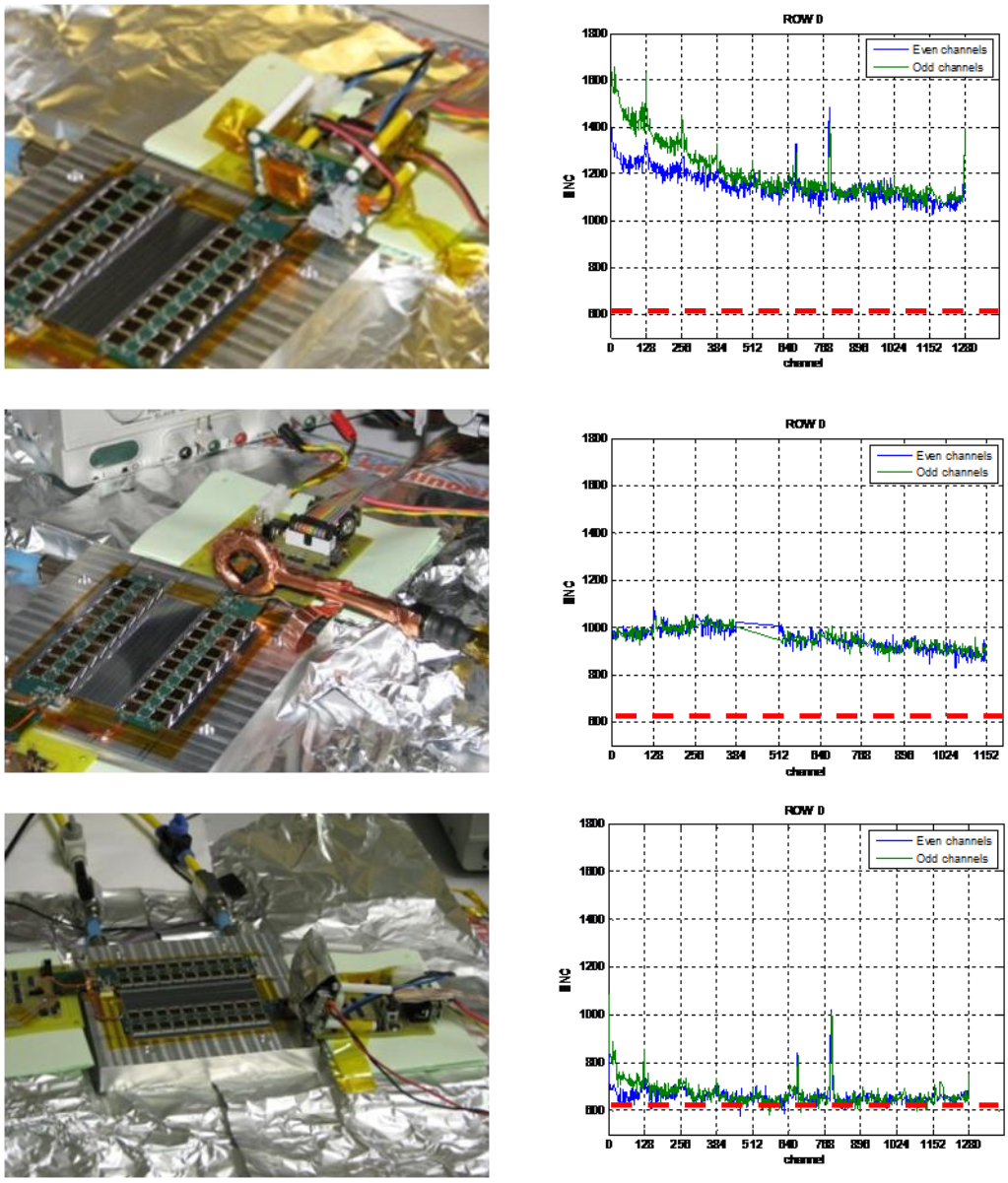

Figure 31: Susceptibility of the Liverpool front-end system against noise radiated by the converter (top), against magnetic field only (center) and using a shielded converter (bottom).

The global increase of the noise level for all channels independently of their distance to the converter is attributed to magnetic field coupling in the hybrid board. This was later on put in evidence using a near field magnetic loop probe radiating towards the system, with all channels increasing their noise uniformly. The mismatch between odd and even channels is attributed to electric field coupling between the converter and the bonding wires that tie the strips to the ASIC inputs: these bonds are arranged in a double layer stack, those placed above being exposed to the electric field coupling, and those sitting under being shielded by them. Wrapping the converter with a tinned copper foil helped to bring the noise down to the reference level.

To improve the compatibility between the converters and the front-end systems, the radiated noise had to be significantly reduced as already explained in section 5. This was achieved with the AMIS2-EMC and with the SM01B plug-in-boards, including the shields, and verified in the laboratory test stands. The AMIS2-EMC converter was evaluated also with the University of Geneva system (Figure 32): this system used separated power inputs for analog and digital circuitry, splitting the currents in 1A and 3A respectively, each being powered with one converter. Although the AMIS2-EMC board targets a nominal current of 2A, it was successfully used up to 3A enabling the test on that system. Placing the two converters straight on top of the front-end ASICs being characterized for this test, facing down to maximize the coupling, a noise increase of only 10% was observed, corresponding to a very significant improvement with respect to Proto5. This noise increase is comparable with the expected noise increase attributed to radiation damage in the detector and front-end ASICs, and is therefore acceptable.

Later on the University of Geneva developed a new prototype based on two modules instead of one, which uses a common input power for both analog and digital sections of the system and it therefore requires more than 4A at its input. The analog voltage is produced within the ABCN ASICs using an embedded linear regulator. The large current required imposed the use of the SM01B board instead of the AMIS2-EMC board. Having only one converter and the front end regulator enabled, placing the converter facing down to the ASICs a noise increase of less than 2% was recorded. A difference in the distance between the converter and the ASIC of 2 mm or 3 mm between the two setups is not excluded, it is however in both cases an excellent result that confirms the compatibility of the DC to DC converters with the two existing systems.

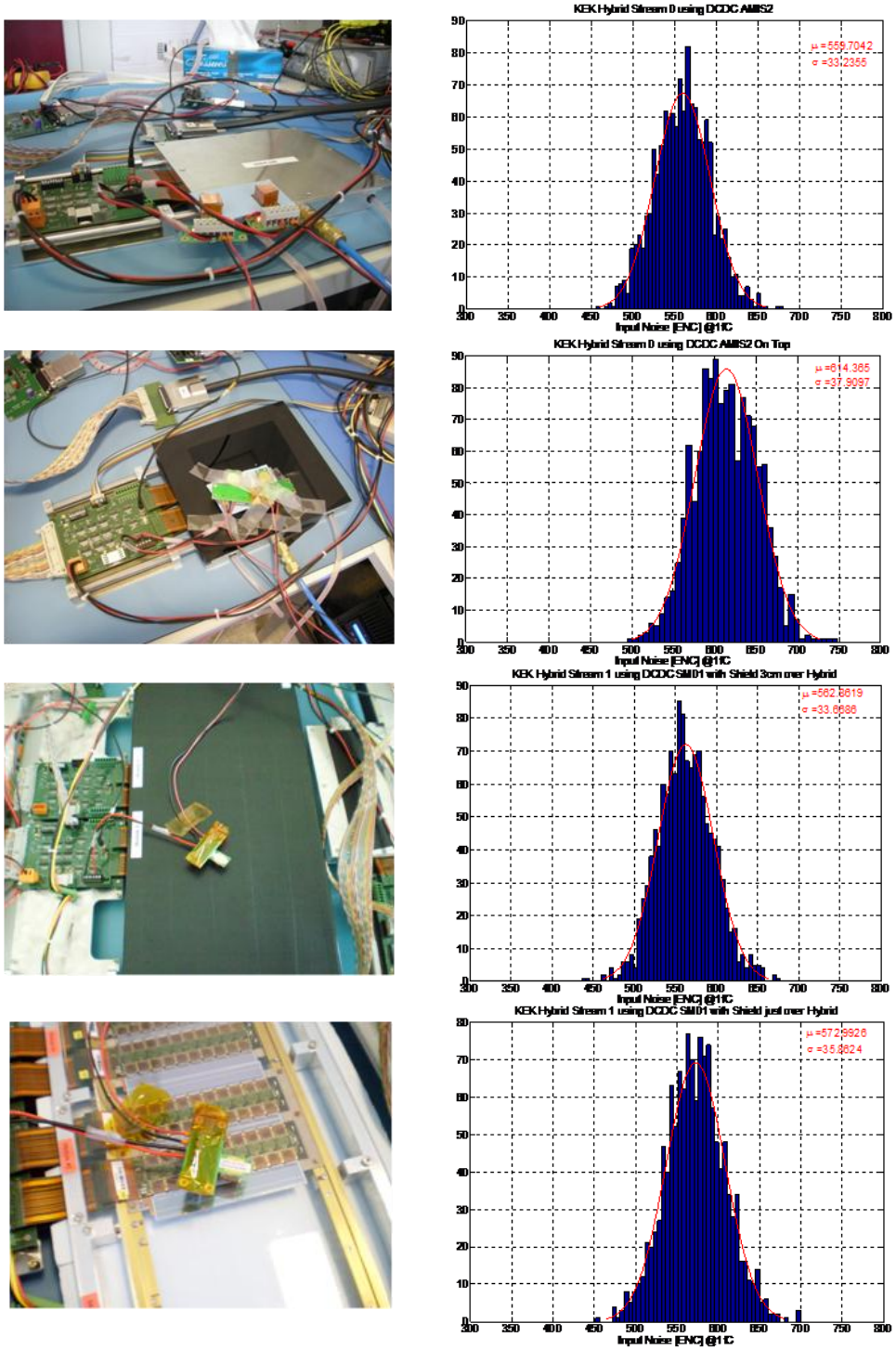

Figure 32: Noise susceptibility measurements of the University of Geneva tracker modules using the AMIS2_EMC converters (2 top figures) and the SM01B converter (two bottom figures).

7. CONCLUSIONS

Because of the increasing demand of power of the planned tracker front-end systems for the upgraded experiments at the sLHC, associated with the need for a more efficient and low mass power distribution system, new powering schemes became an absolute necessity. The scheme based on the use of DC to DC converters offers a classical and efficient solution, but its implementation in the harsh environment of the CERN experiments required solving specific technological issues.

The radiation tolerance is amongst the most difficult one and this was addressed through the exhaustive qualification of several microelectronic technologies: two manufacturers were selected and the basis of the first screening results. One of these was fully qualified for all the expected radiation damages; it was used to produce the AMIS2 ASIC on which the radiation tolerant plug-in-board is based on. The second technology is subject to new developments by the manufacturer, and although it provided very good results during the screening phase, the latest release used to produce the latest IHP2 ASIC failed to meet the radiation tolerance required. This technology requires further developments to fully meet the requirements in terms of radiation tolerance and CERN is actually collaborating with the manufacturer in this direction. Despite these difficulties, a radiation tolerant device suitable for the production of DCDC converters is now available and qualified, enabling the development of the proposed powering scheme.

As said before, four buck converter ASICs were produced, with different improvements in each of them. The AMIS2 device provides efficiencies beyond 78% even after full irradiation without any noticeable performance degradation.

The powering scheme will also require a second stage of DC to DC conversion, to be implemented inside the front-end ASICs. For this a switched capacitor converter has been developed in the same 0.13µ technology as the one planned for the final version of ABCN ASIC, achieving efficiencies of typically 95% for 100 mA of load current.

The compatibility between the converter modules and the front-end systems has been a major concern since the beginning of the project. The existing systems are still using ASICs in 0.25 µm technology, which requires larger currents than those targeted by the DCDC ASICs. Two types of converters have then been produced: those using commercial controllers able to deliver up to 5A, and those using the AMIS2 chip, limited to 2A. The characterization of the converters performance in terms of efficiency and noise is made using methods and setups implemented in a consistent manner at each development location: this enables the comparison of performances independently of the setup conditions, and was proven to be a key issue for the improvement of the designs. The noise generation and coupling mechanisms are now well controlled, and this enabled a strong optimization of the noise emissions finally implemented in the AMIS2-EMC module. Adding a shield cancels almost entirely the remaining radiated and conducted noise, achieving acceptable noise levels in the tested front-end systems even under extreme operation conditions. The commercial chip counterpart of the AMIS2-EMC board, namely the SM01B board, also fitted with a shield was found to be fully compatible on the Geneva system, also under extreme conditions. The AMIS2-EMC layout was used for the development of a similar converter for the CMS inner detector, leading to very good noise performances too. The AMIS2-EMC design methodology was presented recently at the TWEPP Conference.

Finally, the converters must be designed such that they can be industrially produced. The focus is now on the so far hand-made components of the converters. In collaboration with the industry, a custom air core toroidal coil has been designed and prototypes have been

produced with very good performances. Similarly, the manufacturing of the shield is a now the object of several studies: having started with folded copper foils that are unpractical to manufacture, the production of copper coated plastic boxes is now being evaluated and the preliminary results indicate performances very close to those achieved with the copper foil.

Most of the critical issues have now been solved: radiation tolerance, ASIC design, mitigation of noise couplings and production of custom components. All together, the production of converters is now fully possible enabling the implementation of the proposed powering scheme.

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