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Status Report on the RD-12 Project

Timing, Trigger and Control Systems for LHC Detectors

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Timing, Trigger and Control Systems for LHC Detectors

1 Introduction

The project objectives and the technical approach to TTC distribution being pursued by RD12 have been described in detail in the previous Status Report [1] and a more up-to-date overview is also available [2]. Hence this report summarises only the most recent developments and cites the reference documents in which detailed results are presented.

Since the last report the project participation has been enlarged, some new activities have been launched and further development has been carried out on the existing system components. TTC equipment has been supplied for initial integration work to subdetector groups of ALICE, ATLAS, CMS and LHCb, as well as the fixed-target experiment COMPASS, and discussions have commenced with ANTARES.

2 RD12 membership

The following new collaborators have joined the project:

Jose Carlos Da Silva, *Lab. Instrum. e Particules, Lisbon*

Per Gällnö, *CERN*

Thomas Toifl, *Inst. Kernphysik, Technische Universitaet, Vienna*

Joao Varela, *CERN*

These new participants have already been contributing to TTC development for a considerable time in the areas of synchronisation studies, electronics design and ASIC design.

3 LHC timing

The expected RF frequency of the LHC machine is now known with greater precision. Based on an expected machine circumference of 26658.883 m, the current best estimate [3] is 400.78966 MHz -2 kHz +1 kHz. The change of beta from 450 GeV to 7 TeV is $2*10^{-6}$, which results in a shift of about 1 kHz. A change of average radius of the beam in the machine of, say, 10 mm also corresponds to about 1 kHz.

The RD12 development equipment currently being supplied to the LHC experiments has an internal bunch-crossing clock generator with a tolerance of ±2 kHz at 40.08 MHz. The TTC transmitter PLL can track a maximum deviation of ±100 ppm with a bandwidth that can be adjusted to suit the bending field ramp.

As no hardware measurements are available it is not yet possible to refine the estimate of the phase stability of the bunch crossings in the LHC. There will be a periodic modulation of amplitude about ±16 ps at the revolution frequency of 11.246 kHz and also a smaller component (about one third of the amplitude) at the batch frequency. Residual phase noise is now expected to be only about 7 ps rms.

4 TTCvi VMEbus interface

The design has been completed of the TTC-VMEbus interface (TTCvi) module which interfaces the TTC system to the Central Trigger Processor (Global Trigger) and to the processors or development workstations which generate commands and data to be transmitted to the electronics controllers.

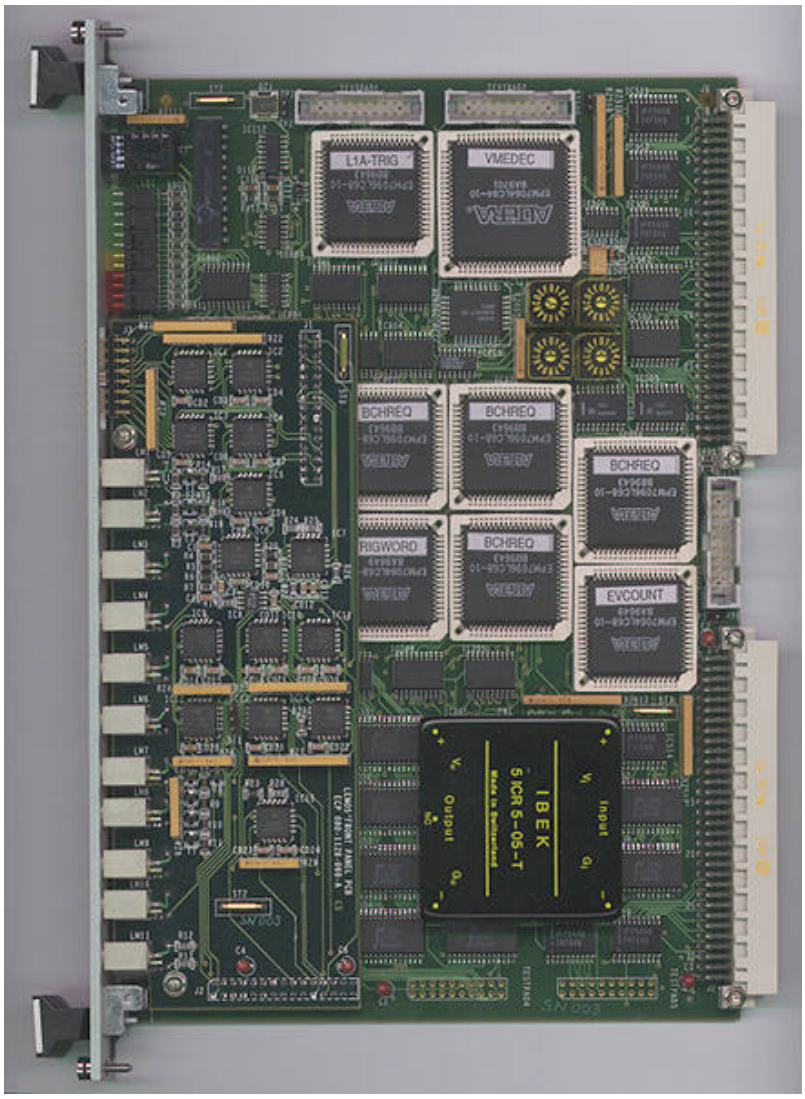

Fig. 1 TTCvi module

The latest version of the module, which is shown in Fig. 1, has been fitted with a power converter so that it requires only standard VMEbus power supplies. Special equipment has been developed for the production testing of this complex module, which contains about 300 components including 10 Altera FPGAs and 20 synchronous FIFOs.

A User Manual [4] for the TTCvi is available and a first batch of 20 modules has been produced, of which 13 have already been delivered and are performing satisfactorily. The components cost of the TTCvi is CHF 2500.

5 TTCvx VMEbus transmitter

While a few high-power laser transmitters have been supplied to TTC development groups and for special applications like the ATLAS test beam and COMPASS, the main demand at present is for mini-crate transmitters for TTC integration work by the LHC collaborations. A total of 19 of these have been produced, mainly equipped with just 3 or 6 channels of optical output each (out of a maximum of 12). User Notes [5] for the mini-crate transmitter are available.

The mini-crate comprises a number of individual modules which were produced early in the development phase of the project and which can be configured in various ways for carrying out a range of tests and evaluating different encoding systems and optoelectronic components. This phase of the work is largely over and the mini-crate will be replaced by a single, more compact, VMEmodule (TTCvx) having less flexibility but lower cost.

It is foreseen that the TTCvx module will incorporate the A/B Channel multiplexer and biphase-mark encoder and provide 4 channels of optical output from individual 1300 nm LED transmitters. A VMEbus crate is an electrically noisier environment than the dedicated transmitter crate, and a VMEmodule will require the use of more compact components. Hence it may be difficult to maintain the same timing jitter specifications but the performance is expected to be adequate for the great majority of applications. The design of the TTCvx is in progress and the module is expected to be available in March 1999.

At a later stage the high-power laser transmitters will also be repackaged in a compact form suitable for use in the LHC experiment electronics caverns. This will be done at as late a date as possible to profit from continued improvements in the cost/performance ratio of laser diodes.

Present estimates by the LHC collaborations of the desirable trigger zone partitioning suggest that there may be a need for an intermediate-power laser transmitter capable of broadcasting to, say, 128 destinations. An electrical output from the encoder in the TTCvx module should allow it to be used to drive a range of different laser transmitters with different optical fanout capabilities.

6 Optical tree couplers

Although 20 years have elapsed since fused biconic taper (FBT) passive optical couplers were first introduced to the market, this proven technology remains more cost-effective than planar silica waveguide, GRIN lens or fibre squid devices for a multimode fibre TTC distribution network. Since 1991, FBT optical tree couplers with fanouts up to 1:32 have been supplied to CERN by Canstar, who pioneered the technology with the Communications Research Center in Ottawa, Canada, in 1977.

In 1997 the Canstar Division of Alcatel Canada Inc was acquired by Framatome Connectors International (FCI), the connector subsidiary of Framatome Inc. (FCI is the third largest connector manufacturer world-wide, with 32 facilities manufacturing products under names like Burndy, Jupiter, Souriau, Connectral and Daut + Rietz). Alcatel is the major shareholder of Framatome Inc.

The Canstar fibre optic couplers are now manufactured in an ISO 9001 - 1994 facility at a pre-existing FCI plant in Scarborough, Ontario. Because the main product of the plant is electrical connectors, it is called FCI Electrical.

Following the transfer to FCI Electrical, production of the lowest-cost (ECS) couplers was discontinued, to be replaced by more robust but somewhat more expensive designs. These components are intended for operation in adverse environments and are temperature-cycled from -40 to +85 °C. FCI Electrical is cooperating with RD12 to define a less expensive optical tree coupler which would meet the needs of TTC distribution at the LHC experiments. This application permits some flexibility in packaging size, which allows a cost-effective housing to be used, and in insertion loss and uniformity, which are the basic criteria determining the fusing yield.

7 Optoelectronic receivers

Previous TTC development work was carried out with a DT200 InGaAs PIN diode + preamplifier device manufactured by Nortel, Paignton, UK, and packaged by Honeywell Optoelectronics, Aldermaston, UK, in either a standard telecommunications ST housing or the Lemo subminiature device mount. This component proved very satisfactory and showed little performance degradation after 20 MRad ^{60}Co irradiation. However, in March 1998 Nortel notified Honeywell that they would no longer supply the part in quantities of less than 10,000, which greatly exceeds that required during the RD12 project development phase.

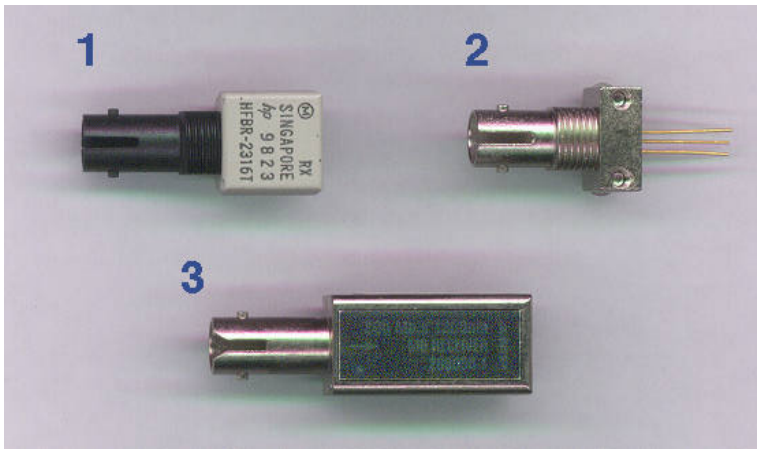

Fig. 2 PIN / Preamp and modular optoelectronic receivers
1 Hewlett-Packard HFBR-2316T
2 Honeywell / Lytel HFD 8005-002 / YBA
3 AMP 269050-1

A small selection of alternative devices (see Fig. 2) is being characterised to allow a choice of different cost / performance trade-offs for different TTC applications. The current baseline choice of PIN / Preamp is the Hewlett-Packard HFBR-2316T, a synthetic-package ST-connectorized device containing an InGaAs photodiode and Si bipolar transimpedance amplifier with a typical bandwidth of 125 MHz and an emitter-follower output buffer.

For more critical applications requiring lower clock jitter and greater dynamic range, a more expensive Lytel device packaged by Honeywell is available. This metal-package ST-connectorized device, HFD 8005-002/YBA, incorporates a GaAs transimpedance amplifier and meets the more stringent Sonet OC-3 specification.

In some applications, such as the ATLAS tile calorimeter electronics being developed at the Enrico Fermi Institute, Chicago, and the University of Stockholm, it is intended to drive a number of TTCrx ASICs on a short bus from each optoelectronic receiver. For this configuration the AMP 269050-1 and 269052-1 Molded-Optronic modular receivers, which have an ECL-compatible output, have proved satisfactory and a monitor receiver using this device is included in all the TTC transmitter crates. These components incorporate a novel integrally-moulded receptacle, lens and light-bending element [6] which results in reduced manufacturing costs but is unlikely to be rad-hard.

The DC-balanced bi-phase mark encoding of the TTC signals favours low systematic jitter. When receiving the signals from a high-power laser transmitter with an optical fanout of 1:1024, these optoelectronic receivers deliver an ECL signal with unfiltered transition jitter of 20 - 40 ps rms when 2^5-1 PRBS data are being sent on both the A and B channels at maximum rate.

As new optoelectronic receiver components are regularly introduced to the market the above selection cannot be considered in any way definitive. The evaluation process must be pursued until the time at which volume procurements of these devices are required by the LHC experiments.

8 Optical connector

Development of the subminiature optical single-fibre “RD12 Connector” family has been completed by industrial partner Lemo UK and the designs have been transferred to Ecublens, Switzerland, for production.

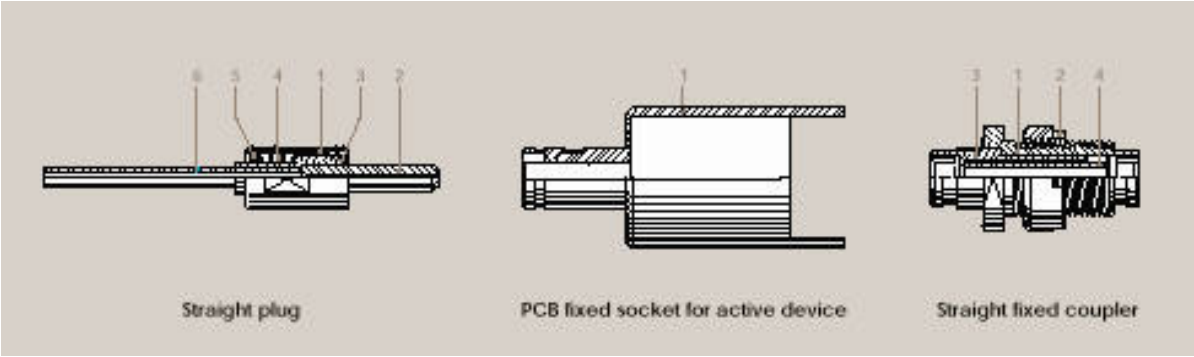

Fig. 3 RD12 subminiature fibre optic connector components

The connector family (Fig. 3) has met Boeing Specification D200Z001 Gaussian random vibration test, 5 hours per axis Category C, and is currently finding applications in a number of areas, such as avionics, where its small size and low mass are important.

The connector family now includes components for 9/125 μm singlemode and 50/125 μm, 62.5/125 μm, 100/140 μm and 200/280 μm multimode fibre. Details and performance characteristics are available from the Lemo website [7].

9 TTCrx timing receiver ASIC

The development of the special 15 x 15 mm BGA package for the TTCrx ASIC was completed by IBM Semea (Vimercate, Italy) and about 200 chips have now been packaged in it. At present, 44 of them have been distributed to some 20 groups using the RD12 TTC system in the LHC collaborations. A TTCrx Reference Manual is available [8].

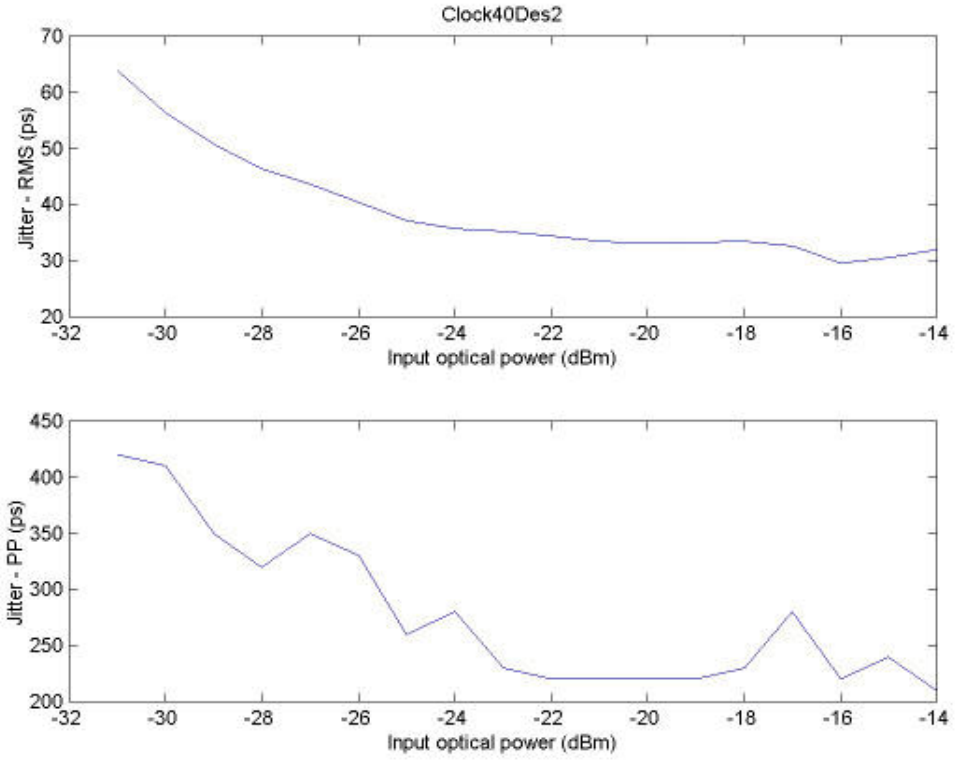

Fig. 4 Variation of TTCrx clock jitter with input optical power

As a result of the lower-inductance packaging, substantial improvements in recovered clock jitter (Fig. 4) and delay linearity (Fig. 5) have been achieved compared with the PGA version.

A new version of the TTCrx has also been developed incorporating several design improvements and this has been fabricated in AMS 0.8 μm technology. This chip incorporates a new design of limiting amplifier which accepts the direct input from a PIN/Preamp, rendering an off-chip postamplifier unnecessary. An initialisation PROM (which would not be rad-hard) is also no longer required and the TTCrx can load its 14-bit ID from the subaddress and data out buses after it is reset.

The new TTCrx incorporates an I2C bus interface through which read and write access is provided to all of the internal registers of the chip (with the exception of the upper 6 bits of the TTCrx ID, which are used as the I2C base address and can only be read). The I2C clock and data signals have been added without increasing the package pinout by re-assigning two pins formerly used for test functions. Access to internal nodes for debugging is still possible through the bunch counter bus (inputs) and the data qualifier bus (outputs), while it has proved possible to maintain the JTAG boundary scan functionality for test purposes.

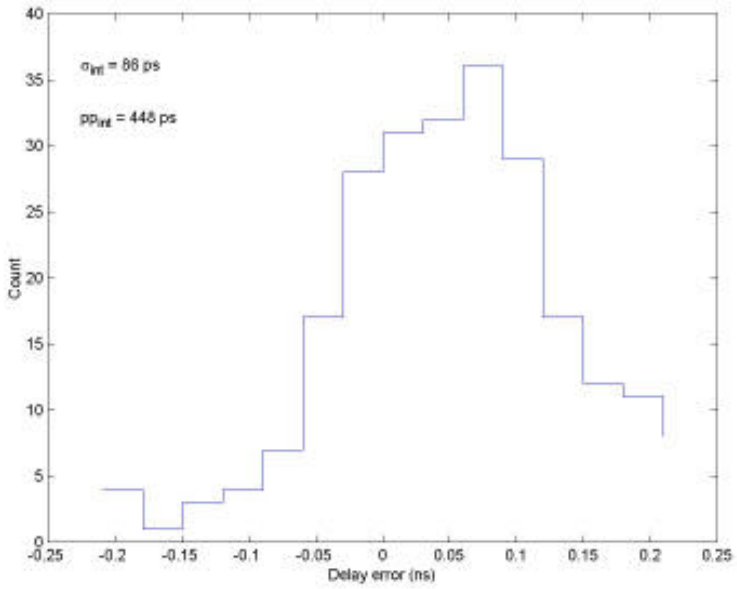

Fig. 5 Histogram of TTCrx delay line integral nonlinearity

The L1A latency of the new TTCrx has been reduced to 75 ns. Finally some decoding changes have been made such that the ERDUMP and CRDUMP commands can be addressed to individual TTCrx chips and 6 bits are entirely freed for user data (such as trigger IDs) in the short broadcast format.

The AMS TTCrx appears to be fully functional with a 3.3v power supply as well as at 5v and it will be characterised at the lower voltage once the test setup has been adapted for this too. The power consumption at 3.3v with all output clocks and buses enabled is only 140 mW. Preliminary measurements at this voltage on a device in a PGA package and using the internal postamp indicate an rms recovered clock jitter of about 35 ps at -20 dBm input optical power, rising to 75 ps at -30 dBm.

10 DMILL test chip

In parallel with the development of the AMS TTCrx the design is being ported to DMILL 0.8 μm SOI technology. A first test chip has been fabricated [9] which incorporates the critical analogue postamplifier, PLL and clock and data recovery circuits and delivers the clock with the multiplexed A/B Channel data. The new postamplifier design in this ASIC has four bipolar stages with hard limiting.

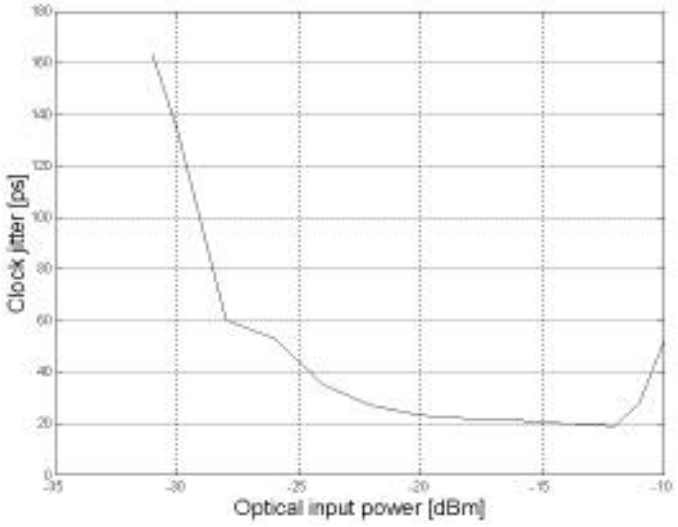

Fig. 6 Variation of DMILL TTCrx test chip clock jitter with input optical power

The PLL, which has a differential oscillator to improve the rejection of power-supply noise, employs a special charge-pump biasing scheme [10] to minimise the effect of variations in transistor parameters. It incorporates a novel phase and frequency detector [11] to lock to the self-clocking biphase-mark encoded signal.

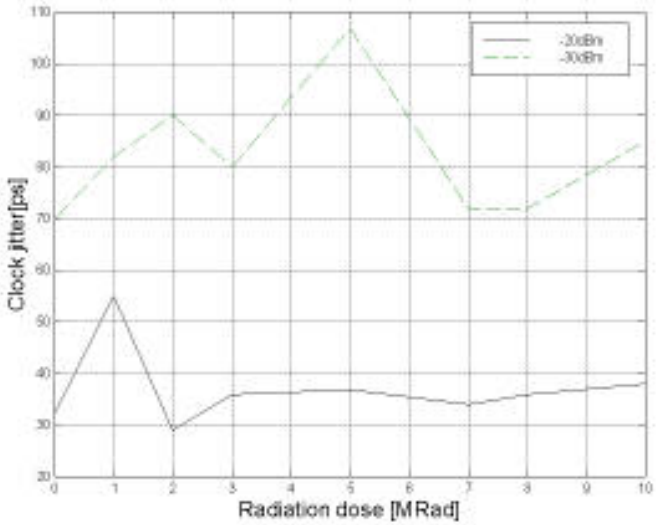

Fig. 7 Variation of DMILL TTCrx test chip clock jitter with radiation dose

Some preliminary measurements have been made on the DMILL test chip and further studies are in progress. Fig. 6 shows the variation in recovered clock jitter with optical input power using the Honeywell / Nortel PIN / Preamp when only the periodic idle sequence is being transmitted. With PRBS data (2^{12} -1 sequence) on only the B Channel, the minimum rms jitter increased to about 84 ps, rising to about 100 ps with PRBS data on both A and B channels.

During this measurement the current in the programmable charge pump was set to its minimum value, but it was subsequently discovered that after irradiation the matching of the NMOS and PMOS transistors deteriorated at low currents. In a preliminary irradiation test, Fig. 7 shows for two levels of optical input power how the recovered clock jitter varied as the dose was increased to 10 MRad. To avoid the problem of imbalance in the charge pump, the reference current in this test was set to twice the minimum value.

The preliminary results with the DMILL test chip demonstrate the feasibility of developing a radiation-hard version of the TTCrx and it is planned to submit the full design for fabrication early in 1999.

11 TTCrx evaluation card

In order to facilitate the work of users making a first evaluation of the RD12 TTC system, a number of mezzanine evaluation cards have been made available which support the TTCrx ASIC and associated components.

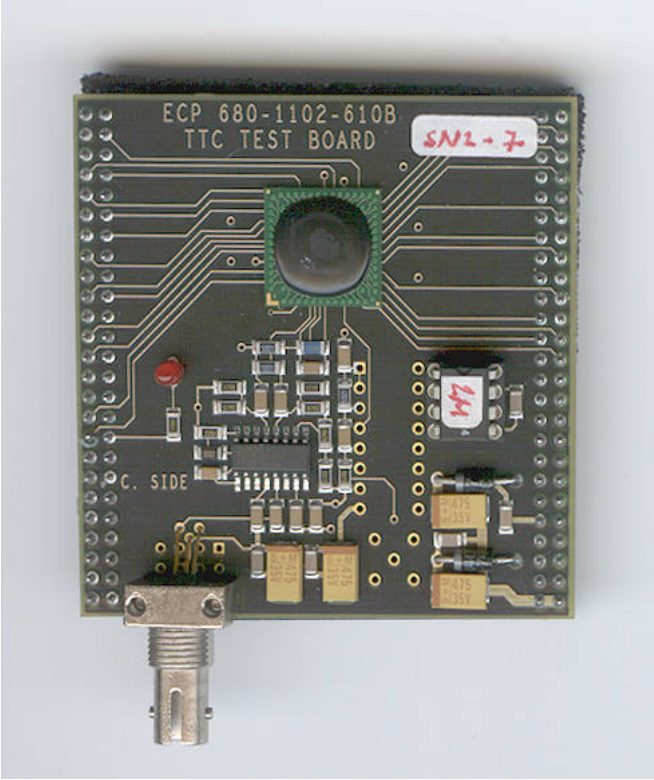

Fig. 8 TTCrx mezzanine evaluation card

The latest version of the card (Fig. 8) carries the BGA-packaged CMOS ASIC and has a special PIN / Preamp footprint which allows it to be fitted with either the HP or the Honeywell / Lytel component.

The present card also carries an NE5225D postamplifier and associated components, which will not be necessary with the production version of the TTCrx. A

configuration PROM is also included, which it will be possible to replace by a hardwired or switch address source.

12 TTCsr PMC module

The TTCsr module, a TTC simple receiver PCI mezzanine card, has been debugged and is now performing satisfactorily. It is being used by the ATLAS data acquisition group for Level-2 data requests and decisions in the DAQ-1 prototype.

13 TTC emulation board

A TTC emulation VMEmodule has been developed for the CMS RDPM programme. This A24/D32 slave module (see Fig. 9) accepts a TTCrx mezzanine card and by software selection the fast input event queue and output farm request queue commands transmitted to the RDPMs can be generated from TTC signals or VME commands.

Fig. 9 TTC emulator board connected to one RDPM

7 TTC emulation boards have been built and tested in a full event builder chain with switch and farm units. A User Manual [12] is available.

In the RDPM test setup the system was driven by a TTCvi module and mini-crate transmitter. As part of this development Macintosh LabVIEW drivers were written which have been made available to other users of RD12 systems.

14 TTC in ALICE

The timing method planned for the ALICE TOF system is to start TDCs from the arrival of the pulse produced by a passing particle, and to stop them with the next 40.08 MHz LHC clock transition delivered by the TTC system.

The Pestov counters, which have a timing resolution of 100 ps, had particularly stringent requirements on TTC clock jitter. In January 1998, the PID panel in ALICE recommended that the PPC option should be chosen for the TOF system instead. Since the timing resolution of the PPCs is about 300 ps the choice of this technology eases the timing precision requirements somewhat. As a result the timing precision required for the TOF detector TTC system may be relaxed and it seems very probable that the RD12 system can meet the requirements.

However, it would be premature for ALICE to subscribe to a User Requirements Document since the propagation of timing errors at each step in the timing chain is an important issue and the timing precision required at each step is still under review. At present, it appears that a timing precision of 50 ps should be sufficient.

For the FMD-MCP detectors the fast trigger logic will use the TTC clock and the MCP pulses to determine the interaction diamond. In this case also a clock signal with 50 ps timing resolution may be required.

ALICE also plans to use the TTC system to send the Level-1 trigger signal to the subdetectors and to distribute trigger numbers. The ALICE team at the University of Birmingham has recently purchased a test setup comprising TTCvi, transmitter mini-crate and TTCrx in order to gain experience with the RD12 system and evaluate its suitability.

15 TTC in ANTARES

The large-scale cosmic neutrino water Cherenkov detector experiment ANTARES has a requirement to distribute a clock signal with a precision of the order of 100 ps to about 100 destinations spread over a volume of 100 m x 100 m x 400 m.

The possibility of using some of the optical distribution technology developed in RD12 for this application is currently being studied. A clock frequency of around 40 MHz would be quite appropriate for this detector so that the use of an RD12 laser transmitter with passive optical fanout to TTCrx ASICs at the undersea electronics destinations is being considered.

An optical fibre TTC distribution network for ANTARES would be considerably larger than for the LHC experiments but at 1300 nm fibre attenuation is very low even for runs of several 100 m. With 50/125 μm graded-index fibre of modest bandwidth (exceeding 400 MHz.km), multimode dispersion is also negligible in an RD12 system for fibre lengths up to 400 m.

16 TTC in ATLAS

ATLAS was one of the first experiments to specify the use of the RD12 system for the TTC distribution backbone [13] and some of the subdetector groups of the collaboration have been using mini-crate systems since early 1996. No serious problems have been encountered except for some accidental physical damage to optical fibres and no electronic or optronic failures have been experienced.

At an early stage the ATLAS Trigger-DAQ Steering Group specified the requirements for interfaces with the front-end systems [14], indicating which part of the RD12 system would be provided and maintained by the Trigger-DAQ Group and which part (essentially from the optoelectronic receivers associated with the TTCrxs onwards) would be the responsibility of the subdetector groups. The document was drawn up in collaboration with RD12, reviewed internally and approved at an ATLAS plenary meeting. It has been the basis of subsequent TTC integration work by the subdetector groups.

In preparation for the submission of the ATLAS Level-1 Trigger Technical Design Report, a TTC User Requirements Document [15] was prepared in February 1998. The URD specifies that the TTC destination shall be able to work in a radiation environment of 100 kRad and 10^{13} N.cm^{-2}, which should be readily possible with the DMILL TTCrx and InGaAs / GaAs PIN / Preamp. It also specifies a maximum BER of 10^{-14} (1 bit error per week at 160.32 MBaud) and a maximum clock jitter of 50 ps rms, which may be considered challenging performance targets for a very large system with some defective channels exposed to numerous potential sources of EMI.

In April 1998 the CTP / TTC plans were studied by a special review panel including representation from the various ATLAS subdetectors. At this review [16] the most stringent timing precision requirement was specified as 100 ps for the LArg calorimeter. The review panel welcomed the introduction of the TTCrx I2C bus interface, which is convenient for TTC destinations on VMEbus modules.

The Level-1 Trigger TDR was submitted in June 1998. The TTC section [17], in addition to reviewing the interfaces, components, partitioning and functionality of the system, specifies the schedule for TTC system production and the review procedures which are foreseen to assure the required quality. Some of the principal milestones given to the Technical Coordination Group are a follows:

Dec 1999	PDR for TTCvi and TTC transmitters Irradiation test of TTCrx
June 2000	FDR for TTC transmitters PDR for TTCrx
Sept 2000	FDR for TTCvi
Dec 2000	FDR for TTCrx
June 2001	TTC components available to ATLAS groups
June 2005	Full Level-1 system available *in situ*

In September 1998 the LHCC endorsed the positive assessments by the referees and recommended to the Research Board to give general construction approval to the ATLAS Level-1 trigger subsystem of which the RD12 TTC system is a part.

17 TTC in CMS

CMS also made an early commitment to use the RD12 TTC system [18] and the experiment collaboration has contributed to its development. Some integration work has started and mini-crate development systems have been supplied for preliminary beam tests of the tracker APV and readout electronics, Level-1 trigger development at the University of Wisconsin and synchronisation studies and event builder work at CERN. The intended development by RAL of a TTC daughter card for the 9U FED board has been postponed due to staff shortages and the need to give short term priority to the FED PMC development.

The FED PMC [19] is an intermediate step for the convenience of instrumentation for beam tests, benchwork and detector module testing, while the 9U FED is still the baseline for the final system as per the latest Tracker TDR and will require TTC integration in due course.

For the FED PMC it is planned to develop a TTC transition module which may be plugged on to the J2 spare pins on the VME backplane. The TTC signals can then be routed via the SBC carrying the FED PMC to the auxiliary connector of the module.

In February 1998 a TriDAS Workshop was organised at CERN and one day was devoted to the review of the front-end systems, including discussion of the TTC requirements. The proceedings [20] record that the CMS users were generally satisfied with the functionality and timing accuracy of the RD12 system. Reservations were expressed about the plans to support only one final (DMILL) version of the TTCrx and the introduction of the I2C bus instead of JTAG. (It has now proved possible to maintain JTAG boundary scan functionality as well as I2C).

At the TriDAS Workshop each of the subdetector groups indicated the expected number of RD12 TTC destinations required for their system architecture and the total for the experiment (excluding Preshower) was about 4700. This information has been recorded in a Table [21] which is updated as additional data are received. Additional details of the TTC implementations planned by different CMS subdetector groups had been reviewed at the earlier TTC Workshop [22].

The CMS Level-1 Trigger TDR will be released in 2000. Prior to that time engineering evaluation and prototyping of the hardware is being carried out to provide the information required for the subsystem designs and interface specifications.

18 TTC in COMPASS

In October 1997, RD12 was requested to provide support to the hadron structure and hadron spectroscopy experiment COMPASS, within the limits of available resources. COMPASS, which was approved by CERN in February 1997, is also considered a test-bed for some technologies to be used at the LHC. However, the RD12 TTC system developed for LHC timing is not directly applicable to an SPS fixed-target experiment.

After discussions the collaboration decided that they wished to exploit the RD12 high-power laser transmitter development but not the TTCvi or TTCrx. A special version of the high-power transmitter crate has been developed for this application

operating at 155.52 MBaud instead of 160.32 MBaud. The COMPASS group at the Technische Universität, Munich, are developing their own receivers for use with it.

19 TTC in LHCb

The LHCb collaboration has been supplied with one mini-crate system for the development of the timing and trigger distribution (TTD) system [23] for the front-end and off-detector electronics of the vertex detector (VD), for which it is planned to use an RD12 backbone. In the planned configuration a local vertex detector TTD transmitter allows both local fast control signal generation and global LHCb running from a central TTD transmitter.

The whole electronics is partitioned in units which follow the geometrical R-phi partition of the VD. A number of FE chips (e.g., on one hybrid) are handled by a read-out module in the ODE. This unit has one TTD receiver in the FEE and one in the ODE. If only one TTCrx is included in one read-out module then its phase adjustment features would be used as a global adjustment affecting all the FADCs in the module. To avoid the complexity of having additional adjustable delays the timing dispersion between hybrids would be minimised, for example by adjusting the cable lengths within 1-2 ns.

LHCb considers that the RD12 TTC system will be a vital part of the Timing and Fast Control (TFC) system [24] of the experiment and that support for it will be crucial. But the detailed mode of operation of the system for the broadcasting of the Level-1 data is the subject of study and the collaboration is not at present in a position to subscribe to a User Requirements Document. The LHCb team has requested a number of changes to the TTCrx design which have been incorporated in the latest version of the ASIC.

In LHCb the TTC A Channel will be used to distribute the Level-0 decision and Level-1 data will be broadcast on the B Channel, which makes a heavy demand on the available bandwidth. Several possible approaches are being studied. The short format frame may be used to broadcast every Level-1 decision with part of the event ID for cross-checking at a rate of about 1 MByte/sec. Alternatively only Level-1 accept decisions may be broadcast using the long format, transmitting up to 16 bits of event ID but only for the accepted events.

20 Synchronisation

The RD12 system provides for the individual fine deskew, in steps of 104 ps, of the phases of the two 40.08 MHz clocks delivered at each TTCrx destination. Provision is also made to adjust the timing of non-periodic signals such as the Level-1 trigger accept and test commands by up to 16 bunch-crossing intervals of 25 ns. The periodic Bunch Counter Reset signal, which is broadcast by the TTC system at the LHC orbit frequency, is automatically subjected to the same coarse deskew as L1A, so that the bunch number delivered with each L1A remains in synchronism with it. A separately programmable delay is provided for test commands.

These timing deskews in each TTCrx can be adjusted by commands which are entered to it by the local I2C bus or transmitted over the TTC network itself. For

each trigger distribution zone, the global adjustment of the phase of those broadcast signals which are synchronised with the LHC orbit is programmable in the TTCvi through the VMEbus.

Subsystem groups in each of the LHC experiments are studying a variety of strategies for using these facilities to set up the timing of each subdetector. The fine deskews must be adjusted so that signal sampling occurs at the appropriate time, while the coarse deskews must be set such that the correct L1A and bunch number are associated with the data from the appropriate bunch crossing.

The general approach to the setting up of the timing in ATLAS is summarised in the Level-1 Trigger TDR [25] and the detailed implementations are being worked out by the Trigger/DAQ and subdetector groups. A database of fibre lengths will be maintained so that an initial setup of the coarse deskews will be possible by the use of test pulses. Final tuning when colliding beams are available in the LHC will be done by crosscorrelation of the occurrence times of events with the known LHC bunch structure.

CMS has issued a Synchronization Document [26] to gather information on timing issues for the different front-end electronics, trigger and readout systems. This addresses many issues relevant to the implementation of the TTC system for the experiment ranging from the requirements on clock jitter, drift and fine deskew step size to the architecture of the optical distribution network itself.

It is planned to hold a CMS Synchronization Workshop at CERN on 11 November 1998 at which the TTC requirements will be discussed in the wider context of the synchronization of the different subdetectors, trigger and DAQ links and the DAQ.

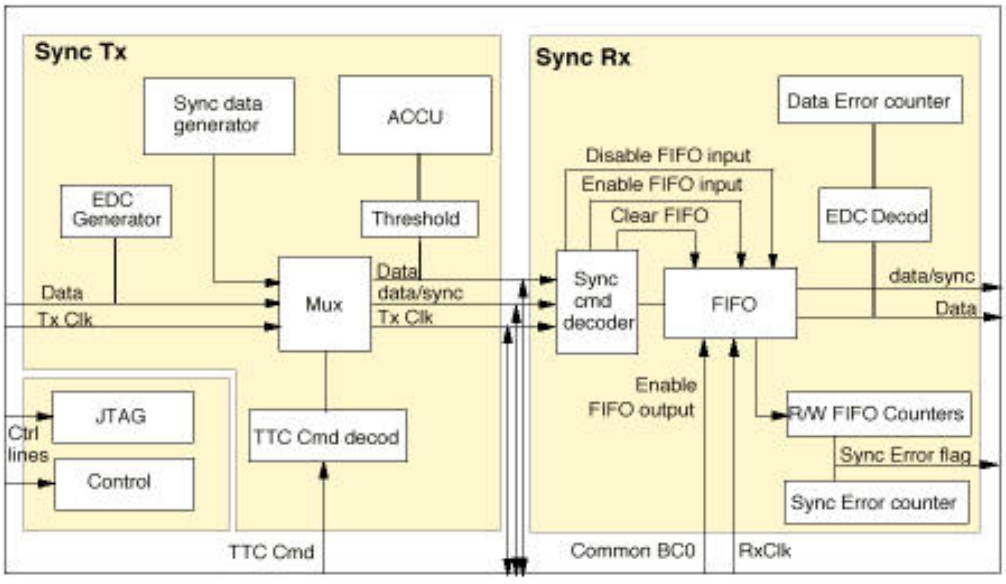

Fig. 10 Synchronization circuit block diagram

The synchronization of the CMS calorimeter trigger has been the subject of detailed study [27] and development. Prototype Sync Tx and Sync Rx circuits (see Fig. 10) have been implemented in two XILINX FPGAs with an external RAM accumulator for histogramming the bunch profiles. The prototype circuits [28] have been

integrated in the trigger primitives test setup for the calorimeter and in March 1998 were successfully tested with a TTCvi, mini-crate transmitter and 3 TTCrxs.

LHCb is studying the integration of special hardware in the FEE and ODE for clock phase adjustment using calibrated data sent over an analog data link. Several scenarios are being considered for event synchronisation and the detection of synchronisation errors using either a digital or analog link [23].

21 Conclusion

The RD12 Project has progressed further in its endeavour to create a common solution to the problem of TTC distribution at the LHC experiments. Systems developers, electronics and microelectronics designers have continued to cooperate successfully with industrial partners and representatives of the experiment collaborations at CERN and external institutes. Regularly-updated information and detailed documentation concerning the developments is available on the web at http://www.cern.ch/TTC/intro.html.

If it is desired to continue funding the work as a common project a budget allocation of CHF 100K should be foreseen for 1999. This will cover the development cost of the TTCvx prototype, optoelectronic component evaluation, irradiation tests, a DMILL submission of the complete TTCrx and an MPW run of the AMS 0.8 μm version including packaging, testing, and the design of new evaluation cards. As in the past, the equipment delivered by RD12 to the experiment teams will be charged directly to them.

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