Using TTC system and VME bus in the LVL2 demonstrator program

1. Introduction.

In the LVL2 demonstrator, a number of ROBs will be housed in one or more VME crates. Each of these ROBs has to:

- Transmit data to the LVL2 processor system each time a ROI involves this particular ROB.
- Clear events which did not pass LVL2 criterion (L2R).
- Transmit events which passed LVL2 criterion (L2A) to LVL3 processors.

This note describes the possibility to use the TTC system (TTCvi, optical fanout and TTCsr) and the VME bus to transmit the ROI requests, the L2R and the L2A.

2. Bandwidth requirement on the transmission media.

2.1. ROI request.

A ROI request could consist of:

• ROI request code	8 bits
• Event ID	24 bits.
• BCID	12 bits.
• Trigger type	8 bits.
• ETmiss	32 bits.
• Eta, Phi	12 bits.
• ROI type	2 bits.
• LVL2 global processor ID	8 bits .
• LVL2 local processor ID	8 bits .
Subtotal	114 bits per ROI.

Assuming an average number of 5 ROIs per event and an event rate of 10^5, this leads to a total bandwidth requirement of 57 Mbits/s.

2.2. L2R request.

The L2R request consists of:

• L2R code	8 bits
• Event ID	24 bits.
• BCID	12 bits.
• Subtotal	44 bits.

Assuming a L2R rate of 10^5, this leads to a total bandwidth requirement of 4.4 Mbits/s.

2.3. L2A request.

The L2A consists of:

• L2A code	8 bits
• Event ID	24 bits.
• BCID	12 bits.
• LVL3 processor ID	8 bits .
• Subtotal	52 bits.

Assuming a L2A rate of 10^3, this leads to a bandwidth requirement of 52 kbits/s.

2.4. Summary of LVL2 bandwidth requirements.

A total of about 65 Mbits/s is required.

2.4. Level 1 and timing requirements.

If one want to use the same TTC network to transmit Level 1 and timing, one has to take the following into account:

• L1A	Use TTC A channel
• Bunch Counter Reset	2 μs each 88 μs are required.
• Trigger type	800 kbits/s

In total we need about 8 % of the TTC network bandwidth.

2.5. Bandwidth available on the TTC network.

The TTC network driven by the TTCvi has a total available bandwidth of 15 Mbits/s. It could appear insufficient, nevertheless the following remarks have to be made:
1. Several TTC networks and TTCvi could be used. If we assume 4 to 5 TTC networks mapped on an Eta/Phi division, the total bandwidth required on each of them will be close to 15 Mbits/s assuming an intelligent selection is done before transmitting the ROIs requests so that they are sent only in the proper Eta/Phi zone.

2. For the demonstrator, one could restrict the requirements as the number of ROBs will cover a very small equivalent Eta/Phi zone. We could then assume that there is only 1 ROI per event. In this case the TTC bandwidth is large enough.

3. TTC simple receiver [TTCsr].

The TTCsr is a PMC module with a slave PCI port, which can handle the LVL1 signals and store in FIFOs the data received from the TTC network or generated by the TTC receiver chip [TTCrx] such as EvtID and BCID.
Using this module for ROI requests, L2R and L2A means that one has to implement on the PMC carrier board which houses it, the read out and the decoding of the information stored in the FIFOs and them to transmit them to the ROBs.
This could be implemented in software in one uses intelligent PMC carrier board. The basic task to be implemented would be:

• Read TTCsr FIFO
• If L2R
  Broadcast EvtID, BCID, Command to the ROBs
• If L2A
  Broadcast EvtID, BCID, LVL3 Proc. ID, Command to the ROBs
• If ROI request
  Decode Eta/Phi
  Broadcast to concerned ROBs EvtID, BCID, LVL2 Proc. ID, Command

Assuming there is no operating software overhead, the 10 μs available in average to perform this task should be enough (measurements are foreseen in the LVL3/DAQ prototype group).

4. Bandwidth requirement within a crate.

The information received in the TTCsr and decoded has to be transmitted to the ROBs located in the crate.
Here are the information a ROB needs with each request:
• L2A
• L2A code 8 bits
• Event ID 24 bits.
• BCID 12 bits.
• LVL3 processor ID 8 bits .

• Subtotal 8 bytes.
All the ROBs have to receive this information.

• L2R
- L2R code 8 bits
- Event ID 24 bits.
- BCID 12 bits.

- Subtotal 8 bytes.

All the ROBs have to receive this information.

• ROI request
- ROI request code 8 bits
- Event ID 24 bits.
- BCID 12 bits.
- LVL2 processor ID 8 bits

- Subtotal 8 bytes.

Only the ROBs which have data belonging to the ROI have to receive this information. Assuming 8 bytes of information leaves some room for additional information (for instance to make a pre-processing selection).

To evaluate the bandwidth requirement, the following assumptions are made:
• L2A and L2R are broadcasted to the ROBs.
• A sub-detector is mapped in Eta/Phi in N ROBs. There are X ROBs within a crate and a ROI involves n ROBs. This leads to the fact that each ROI request involves in average X*n/N ROBs in a crate[1].

The bandwidth requirement is then:
• L2A 8 kbytes/s.
• L2R 800 kbytes/s.
• ROI request X*(n/N)*800 kbytes/s /ROI.

• Total for 5 ROIs/event 0.8 * (1 + 5 * X * n/N) Mbytes/s.

Let's take the TRT as an example. There are 512 ROBs mapping the detector and a ROI involves 6 ROBs. Assuming 16 ROBs per crate this leads to a bandwidth requirement of about 1.6 Mbytes/s. This number makes the VME bus a very good candidate to transmit these requests.

[1] If the X ROBs of the crate are not mapping adjacent Eta/Phi, then a ROI either does not request any data from the crate or only data from one ROB. This gives in average X*n/N ROBs involved per ROI.
If the ROBs are mapping adjacent Eta/Phi, then there are X-n+1 ROIs which involve n ROBs in the crate, 2 which involve 1 ROB, 2 which involve 2 ROBs, ..., 2 which involve n-1 ROBs. In total it gives again an average of X*n/N ROBs involved in a ROI.

It has been assumed that a broadcast mechanism is implemented, which is the case for instance if we use the CES RIO2 board. If this mechanism were not available then the required bandwidth would be about 14 Mbytes/s (for 16 ROBs in a crate) which is still reasonable. In addition, one could make use of maximum VME capability in waiting for a number of L2R before initiating a DMA access. One could also, when several ROBs are connected to a "concentrator", limit the communication to the "concentrator" alone.

5. Conclusions.

1. The TTC system is a good candidate to transmit LVL2 requests and results to the ROBs of the LVL2 demonstrator. Its usage in a full system could be envisaged but might be marginal. This applies only for demonstrator B type as the demonstrator C uses ATM for this purpose.

2. The capability to use a standard processor in a PMC carrier board to decode the LVL2 requests has still to be confirmed but does not seem to be unrealistic. This would allow to easily emulate the LVL2 requests for test purposes and during the time the necessary interfaces are being developed (e.g. TTCsr). This makes also very easy the use of different media to transmit LVL2 requests and results: only the PMC interface has to be changed.

3. VME bus can be used to transmit the LVL2 requests and results to the ROBs within a crate as the required bandwidth is low. This is valid for all the demonstrators and is also valid for the full system.