TTCrx and QPLL Mezzanine Card (TTCrq)

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Rev 0.1 – Preliminary

Introduction

A new mezzanine card is being designed as an alternative to the existing TTCrm supported by the CERN Electronics Pool (EP-ESS Group). The aim is twofold: to produce a card that can be mounted on a standard VME unit without imposing restrictions on the spacing between two modules and to add the QPLL functionality to the board[1]. Additionally the TrueLight pin-preamp (TRR-1B43-000) will replace the Agilent (HFBR – 2316).
The new TTCrx mezzanine card will be backward-compatible with the TTCrm. That means that the existing electrical connectors (J1 and J2) will be kept in the same physical positions with the same pinout. An additional connector (J3) will be added to the card located on the PCB side opposite to the optical connector side as represented in Figure 1. J3 will be a 26-pin connector. (VME board areas under the dotted/shadowed regions (top view drawing) should remain free for tool insertion during board removal.)

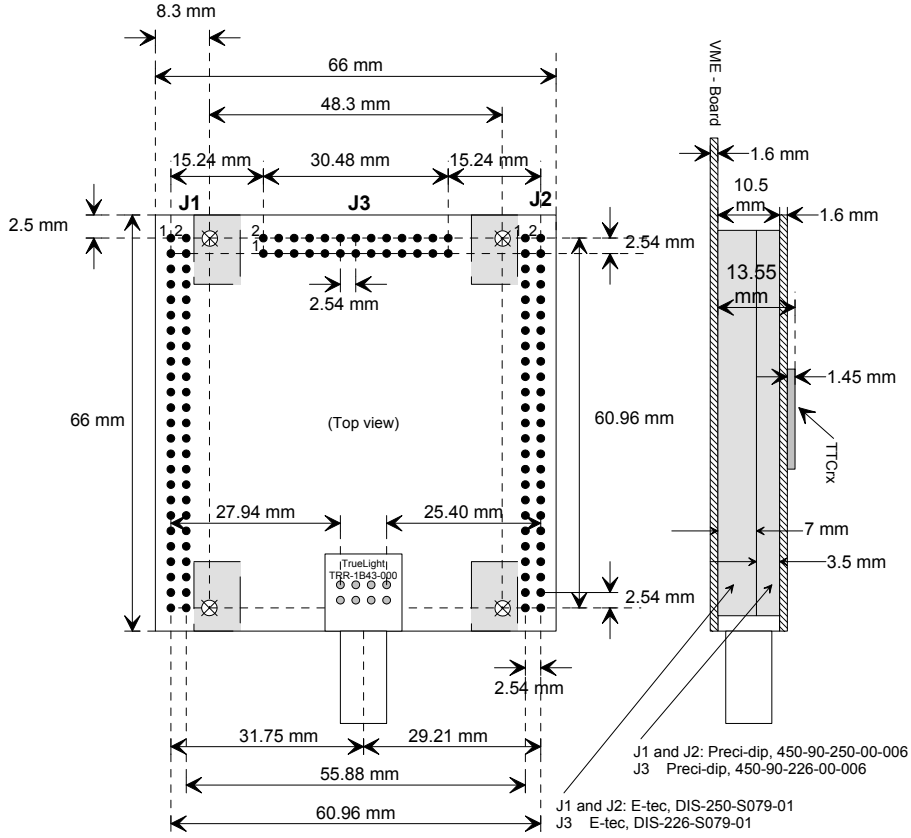

Figure 1 TTCrx and QPLL mezzanine card

To reduce the module height the optical receiver will be mounted under the card on the same PCB side as the electrical connectors. Therefore, the optical connector will moved to the other side of the PCB but its distance to the J1 and J2 connectors will remain unchanged (please see details in Figure 1).
As shown in Fig. 1, the overall height of the components on the mounted TTCrq mezzanine card is 13.55 mm above the components side of the VME motherboard. To ensure compliance with VMEbus Rule 7.14, assembled VME modules should be measured to verify that the sum of TTCrm component height and board warpage does not exceed 13.71 mm.

[1] Support by CERN Electronics Pool for the new mezzanine is under discussion.

The 13.71 mm limit allows a guaranteed 2.44 mm clearance between the TTCrx and the longest component leads on the adjacent VME board. More importantly for the cooling airflow, it allows a nominal 4.91 mm space to an unwarped adjacent VMEboard. According to VMEbus Observation 7.11, this space allows adequate airflow for cooling. However, designers should avoid putting high-dissipation components on the VME board underneath the mezzanine board, as the horizontal orientation of the connectors is likely to restrict cooling airflow to them.

Circuit

A block diagram of the mezzanine card is represented in Figure 2. As before the card contains a pin-preamplifier (the Truelight TRR-1B43-000), the TTCrx, the PROM and a bank of pull-up/pull-down resistors to setup the TTCrx address. The address jumpers were removed to satisfy the space constraints. Dipswitches will replace the jumpers if the available PCB space will allow for them. Otherwise, address setting will be done by soldering the appropriate pull-up / pull-down resistors. Connectors J1 and J2 remain in the same relative positions with the same pin assignments. Additionally, a QPLL and its associated crystal are added to the card. All the QPLL pins (with the exception of the crystal dedicated pins and VCXO decoupling capacitor pin) are accessible through the connector J3. The QPLL input can be taken either from the J3 connector (external source) or from one of the TTCrx clock outputs (Clock40, Clock40Des1 or Clock40Des2). When using the QPLL with an external source the reference clock signal can be either LVDS or CMOS.

All the QPLL clock signals are available in the J3 connector as LVDS signals. Additionally, the 40 MHz clock output is also present as a CMOS output.
As before, two independent power connections are present on the board: one dedicated to the pin-preamplifier and the other for the remaining circuitry. The TTCrx, the PROM and the LVDS/CMOS level converter can be either powered from 3.3 or 5 V. The choice of this voltage will set the CMOS levels of all the TTCrx signals as well as that of the 40 MHz CMOS clock output in the J3 connector. Notice however, that the pin-preamplifier has to be powered from a 5V power supply. The power supply for the QPLL is obtained from the TTCrx power using a 2.5V low dropout regulator.

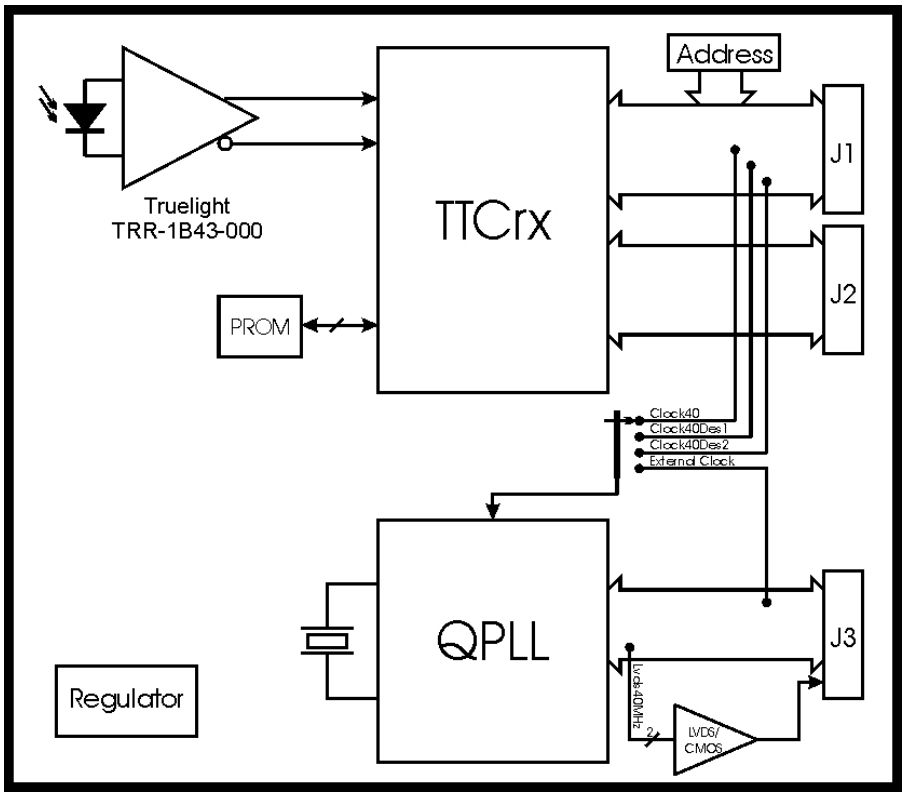

Figure 2 TTCrq block diagram

Users of the TTCrq should be aware that due to limited lock range expected for the QPLL (≈ ±50 ppm), high precision clock references centered around the LHC clock frequency will be required to guaranty lock during laboratory test.

J3 connector pin assignments[2]

Pin Number	Signal Name	Signal type
1	f_0Select<0>	Input, CMOS 5V compatible
2	mode	Input, CMOS 5V compatible
3	inLVDS+	Input, LVDS
4	inLVDS-	Input, LVDS
5	gnd	Power
6	externalClock	Input, CMOS 5V compatible
7	autoRestart	Input, CMOS 5V compatible
8	externalControl	Input, CMOS 5V compatible
9	f_0Select<3>	Input, CMOS 5V compatible
10	~reset	Input, CMOS 5V compatible
11	locked	Output, CMOS 2.5 V
12	error	Output, 2.5 V compatible
13	gnd	Power
14	lvds80MHz-	Output, LVDS
15	lvds80MHz+	Output, LVDS
16	gnd	Power
17	f_0Select<2>	Input, CMOS 5V compatible
18	gnd	Power
19	lvds160MHz+	Output, LVDS
20	lvds160MHz-	Output, LVDS
21	gnd	Power
22	lvds40MHz-	Output, LVDS
23	lvds40MHz+	Output, LVDS
24	f_0Select<1>	Input, CMOS 5V compatible
25	cmos40MHz	Output, CMOS
26	gnd	Power

[2] J1 and J2 pin assignments are left unchanged. Please see the TTCrx reference manual in the TTC system web site (http://ttc.web.cern.ch/TTC/intro.html).