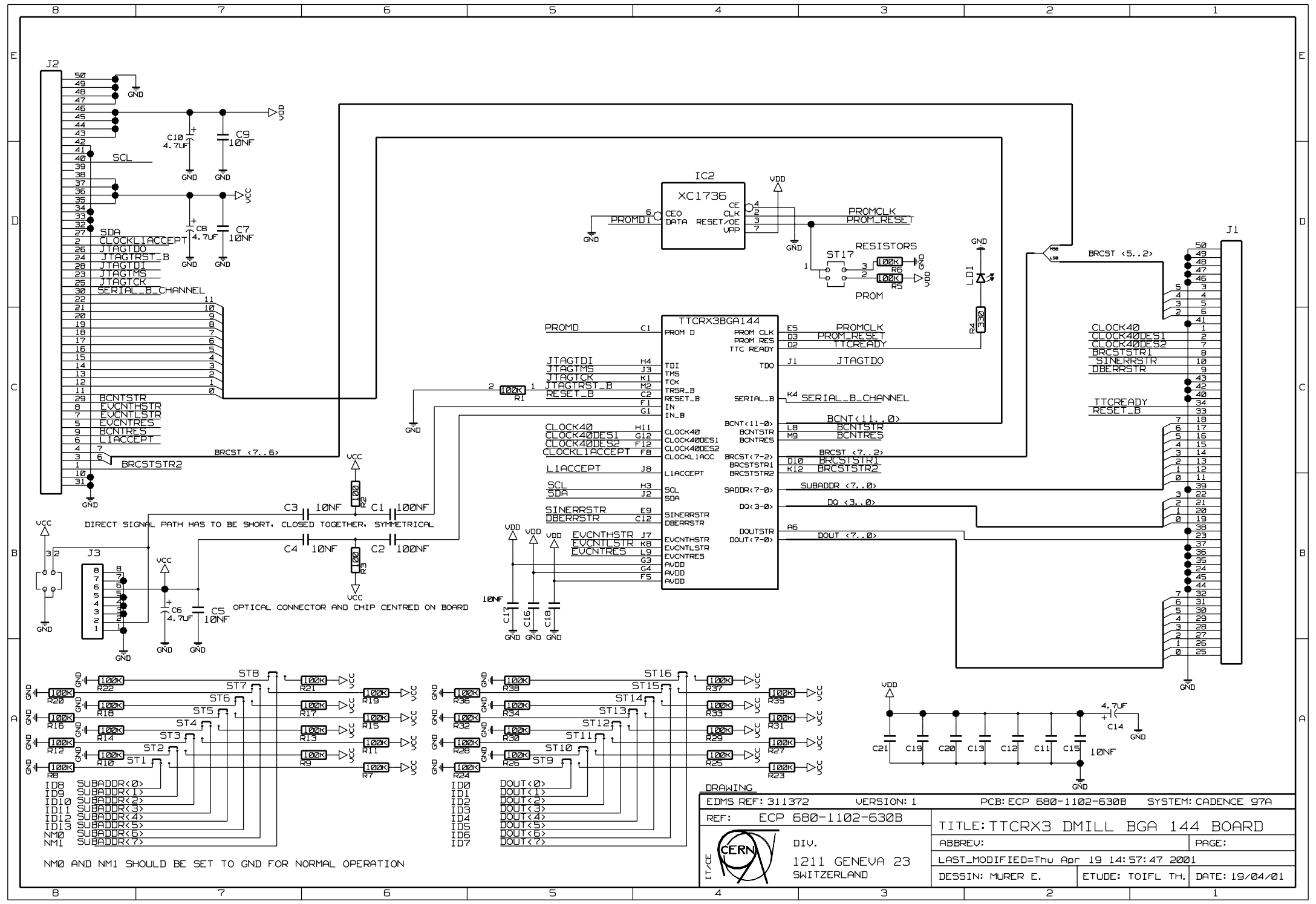
J2
IC2
XC1736
PROMDI
PROMCLK
PROM_RESET
RESISTORS
ST17
PROM
LD1
J1
TTCRX3BGA144
PROM D
PROM CLK
PROM RES
TTC READY
TDO
SERIAL_B
BCNT<11-0>
BCNTSTR
BCNTRES
BRCST<7-2>
BRCSTSTR1
BRCSTSTR2
SADDR<7-0>
DQ<3-0>
DOUTSTR
DOUT<7-0>
TDI
TMS
TCK
TRSR_B
RESET_B
IN
IN_B
CLOCK40
CLOCK40DES1
CLOCK40DES2
CLOCKLIACC
LIACCEPT
SCL
SDA
SINERRSTR
DBERRSTR
EVCNTHSTR
EVCNTLSTR
EVCNTRES
AVDD
BRCST <5..2>
BRCST <7..6>
BRCSTSTR2
SUBADDR <7..0>
DQ <3..0>
DOUT <7..0>
JTAGTDO
SERIAL_B_CHANNEL
TTCREADY
RESET_B
DIRECT SIGNAL PATH HAS TO BE SHORT, CLOSED TOGETHER, SYMETRICAL
OPTICAL CONNECTOR AND CHIP CENTRED ON BOARD
NM0 AND NM1 SHOULD BE SET TO GND FOR NORMAL OPERATION
DRAWING
EDMS REF: 311372
VERSION: 1
PCB: ECP 680-1102-630B
SYSTEM: CADENCE 97A
REF: ECP 680-1102-630B
DIV.
1211 GENEVA 23
SWITZERLAND
TITLE: TTCRX3 DMILL BGA 144 BOARD
ABBREV:
PAGE:
LAST_MODIFIED=Thu Apr 19 14:57:47 2001
DESSIN: MURER E.
ETUDE: TOIFL TH.
DATE: 19/04/01