
Status report on TTCrx chip

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29-601

Conclusions

- ✍ Chip is fully functional after neutron and ? irradiation.
- ✍ Chip itself rather insensitive to SEU
- ✍ Hamming error correction logic works
- ✍ Main problem: Loss of lock in PLL due to charge deposited in the photodiode
 - PLL made more robust in latest run (expected 12/00)

Project short history

- ✍ Several prototypes made in rad-soft technologies
- ✍ Users
 - Several in Atlas and LHC machine
 - Few in other experiments
 - Slow reaction and limited feedback
- ✍ Ported to DMILL in 1999-2000
- ✍ First full version in DMILL fully working Q1 2000
- ✍ SEU tests indicated potential sensitivity to SEU in pin-diode
- ✍ Submission with two versions (almost identical) in Q2 '00

Submissions

- ✍ Engineering run submitted 15/6/2000
 - Two TTXrx-D + small delay line ASIC
- ✍ Received January 2001
- ✍ Unfortunately original BGA package not accessible any longer (too expensive)
- ✍ New package in fpBGA
- ✍ New test set-up developed



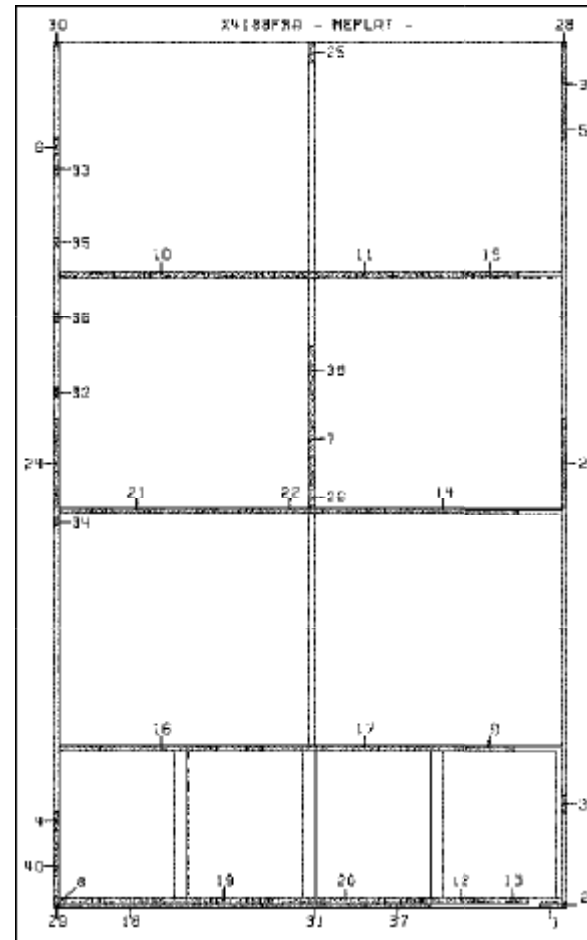
New fpBGA package

- ✍ Good price
- ✍ Good electrical performance
- ✍ Fast service from vendor

Engineering Run: August 2000

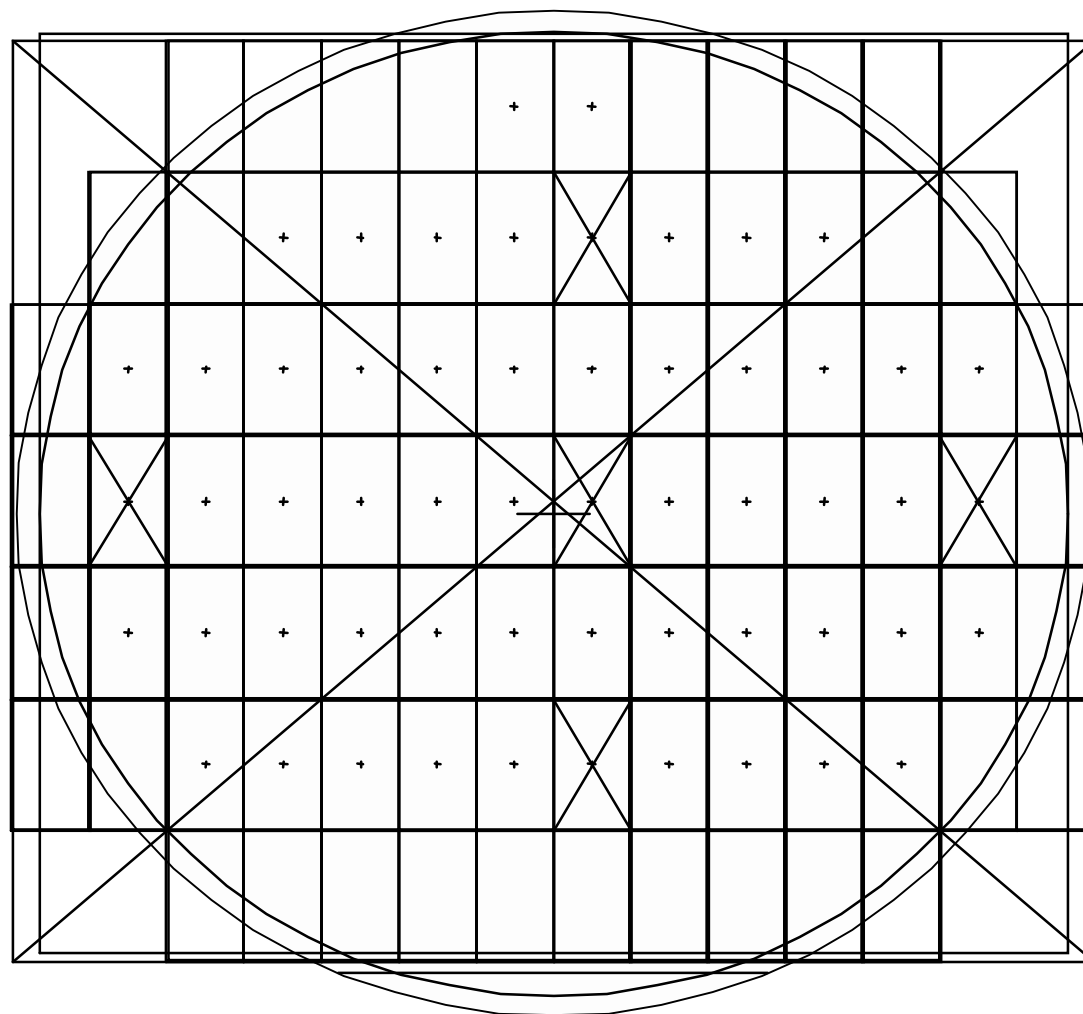
- ✍ Two TTCrx-D versions:
 - Eight wafers in engineering run
 - Version 3.1:
 - » No modifications
 - » Number of ASICs: **1650**
 - » Old test socket: Yield ~75% (tested 208)
 - » New test socket: Yield 80% (tested 480)
 - Version 3.2:
 - » Tolerance to PIN-SEU improved
 - » Number of ASICs: **1550**
 - » Yield ~70% (tested 690, old test socket)

Engineering Run: August 2000



Structure : FLGTX4188FRA
Date : 18 Jul 2000 08:01:33

Engineering Run: August 2000



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TTCrx : Timing, Trigger and Control Receiver ASIC

Meplat

⊗ GD MEASURE SHOTS FOR UV ALARM

Scenario for production

- ✍ A) keep same mask set
 - Too many non-useful chips for Atlas (but could be used by others)
 - Difficulties in dicing and packaging
- ✍ B) optimize mask sets
 - Adapt masks to exact numbers
 - Extra cost to amortize first mask set

How to proceed

- ✍ Establish clear and firm volume needs
- ✍ Compute cost in option A) and B)
- ✍ Organize testing of volume