TIMING,TRIGGER and CONTROL WORKSHOP

Friday, 29 June 2001

General overview and status of TTC components :

TTC beam instrumentation receiver module (TTCbi)

- BI Requirements
- Use of the TTC system
- TTCbi Features
- TTCbi Status.

BI Requirements (What do we want ?)

Evaluation within the context of LHC Tim W.G

> Transmission to all acquisition crates of:

1- Machine Events & Machine Status.
2- Time of day.
3- Beam Synchronous Clock:
   - Bunch Clock (40MHz)
   - Turn Clock (11KHz)
4- Beam Synchronous commands:
   - Injection Warnings.
   - Acquisition triggers.
   - Real time settings.
   - Post Mortem triggers.

> Use a single distribution network.

- Use of the TTC system (How to provide it ?)

- Motivation:
- Can we use an updated LEP BST system for LHC ? > **NO**
  - Profit from RD12 investment.
  - Common system for Experiments & accelerators.
  - Use support facilities.
  - Price < 1000FS / Channel (Without fibers)

  > > Save time & money !

- Implementation:
- **New LHC Beam Synchronous Timing based on T.T.C.**

• Use of the TTC system (How to provide it ?)

- TTC system provides a convenient way of distributing the 40 MHz clock and the Orbit Turn Clock over channel A from the central Prevessin Control Room (PCR) to both the LHC experiments and the beam instrumentation areas around the collider.
- In addition we profit from the TTC's ability to transmit data over channel B, by inserting a so-called BST message, containing commands and parameters that can be broadcast simultaneously to all instruments.
- A BST message consists of 32 long format broadcast commands .

  Long Format : TTCrx ADDR = 0 + 8b SUBADDR + 8b Data

  Use a TTCvi for the message transmission at each Turn Clock.
- A TTC receiver interface for Beam Instrumentation (TTCbi), is being designed to recover the two distributed clocks, decode and store all BST messages and make them available to the front-end controller.

32 Bytes BST MESSAGE Description

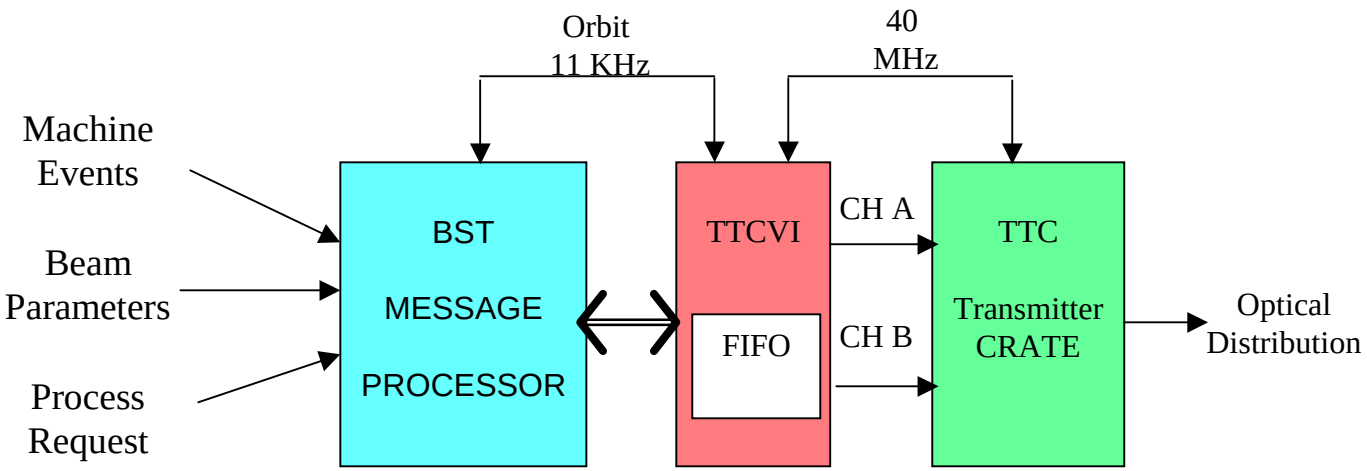
DRAFT

3/5/2001

Bytes	Desc	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
0	Machine Mode	Encoding in one Byte.							
1	Beam Type	Encodting in one Byte.							
2	Beam Energy	High Byte							
3	Beam Energy	Low Byte							
4	Mean Current per Bunch	High Byte							
5	Mean Current per Bunch	Low Byte							
6	Number of Bunches	High Byte							
7	Number of Bunches	Low Byte							
8	Next Batch to Inject	0,1...12							
9	GPS Absolute Time	8 bytes Format ?							
...	....								
16	GPS Absolute Time								
17	Last Tg8 Event	Event Byte							
18	Last Tg8 Event	Extra Tg8 Cycle Info (?)							
19	BI Predefined Tg8 Events	Injection Warning	...						
20	BI Predefined Tg8 Events								
21	Main BI Byte	10 Hz Clock	50 Hz Clock	100 Hz Clock	Capture Trigger	Prepulse	Start Post Mortem	Stop Post Mortem	Warning
22	BI devices dedicated Bytes	One byte for up to 10 types of instrument.							
...	...								
31	BI devices dedicated Bytes								

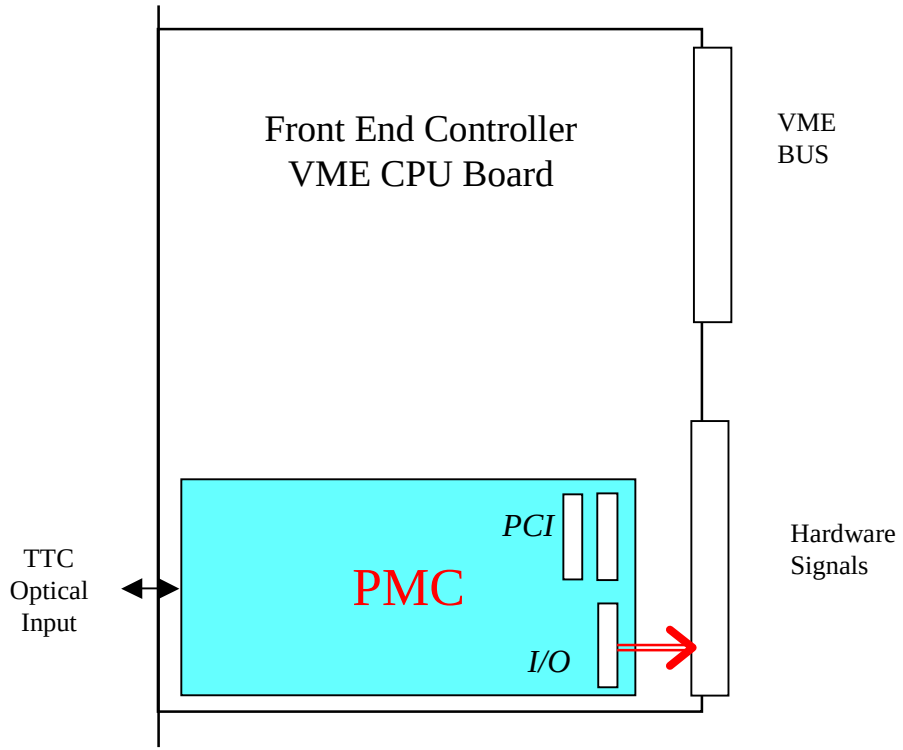
- Use of the TTC system (How to provide it ?)

Message Transmission



- Use of the TTC system (How to provide it ?)

Message Reception > TTCbi



• TTCbi Features

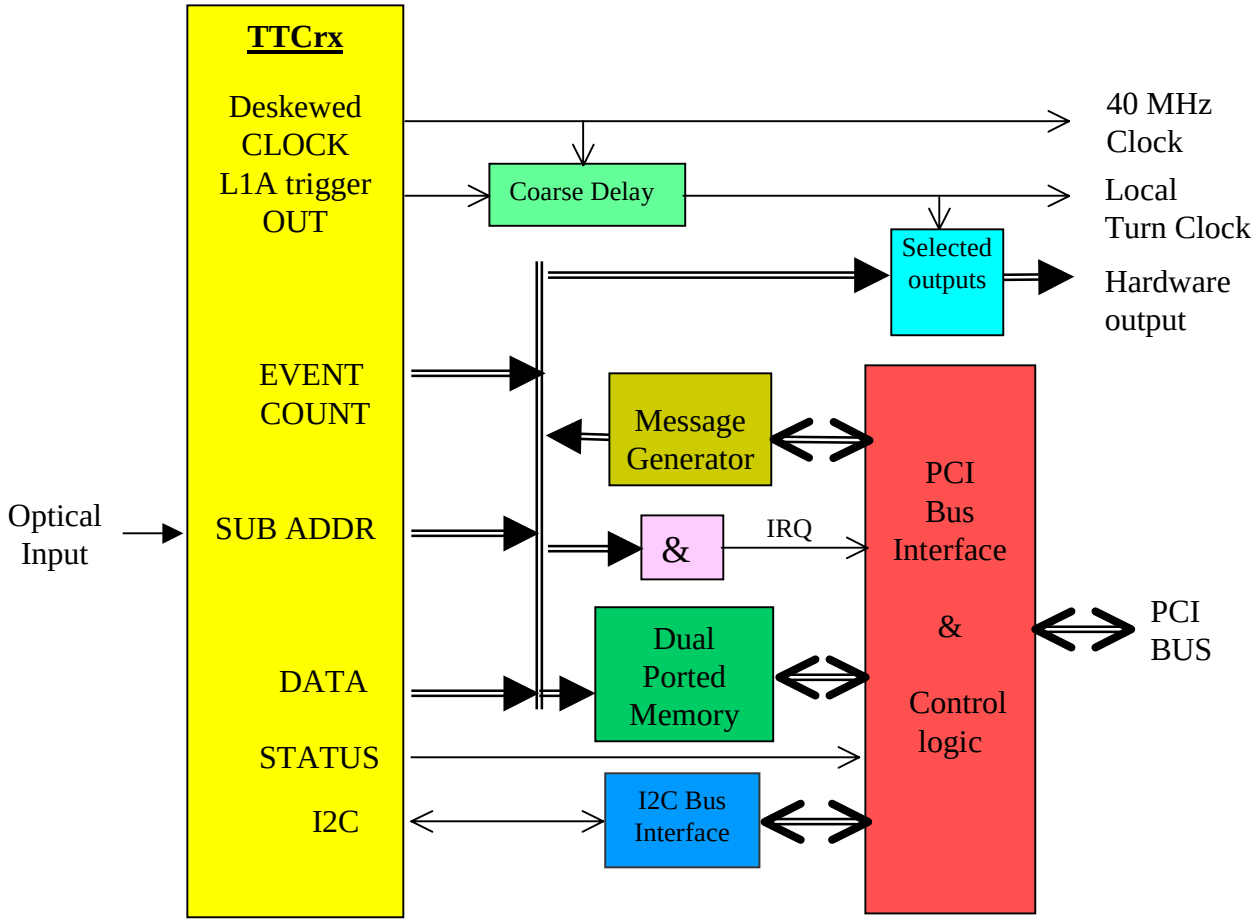
- TTCbi is a PMC slave card IEEE P1386 standard to be plugged onto a motherboard.
- TTCbi can provide LHC Beam Synchronous Timing for both the LHC and SPS .
- Supply the 40 MHz Bunch Clock, which remains synchronous with the bunch structure during all the SPS / LHC beam cycle.
- Supply the Turn clock, corresponding to 1/ 924 of the bunch frequency for SPS or 1 / 3564 for LHC.
- Local delay provides Turn Clock with the appropriate phase relative to the beam structure, taking account of the difference between particle time-of-flight and signal propagation. (0 … 1 Turn)
- The overall jitter of the received clocks anywhere around the rings shall be less than 1ns. (rms.)
- The 2 clocks and two selected Data Bytes among the 32 sub-addresses are routed to an hardware connector. (VME P2)
- All the received commands are stored in a dual ported RAM accessible by the local controller.

• TTCbi Features

- All the TTCrx internal registers are accessible by the local controller via the I2C bus.
- According to the PCI LOCAL BUS Specification, TTCbi uses 256 bytes of config space.
- All control registers and dual-ported RAM are mapped into 256 bytes of PCI space.
- A PCI interrupt request can be generated on reception of a specific message (Mask).
- Local emulator allows the TTCbi module to run in stand alone mode for test in absence of optical input signal.
- Optical Input, main timing signals outputs and indicator leds are on the front panel.
- All output signals are available on a 64 pins PMC I/O connector routed to the I/O connector of VME P2.
- A PMC Connector supplies the following standard power supply from motherboard:
  + 5 V Max 1A ; + 3.3 V Max 1A ; + 12V and - 12v (not used)
- All logic is included inside a FPGA > (can be remotely modified)
- Not intended for radiation environments.
- Cost estimation for production ~ CHF 700.

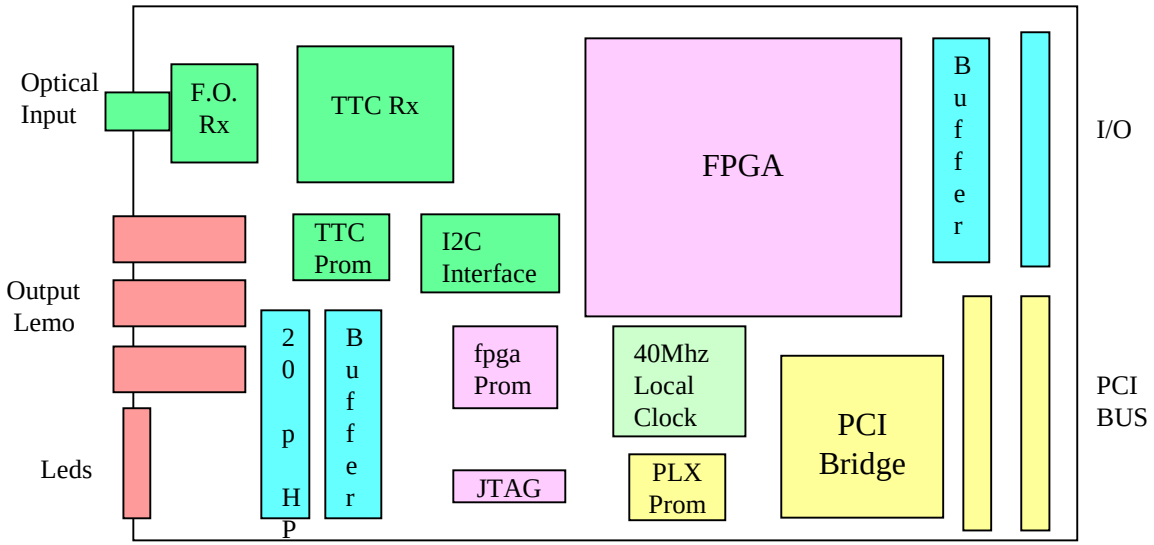
• TTCbi Features

Bloc Diagram



• TTCbi Features

PMC Board



• TTCbi Status.

Specifications; Design; Production; Testing; Delivery schedules…..

- Propose solution within the context of Tim W.G. → … 2000
- TTC Transmission test. "
- TTC vi / BST compatibility test. "
- Project approval (SLTC) (BITB) → 5 / 2001
- 1 st. Prototype : design and test in SPS → 5…11 / 2001
- Final Specifications → 12 / 2001
- 2 nd. Prototype : design and test in SPS → 01...06 / 2002
- Software design → … 2002
- 1 st. batch (50 u.) manufacturing & test → 06…12 / 2002
- 2 nd batch (250 u.) manufacturing & test → 06…12 / 2003

- Issues.

Are there other users for this interface?

(Users could also receive useful messages of machine events and the information about the status of the LHC by using “slow” timing system)

If Yes :

- Could we achieve an agreement on the technical specifications by end 2001. And know the number required by the experiments ?
- Do we need to prepare the technical dossier for the market survey ? (if > CHF 200K)
- Could we have help for organizing the production ?
- Can EP provide maintenance support as for other TTC components ?