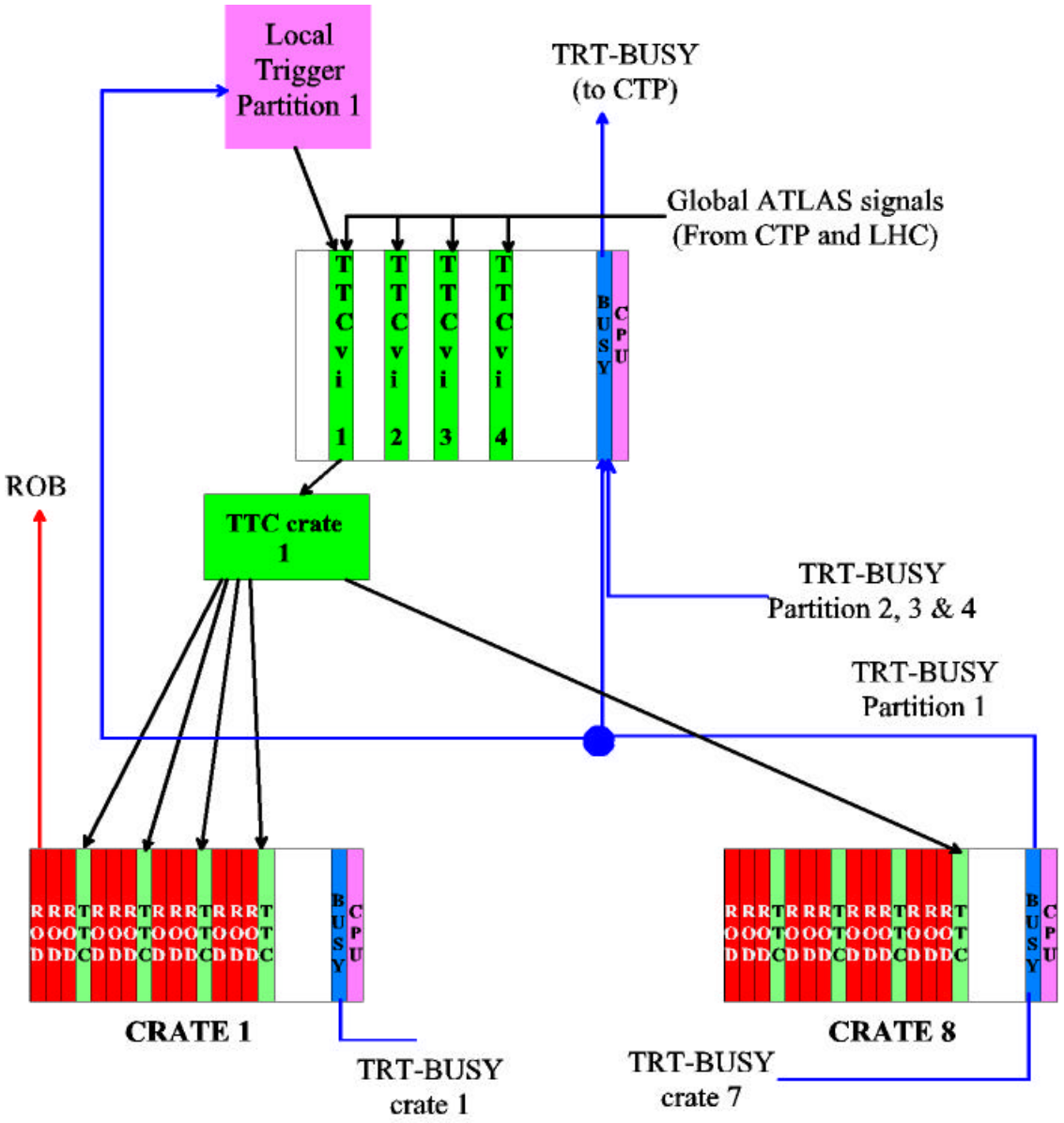
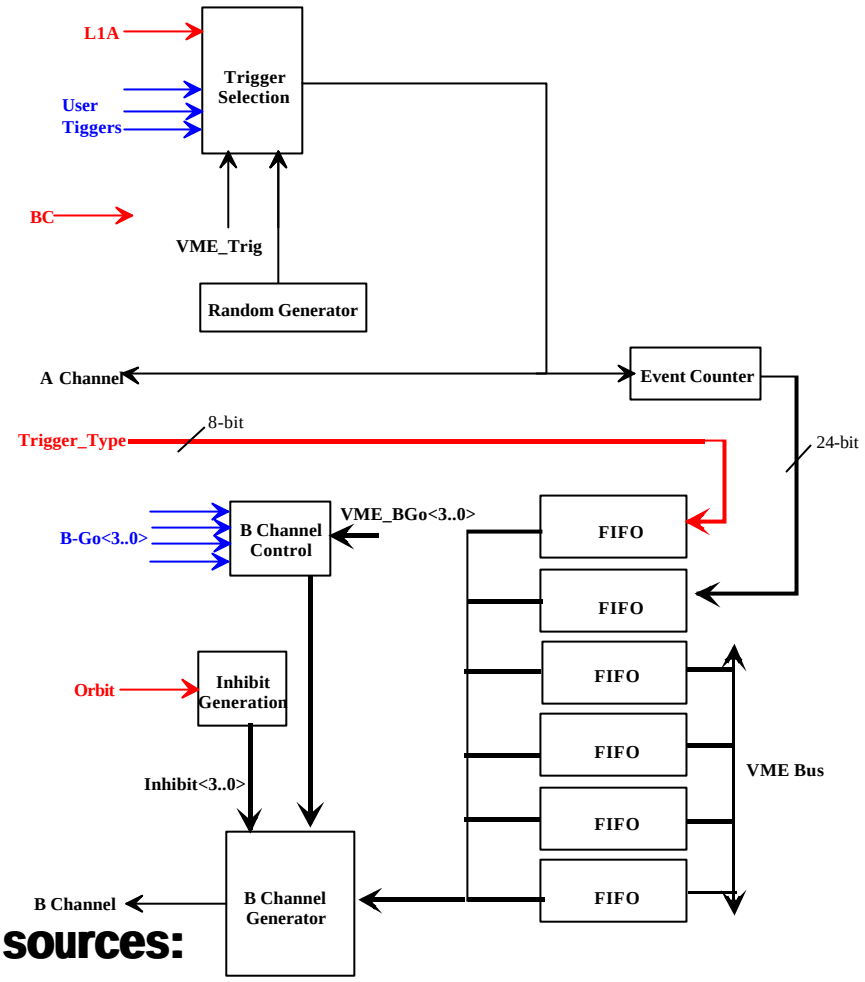
TTCvi - Functionality (1)



- **VME interface providing A- & B-Channels to the modulator**
- **Control one TTC partition**
  - Shall allow to work with the global trigger or with local triggers (test and monitoring)

TTCvi - Functionality (2)



- **Trigger (L1A) sources:**
  - 1 low latency (ECL) from the Central Trigger Processor
  - 3 NIM inputs for
  - VME access
  - Random trigger generator (1 kHz to 100 kHz in 8 steps)
- **Parameter Data/Command**
  - Broadcast or Addressed asynchronous transfer by direct VME access
  - Four 256-word FIFO's containing parameter/commands
    - » Synchronous or asynchronous cycles initiated by external signals (B-GO<1..4>)
    - » Single or repetitive
    - » Precise timing relation with the LHC cycle thanks to Inhibit<1..4> signals

TTCvi - Functionality (3)

- **8-bit trigger word**
  - from the CTP
  - broadcasted (optionally) on the TTC network
  - Differential ECL
- **Internal EvID**
  - broadcasted (optionally) on the TTC network
  - Checking purpose
- **Synchronous transfer for**
  - Bunch Counter Reset: BCR
  - Test pulses
  - Test triggers

TTCvi - Production history

- **Original TTCvi module designed in 1997**
  - 40 modules produced and delivered to users
- **Users requirements survey in 1999**
- **Improved version designed: TTCvi MkII**
  - Taking into account most of the extra requirements
    - » at the exception of some requirements from CMS (increase the # of B-Go)
  - 43 TTCvi MkII modules fabricated

TTCvi - MkII new features

- Internal counting of either the event triggers or the LHC orbit pulses
- Event/orbit-counter may be reset by a VMEbus generated function
- Address, sub-address, size/int/ext bits of the event/orbit-count/trig-type B-channel transfers fully programmable from the VMEbus
- Event/orbit-count/trig-type B-channel transfers may be disabled
- Generation of a delayed calibration TRIGGER triggered by an external pulse on one of the B-Go inputs. The delay is programmable in the same way as the INHIBIT delay
- Command bursts triggered and timed by the Inhibit signal
- Additional LEDs
- Bugs correction

TTCvi - Tests

- **Test bench set-up for testing TTCvi**
- **"TTCvi Test Module" developed**
  - generates all the input signals
  - de-serialises, strips and buffers packages generated on the B-Channel
- **Test software**
  - Per Gallno's version
  - ESS student version

TTCvi - Distribution in the experiments

- **83 modules fabricated**

TTCvi ordered/delivered			
ALICE	10		
ATLAS	32		
CMS	25		
LHCb	6		
LHC Beam I	5		
RD12	3		
EP-Pool	1		
spares	1	***83***	

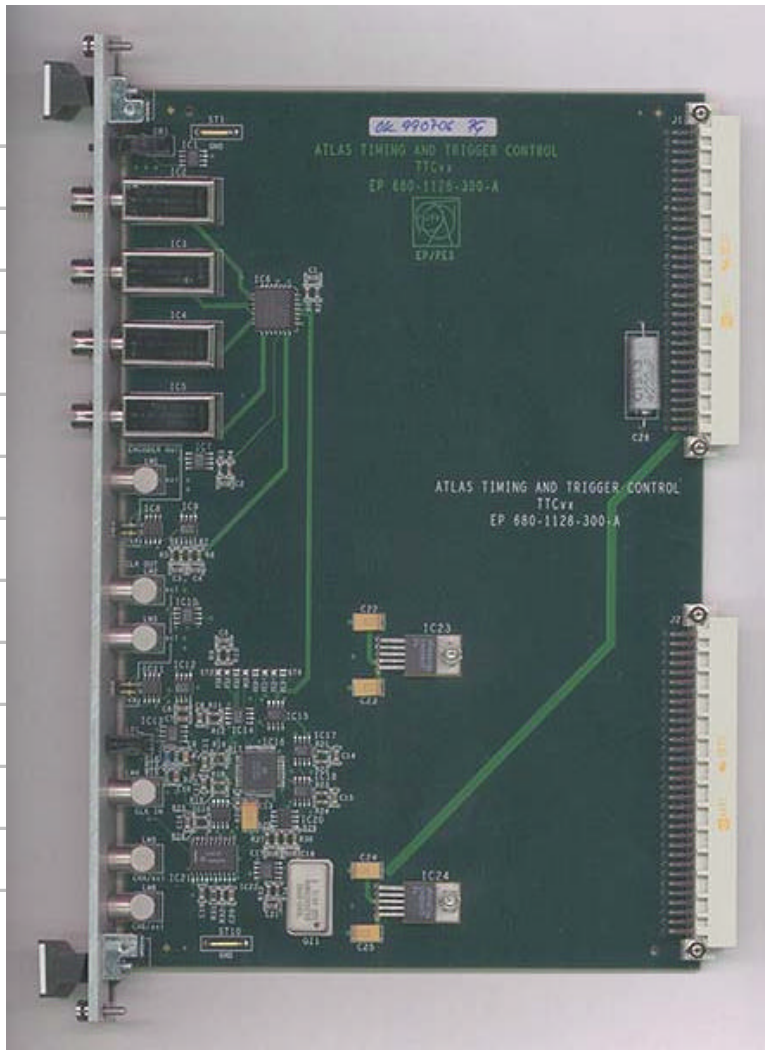
TTCvi - Production

- **Market survey done**
- **Call for tender ready**
  - 1 batch of 100 boards
  - Additional batches of 10 boards
  - Maintenance until 2015
- **Wait for this workshop to finalise the numbers**
- **Modules available in 2002**
- **How shall we fill the gap?**

TTCvx

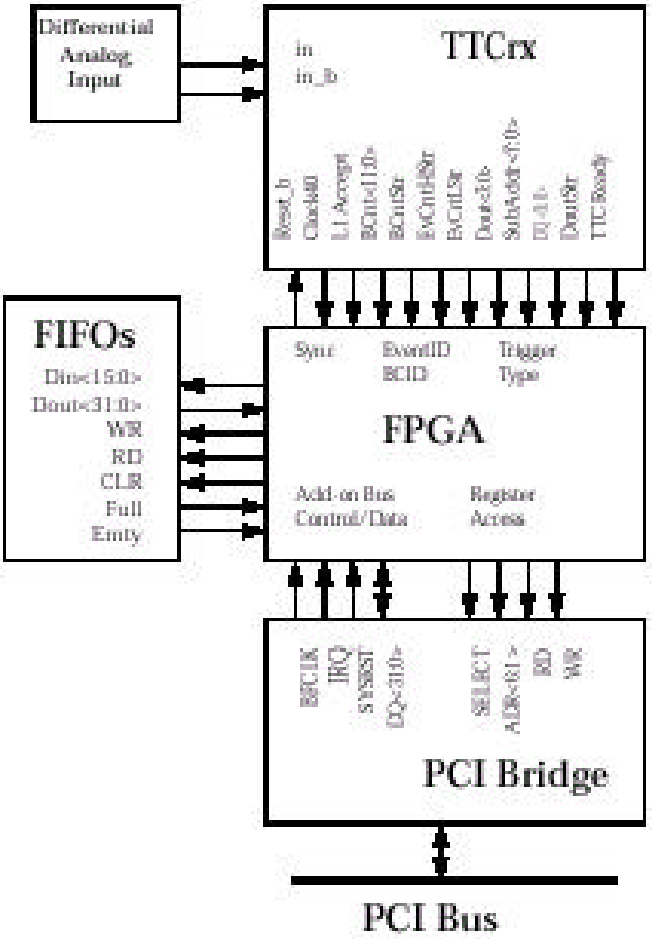
- **Low cost and low power emitter**
- **Production:**

TTCvx ordered/delivered			
ALICE	11		
ATLAS	27		
CMS	27		
COMPASS	6		
LHCb	6		
LHC Beam I	1		
RD12	2		
spares	6	***86***	
in productior	30		



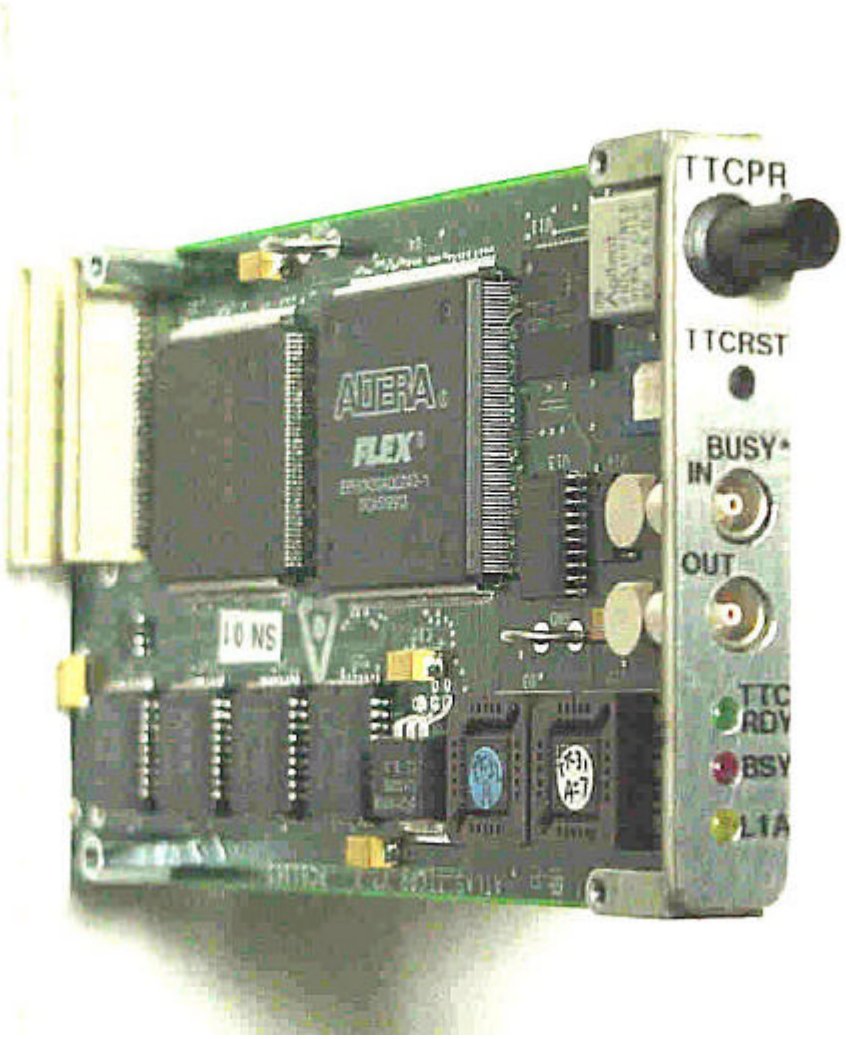
- **Do we need more?**

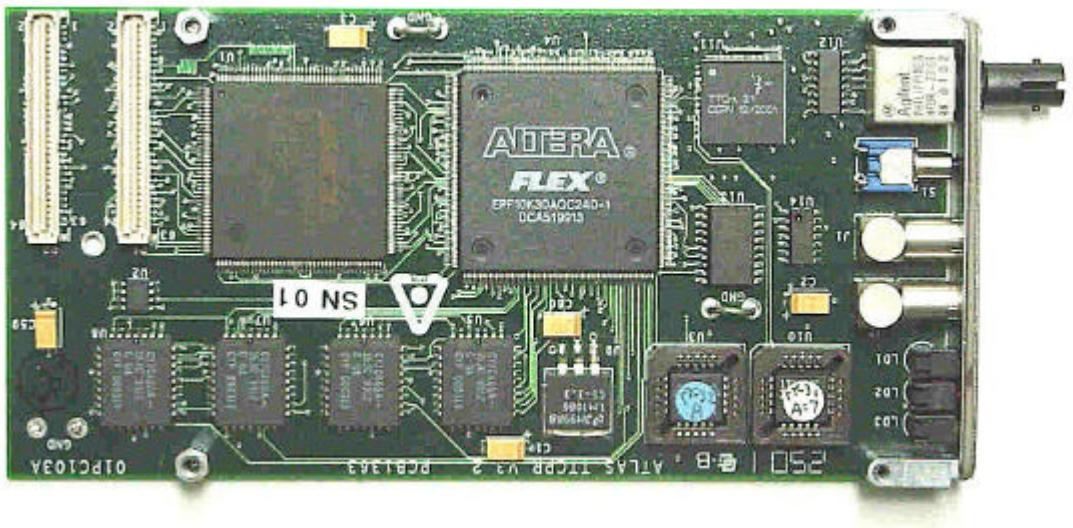
TTCpr (1)



- **TTC destination device (opto + TTCrx)**
- **Stores in FIFO's EVID, BCID and trigger_type received**
- **BUSY signal**
  - set on L1A reception
  - reset with PCI access
- **PCI interface (AMCC 5933 Bridge)**
- **PMC form factor**

TTCpr (2)


TTCPR
TTCRST
BUSY*
IN
OUT
TTC
RDY
BSY
L1A
ALTERA
FLEX
10 NS


ALTERA
FLEX
10 NS