High-Speed Serializer for LHC Gbit/s Links in Radiation Tolerant 0.25mm CMOS Technology

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Outline

- Introduction
- ASIC architecture
- Experimental results
  - Test setup
  - Total dose
  - SEU
- Summary

Introduction

- LHC detectors require Gbit/s links:
  - Sub-detectors ⇔ control/counting room
  - Data readout systems
    - Asynchronous/synchronous data transmission
  - Trigger systems data path
    - Data transmission must be synchronous with the 40.08MHz LHC master clock

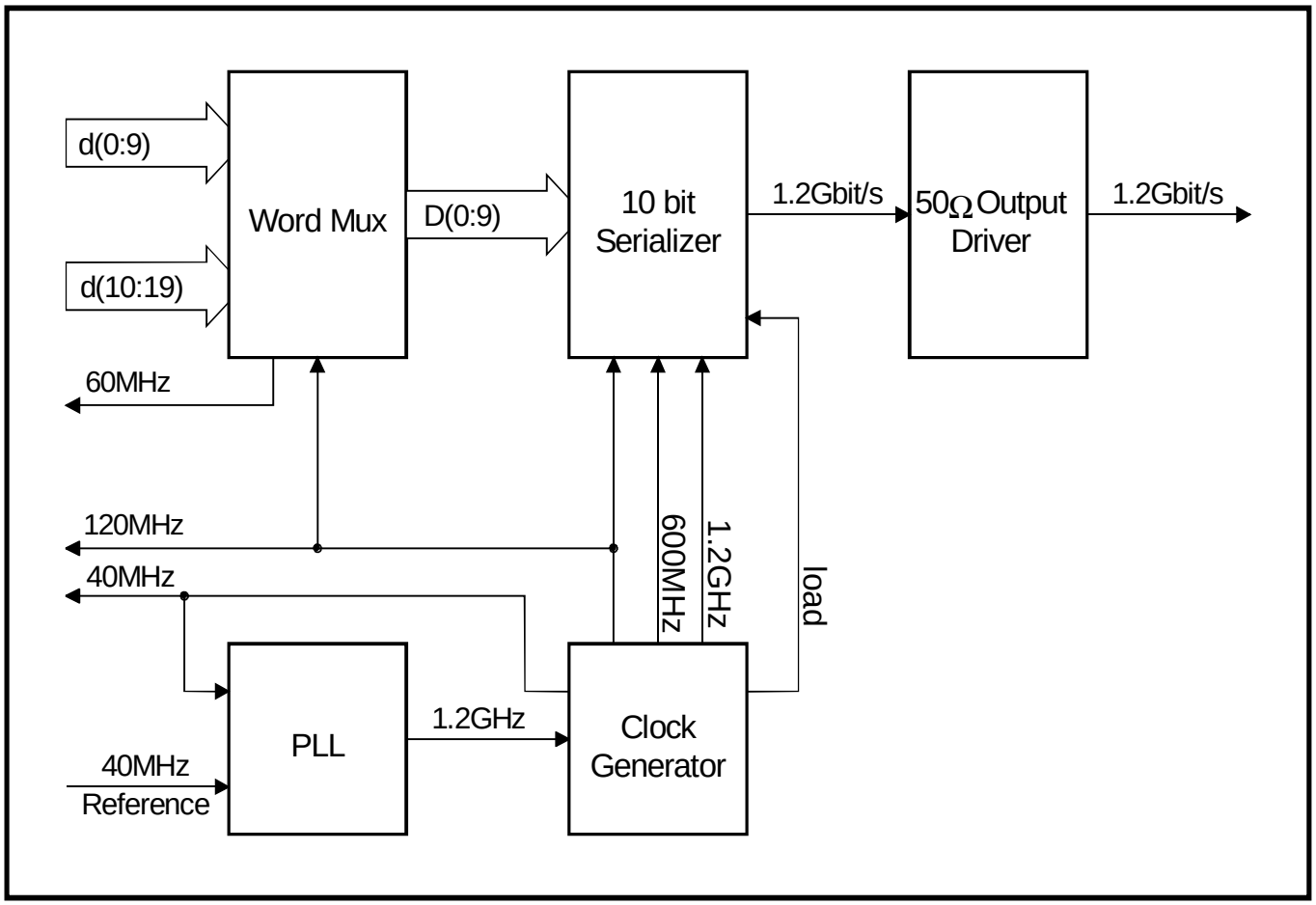
LHC High-Speed Optical Links

- Typical configuration:
  - Unidirectional
- Transmitters inside the detectors:
  - Transmitters subject to high levels of radiation during the experiments lifetime
  - Large numbers $\Rightarrow$ constrained power consumption

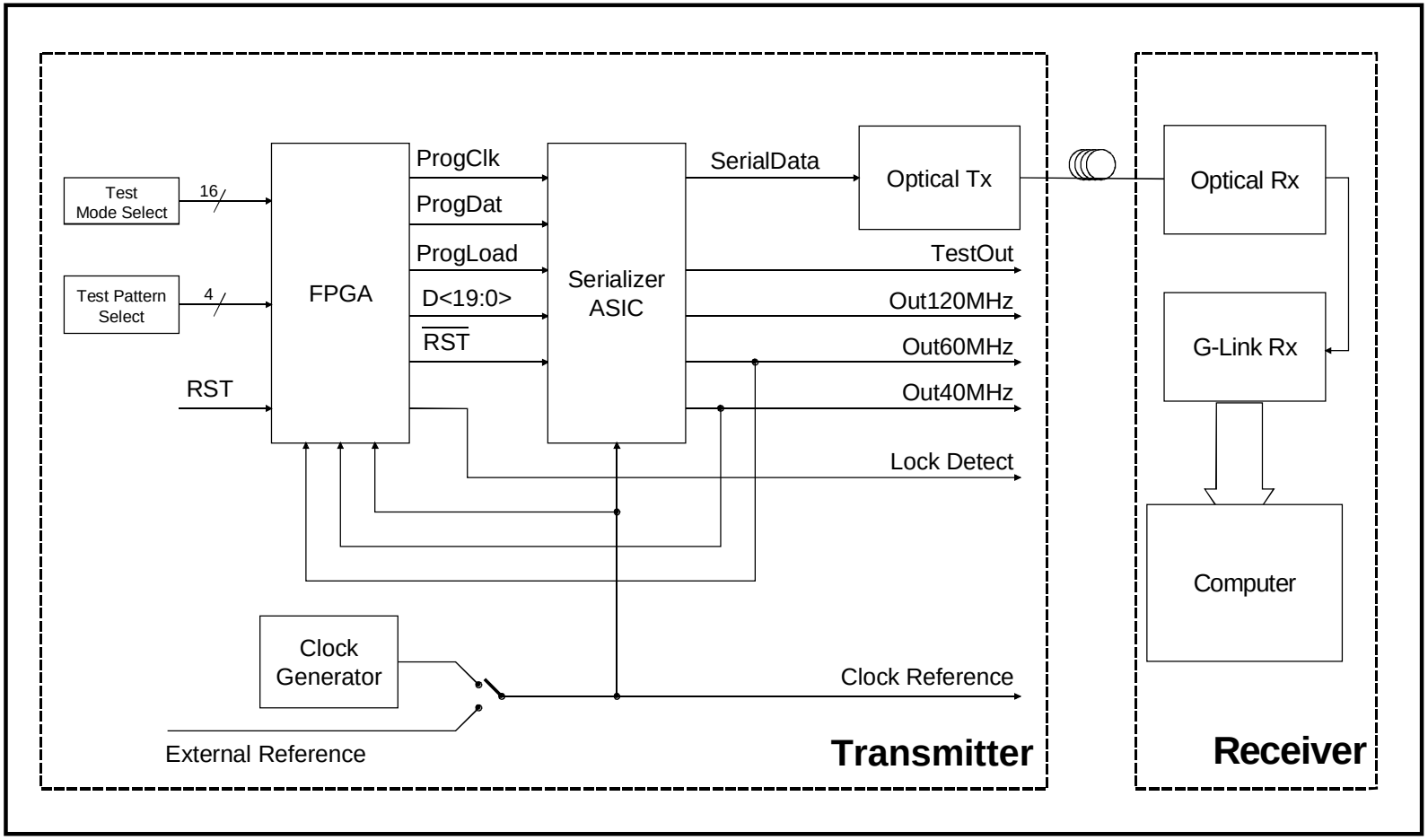
LHC High-Speed Optical Links

- LHC high-speed links requirements:
  - Hardness to total dose radiation effects
  - Operation tolerant to SEU
  - Constant latency transmission for trigger systems (40.08 MHz synchronous)
  - Low power dissipation
  - Low cost

ASIC Architecture

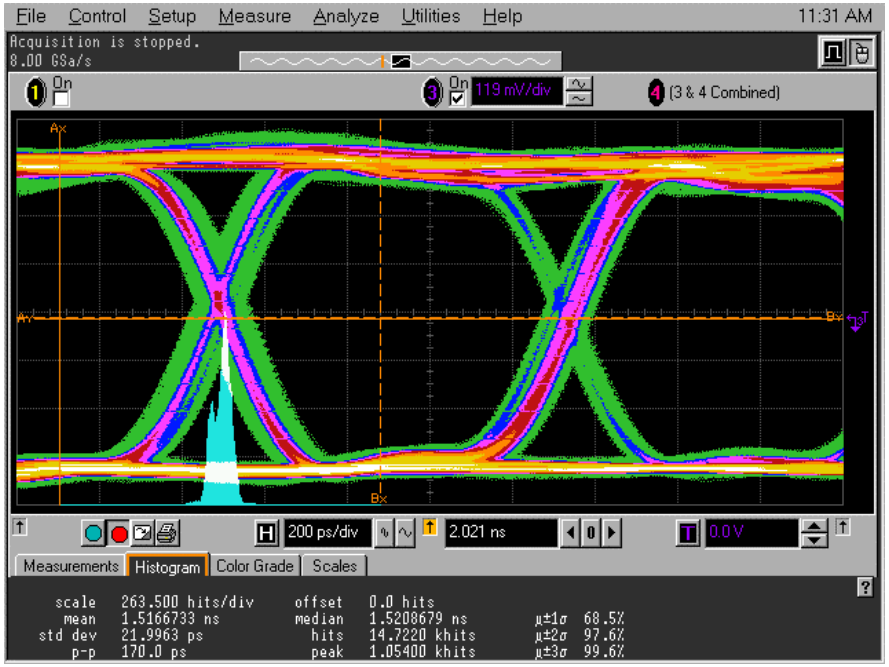


Test-Setup


Test
Mode Select
16
Test Pattern
Select
4
RST
FPGA
ProgClk
ProgDat
ProgLoad
D<19:0>
RST
Serializer
ASIC
SerialData
Optical Tx
TestOut
Out120MHz
Out60MHz
Out40MHz
Lock Detect
Clock
Generator
Clock Reference
External Reference
Transmitter
Optical Rx
G-Link Rx
Computer
Receiver

Total Dose

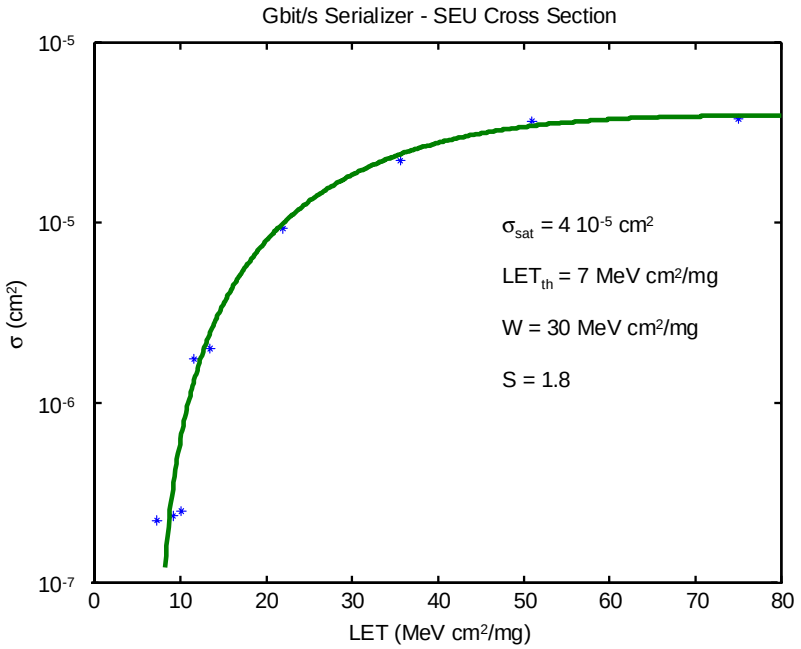
- Total dose 10 Mrad (SiO_2):
  - X-rays 11.7 Krad/min
  - Single irradiation step
- Chips tested before/after irradiation for:
  - Jitter
  - Data transmission errors
- Data transmission:
  - 72 hours of error free data transmission (before/after)
- Cycle-to-cycle Jitter
  - RMS: 22ps
  - P-P: 170ps



Single Event Upsets

- Data transmission under irradiation with heavy ions
- Synchronization loss was the main source of errors:
  - mechanism not clear
  - further simulation and testing necessary
  - LET_{th} = 7 MeV cm^2/mg

    σ_{sat} = 4 10^{-5} cm^2
  - No errors observed for:
    - LET_{th} = 6.2 MeV cm^2/mg ! (fluence 9 10^6 ions)
    - Did we wait long enough ?



Single Event Upsets

- Can we extrapolate for LHC?

CMS Environment	Pixel R = 4 – 20cm	Endcap ECAL R = 50 – 130cm	Tracker R = 65-120cm	Cavern R = 700 – 1200cm
Error/(chip hour)	$1.4\ 10^{-2}$	$1.9\ 10^{-4}$	$8.4\ 10^{-5}$	$3.1\ 10^{-8}$
#chips for one error each hour!	71	5.3K	12K	32M

- Values calculated assuming $1\mu m^3$ sensitive volume:
  - For the technology used the sensitive volume is probably smaller
  - The correct error rate estimate should be 2 to 4 times higher
- No SEU “robust” circuit techniques where used in the design!

Summary

- A 1.2Gbit/s data serializer has been fabricated
  - In 0.25μm CMOS
  - Using radiation tolerant layout
- The ASIC was tested for:
  - Functionality
  - Total dose irradiation
  - Single Event Upsets
- Consequences of operating the ASIC in different LHC environments were estimated