AN APPLICATION OF S-LINK, A DATA LINK INTERFACE SPECIFICATION, IN THE ATLAS READOUT SYSTEM

R.A. McLaren, H.C. van der Bij, *ECP Division, CERN, CH-1211 Geneva 23*
and
O. Boyle, *Edinburgh University, Mayfield Road, Edinburgh EH9 3JZ*
and
G. Rubin, *RMKI, PO-Box 49, H-1525 Budapest*

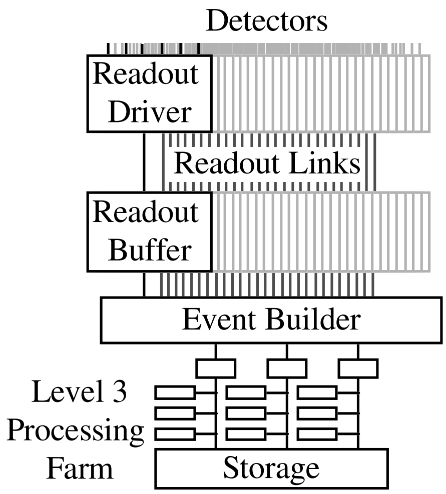
ABSTRACT

In the ATLAS readout system there is a provisional requirement for two thousand data links between the Readout Drivers and the Readout Buffers. Current evaluations call for data transfer at 1 Gb/s over distances, for some detectors, of 200 metres. There is a strong motivation to adopt a standard link that would allow common Readout Buffers for all detectors but, given the LHC time-scale, it is premature to choose a technology in which to implement the links.

The S-LINK concept is currently being studied as an option that would provide the benefits of standardisation without the limitations. The S-LINK specification defines, at both ends of the link, a simple FIFO-like user interface that remains independent of the technology used to realise the physical link. The physical link provides transfer of event data and control words, error detection, optional flow control and test facilities. This paper describes the S-LINK interface specification, the use of the S-LINK in ATLAS, the physical links being designed, and the test equipment that has been developed.

1. Introduction

The ATLAS[1] detectors are grouped into 3 sub-detectors. These are the Inner Tracker, the Calorimeter and the Muon Detectors. Data from these detectors is collected by the Front-end modules where it is buffered until a LVL1 accept is received. The accepted data is then transmitted to the Readout Drivers where the input streams are multiplexed into one Readout Link. Each Readout Link is connected to a Readout Buffer that stores the event fragments until it receives a LVL2 accept whereupon the event fragments for a single event are concatenated or “built” into one event. This event is then processed by the LVL3 farm before being stored.



Distances are important as they determine the choice between electrical or optical transmission. The distance between the Front end modules, which are on the detector, and the Readout Drivers vary between detectors. Some Readout Drivers are close to the detector and others will be installed in USA15, an underground cavern situated 80 metres from the detector. USA15 is approximately 100 metres below the surface and this determines the length of the Readout links. Once on the surface there will be a computer room environment with distances between equipment of the order of 10 to 20 metres.

Estimates of the number of Readout Links from the detector and trigger sub-systems to the Readout Buffer are shown in the table below.

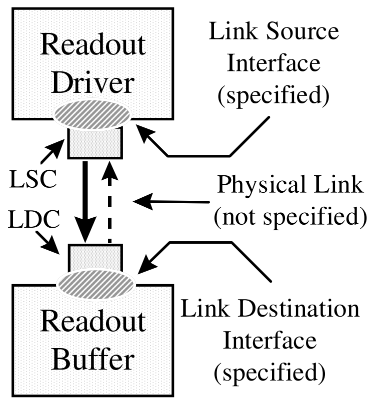
Sub-detector	**Number of Readout Links**
Pixel Detector	150 - 200 @ 1 Gb/s
Semi-Conductor Tracker	250 - 450 @ 1 Gb/s
Transition Radiation Detector	256 - 512 @ 1 Gb/s
Calorimeter	500 @ 1 Gb/s
Muon Detector	300 @ 1 Gb/s
LVL1 Trigger	20-30 @ 1 Gb/s
LVL2 Trigger	1 @ 1 Gb/s

The front end modules are grouped in such a way as to limit the output bandwidth of the Readout Driver to 1 Gb/s This translates to a 32-bit word at 33 MHz which is easy to achieve using modern electronics. In addition several standards, for example HIPPI and Fibre Channel, run at this rate so no special developments should be required for serialisation and optical components. In addition to data from the detectors, both the LVL1 and LVL2 triggers will send data to the Readout Buffers.

Cost is a key issue. Presently, there are plans to use between 1000 and 2000 Readout Links. The cost of these links will include the logic required to format the data, the conversion to optical, the connectors and the patch panels at each end of the link plus 2*200 metres of optical fibre per link. Comparing current prices with those of similar installations at LEP has shown that electronic component prices have dropped by a factor of ten. Clearly if we define today the technology that will be used in the ATLAS Readout Links, we will be unable to benefit from future cost reductions.

The advantages of cost savings that can be achieved by waiting and the desire for a common standard have to be balanced with the requirements of the detector designers who wish to start tests in the relatively near future. For example the Muon Drift Tube Chambers may be ready to start tests at the end of 1997. Whilst tests could be done locally, without a Readout Link, these would not test the integration into the overall readout architecture. There is therefore a desire to integrate into the DAQ system for at least some of the tests.

On the basis of these conflicting requirements we have defined the S-LINK specification[2]. The S-LINK data link interface specification defines the Link Source Interface and the Link Destination Interface, but not the physical link. In this way various implementations of S-LINK, including electrical and optical, can be developed using new technologies without changing the design of the Readout Drivers or Readout Buffers. For ease of use, both Source and Destination interfaces are closely modelled on a synchronous FIFO: transmitting data is like writing to a FIFO while receiving data looks like the link is writing to a FIFO in the Readout Buffer.

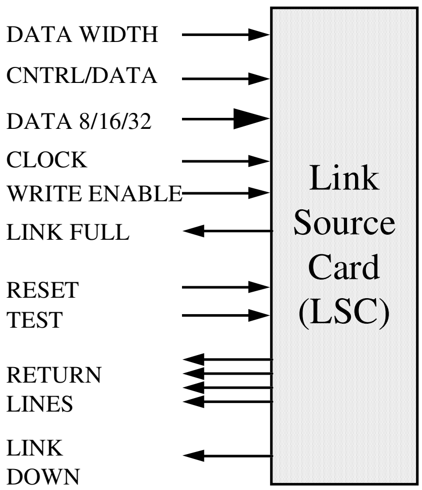


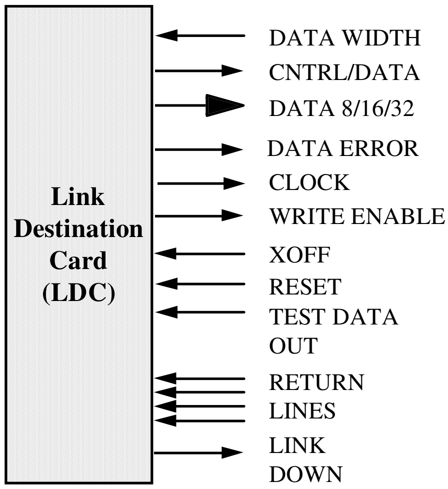
2. S-LINK mechanics

To allow different physical implementations of the S-LINK, the S-LINK specification recommends the use of small daughter boards in the format of the Common Mezzanine Card standard. (This is the same format as used by the PCI Mezzanine Card.) A single, high density, 64-pin connector connects the Readout Driver to the Link Source Card (LSC) and the Link Destination Card (LDC) to the Readout Buffer.

3. S-LINK basics

The Readout Driver's view of the S-LINK starts with two lines that can be used to select the DATA WIDTH. These should be set to 32 bit for the Readout Driver to Readout Buffer link. The CNTRL/DATA line allows the user to define the start and end of event fragments. DATA is a 32-bit word that must respect the set-up and hold times with respect to the CLOCK signal. DATA will only be written when WRITE ENABLE is active. LINK FULL is generated when the Readout Buffer can no longer accept data and this should cause the Readout Driver to suspend the data transfers. RESET is used to set the link in a known state. When TEST is asserted the LSC enters the test mode and generates a predefined data pattern. At the other end of the link the LDC recognises the test mode and begins checking the incoming data words. Return lines allow the Readout Buffer to send a few user defined control signals back to the Readout Driver. Finally, the LINK DOWN signal is asserted when there is a major problem with the link, for example no light in the fibre.





The signals arriving at the Readout Buffer are almost a copy of those transmitted at the Readout Driver. The data width lines are again set to receive 32 bits of data. The CNTRL/DATA bit informs the Readout Buffer if the DATA received is the start/end-of-event or just plain data. DATA ERROR is asserted if an error has taken place during the transfer, either on a word, or on an event. The DATA word is presented synchronously with CLOCK and WRITE ENABLE. XOFF is used by the Readout Buffer to indicate that it can no longer accept data. RESET initialises the link and TEST DATA OUT allows the data generated in test mode to be output on the DATA lines. The RETURN LINES are used to send control bits back to the Readout Driver and the LINK DOWN indicates a serious problem on the S-LINK.

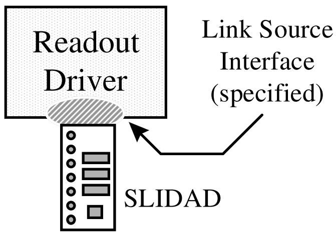
4. The Data Format

The specification of a common hardware interface for the output of the Readout Drivers is only part of the solution. It is also necessary to define a format for the event fragments that is common to all receiving Readout Buffers. An example of a possible format is shown in the adjacent table and is presently being discussed within ATLAS. The event block starts with a fixed header, has a variable number of STATUS and DATA words and has a fixed trailer. The beginning and end of the block are CONTROL words which enables the Readout Buffer to recognise the start and end of events and to re-synchronise in case of an error.

CONTENT	TYPE
START_OF_BLOCK_TYPE N	**LCW**
FORMAT_VERSION_NUMBER	LDW
RESERVED	LDW
ROD_L1ID	LDW
ROD_BCID	LDW
ROD_MODULE_ID	LDW
TRIGGER TYPE	LDW
STATUS_WORD	LDW
STATUS_WORD	LDW
•	LDW
•	LDW
DATA_WORD	LDW
DATA_WORD	LDW
•	LDW
•	LDW
RESERVED	
NO_ OF_STATUS_WORDS	LDW
NO_OF_DATA_WORDS	LDW
END_OF_BLOCK_TYPE N (INCL. LINK ERROR SUMMARY)	**LCW**

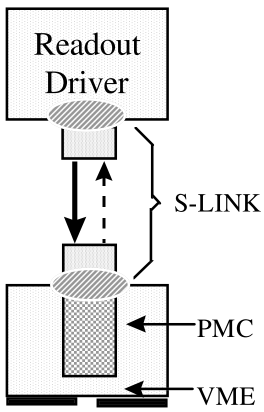
5. S-LINK test equipment and interfaces

When testing links one of the main problems is the amount of hardware and software that must be assembled to test the simplest function. Typically to test any part of the link, it is required to have a data transmitter, a physical link to transfer the data and a data receiver. In addition software is usually required to provide a user interface to allow the user to choose data size and content, to start/stop the transfer and to check/display any errors. Often more effort is spent setting up this complex chain than in checking the link hardware.



To help designers of the Readout Drivers and the Readout Buffers test S-LINK interfaces, two boards are being built, a dummy destination and a dummy source. The dummy destination, SLIDAD, replaces the Link Source Card (LSC) using the same connector. Words written to the link are displayed on LEDs with a single step function. Logic state analyser connections are provided for measurements at full speed. The reaction of Readout Driver logic to signals from the link, for example XOFF, can also be verified. At the Readout Buffer a similar module, SLIDAS, can emulate an S-LINK input by generating predefined event blocks or data blocks, including blocks containing errors. To further help designers, there is an implementation guide and VHDL models of the LSC and LDC.

Once the basic functions of the Readout Driver have been tested, the Readout Driver designer would normally like to read the data via VMEbus. The recommended method is to use a VMEbus processor board with a PCI Mezzanine Card (PMC) site, for example a Motorola MVME1600 or a CES RIO2 8060. An S-LINK to PMC card has been built for this purpose and test program has been written under LynxOS. An S-LINK library is also being written for the DAQ Prototype-1 project. The S-LINK to PMC interface has a maximum transfer rate of 65 MB/sec. A PMC to S-LINK interface also exists.



6. Link Source and Destination cards

The design and development of the test equipment and interfaces has been done at CERN. The design of the link cards has taken place outside CERN. Five separate developments are ongoing based on different technologies. These are shown below;

Institute	Medium	Technology	Speed	Status
RMKI, Budapest[3]	Serial Fibre	Fibre Channel	103 MB/s	Under test
INFN Rome	Serial optical	MATCH	100 MB/s	Being built
Univ.of Stockholm	Parallel optical	OPTOBUS	150 MB/s	Under test
KEK, Tsukuba, Japan	Serial electrical	G-LINK	125 MB/s	Under test
INP, Cracow	Parallel electrical	LVDS	50 MB/s	Being built

7. Commercial availability and further information

The S-LINK to PMC, the PMC to S-LINK, SLIDAD and SLIBOX modules are available from INCAA[4]. It is planned to commercialise the physical S-LINKs as they become available. For further information, including the specification, hardware/software documentation, status and other applications in ATLAS please refer to the S-LINK WWW homepage at http://www.cern.ch/hsi/s-link.

8. Conclusion

A specification for a data link interface has been written together with a definition of a data format. For the next few years, this will be the de-facto standard for the ATLAS Readout Link. The specification should allow Readout Links with different technologies to be implemented independently of the design of the Readout Driver and Buffers. Test features and equipment are available to Readout Driver and Buffer designers. Interfaces and software exist to allow readout via VMEbus. A range of physical links to cover different user requirements is being built.

9. Acknowledgements

The authors would like to thank the many members of the ATLAS experiment that have helped shape the S-LINK specification and to thank especially Nick Ellis, Philippe Farthouat, Livio Mapelli and Michal Turala for their support and encouragement.

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[1] ATLAS Technical Proposal, *CERN/LHCC/94-43, LHCC/P2*, 15 December 1994, ISBN 92-9083-067-0

[2] H.C. van der Bij et al., “S-LINK, A DATA LINK INTERFACE SPECIFICATION FOR THE LHC ERA”, *Presented at the 1996 Nuclear Science Symposium, Anaheim, CA, USA*, November 3-9, 1996.

[3] G. Rubin et al., “Development of FCS-Link Interface Cards”, Presented at the Second Workshop on Electronics for LHC, Balatonfüred, Hungary, 23-27 September 1996.

[4] INCAA Computers, http://www.universal.nl/incaa