Phase 2 Tracker Upgrade(2.1)

1. Limitations of the CMS Tracker

① The present Outer Tracker was designed to operate without any loss of efficiency up to an integrated luminosity of 500 fb^{-1}, and an average pile-up (PU) of less than 50 collisions per bunch crossing.

② The pixel detector will be replaced with the "Phase-1" upgrade during the Extended Technical Stop at the end of 2016, when the total integrated luminosity is assumed to reach about 150 fb^{-1}.

③ the Phase-1 tracking detectors restrict the CMS Data Acquisition to a maximum Level-1 (L1) accept rate of about 100 KHz, with an available latency of 4 μs for the trigger decision. Operation at high luminosity requires a substantial upgrade of the trigger system, with significantly higher rate and longer latency.

④ Accumulated radiation damage in the pixel sensors reduces the charge collection as well as the Lorentz angle, leading to lower charge sharing among neighboring pixels and hence worse spatial resolution. A worse hit resolution directly translates to degraded precision in primary vertex reconstruction, track impact parameter resolution and b-tagging performance.

⑤ After 500 fb^{-1} the aging model predicts an impact parameter degradation of more than 50% while the longitudinal impact parameter resolution degrades by a factor of two.

⑥ For a PU of 140, bandwidth limitations in the readout electronics would lead to an irreducible data loss of approximately 7% in the first pixel barrel layer, which is the crucial layer for primary and secondary vertexing.

⑦ For the Outer Tracker, the most prominent consequence of irradiation is the increase of leakage current, which can be mitigated by lowering the operating temperature of the cooling system to achieve a lower silicon sensor temperature.

⑧ The evolution of the leakage current of the tracker sensors is predicted by a detailed model that takes into account the estimated luminosity profile, the position and size of each module, the expected particle fluence at specific module locations and the expected temperature versus time scenario that includes annealing(降溫 退火) periods. The model also implements a map of the efficiency of the module thermal contacts derived from data.

- Map of non-functional modules (in blue) after an integrated luminosity of 1000 fb^{-1}, for the achievable minimum coolant temperature of −20℃. Almost all the stereo modules in the barrel, as well as in the End-Cap are no longer operational.
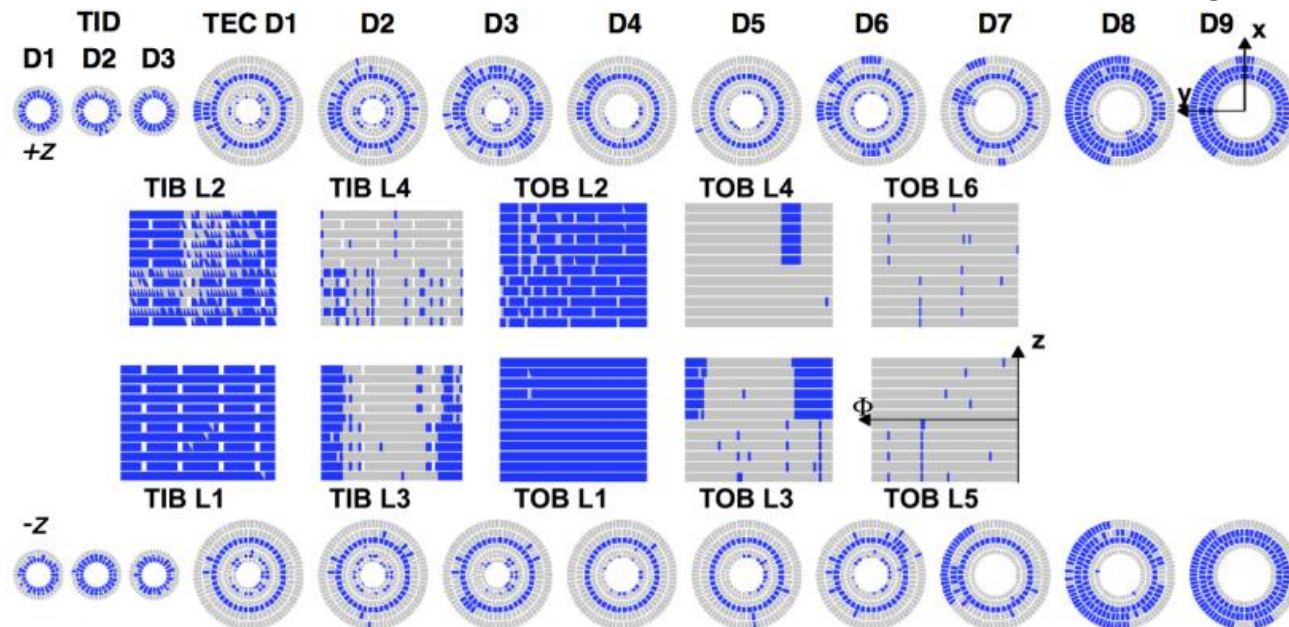
- The loss of hits on many layers of the tracker results in a significant degradation of track reconstruction performance. Within |η| < 2.4, the track finding efficiency for $p_T = 10 GeV$ muons decreases from 100% for the strip tracker without aging at 50 PU to 75 − 95% after 1000 fb^{-1} at 140 PU. The efficiency for tracks from $t\bar{t}$ events with $p_T > 0.9 GeV$ drops from above 85 − 95% to 50 − 80%, while the single track fake rate increases from less than 5% to 12 − 45%. Reducing the fake rate can only be achieved by requiring more hits on each track, thereby further reducing the efficiency for finding real tracks. (t̄t events?)(3.5cm is the interaction region in the transverse direction)
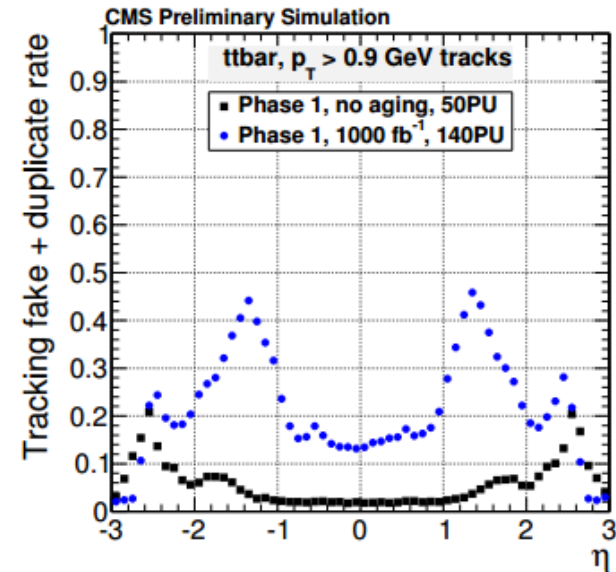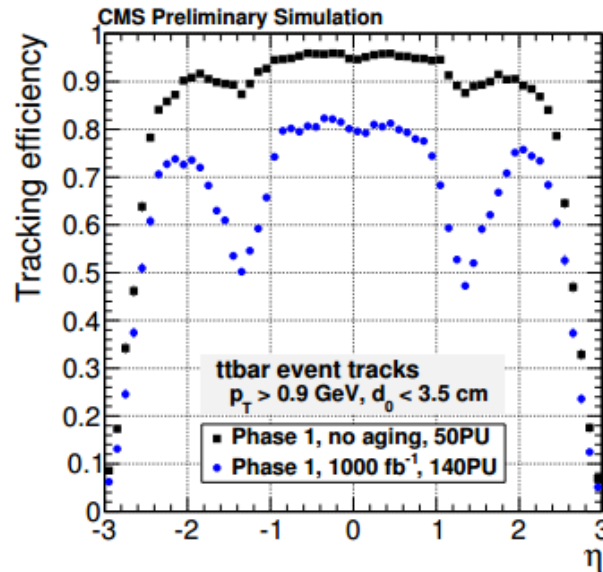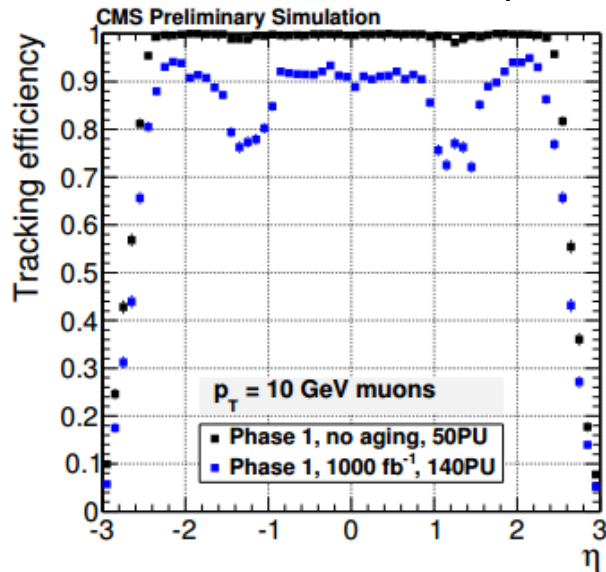
⑨ The efficiency loss decreases the physics reach of most searches for new physics, diminishes the effectiveness of high-p_T lepton isolation criteria, and degrades jet energy and missing transverse energy (MET) resolution. Fake tracks cause biases and resolution degradation in jet energy measurements, increase background levels, and adversely affect high-p_T lepton isolation criteria.

⑩ the track finding efficiency progressively decreases at very low momentum. For $p_T < 0.9\,\mathrm{GeV}$ the performance degradation in the aged detector is even larger, with the fake rate reaching close to 70% in the rapidity regions around |η| = 1.5.

- Left: map of the expected particle fluence in the Tracker volume corresponding to an integrated luminosity of 3000 fb^{-1} , expressed in terms of 1 MeV neutron equivalent fluence.
- Right: detail of the fluence in the pixel volume. The expected fluence has a strong dependence on radius, while it is almost independent of the z coordinate.
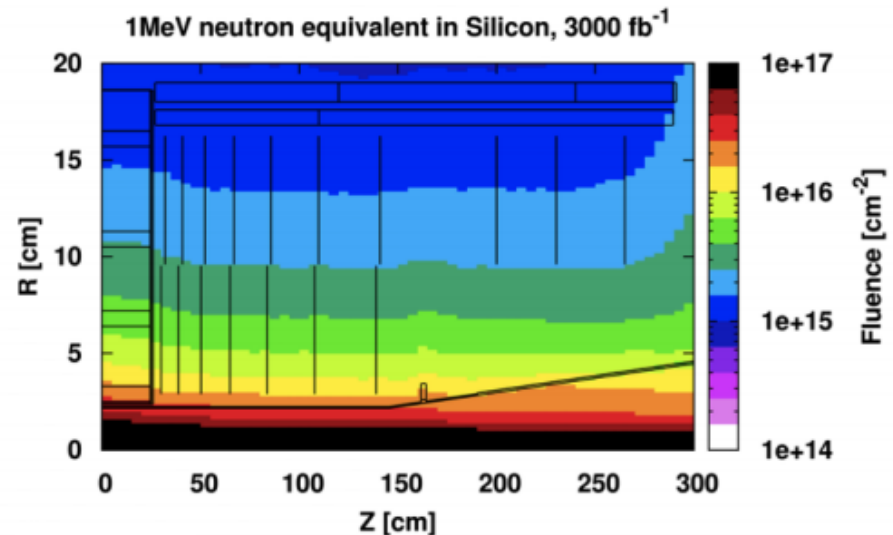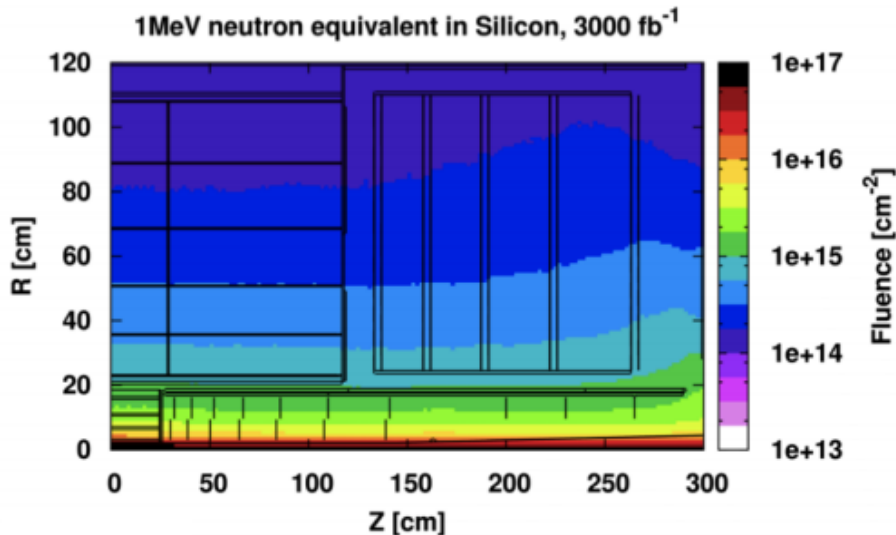
2. Requirements for the Tracker Upgrade

① Radiation tolerance : The upgraded Tracker must be able to operate efficiently up to an integrated luminosity of 3000 fb−1. The expected particle fluences that must be tolerated are shown in the figure in page 4. This requirement must be fulfilled without any maintenance intervention for the Outer Tracker, while for the Pixel detector it is envisaged to keep the present concept of easy accessibility, offering the option to replace modules and other elements in the innermost regions.

② Increased granularity : To ensure efficient tracking performance at high pile-up, the channel occupancy must be maintained near or below the 1% level in all tracker regions, which requires higher channel density. An average of 140 collisions per bunch crossing is taken as the target number of pile-up events to benchmark the performance of the detector.

③ Improved two-track separation : The present Tracker has degraded track finding performance in high-energy jets, due to hit merging in the Pixel detector. To optimally exploit the statistics of the high luminosity operation, the ability to distinguish two close-by tracks needs to be improved.

④ Reduced material in the tracking volume : The performance of the current Tracker is significantly limited by the amount of material, which also affects the performance of the calorimeters and of the overall event reconstruction in CMS. Operation at high luminosity will greatly benefit from a tracker with significantly less material in the fiducial (基準的) volume.

⑤ Robust pattern recognition : Track finding at high pile-up becomes increasingly more difficult and time consuming. The layout of the upgraded Tracker should enable fast and efficient track finding, which is particularly important for the high level trigger (HLT).

⑥ Compliance with the L1 trigger upgrade : The selection of interesting physics events at L1 becomes extremely challenging at high luminosity, not only because of the rate increase, but also because selection algorithms become inefficient at high pile-up. Therefore, in order to preserve and enhance the performance of CMS in a wide spectrum of physics channels, it is foreseen to increase the L1 rate and latency to 750 kHz and 12.5 µs, and to add tracking information in the trigger decision, moving to L1 part of the reconstruction that is today performed in the high-level trigger.

⑦ Extended tracking acceptance : It has been demonstrated that the overall CMS physics capabilities would greatly benefit from an extended coverage of the tracker and calorimeters in the forward region. For the Tracker, this requirement mostly concerns the layout of the Pixel detector.

A sketch of one quadrant (1/4) of the Phase-2 Tracker layout is shown below.
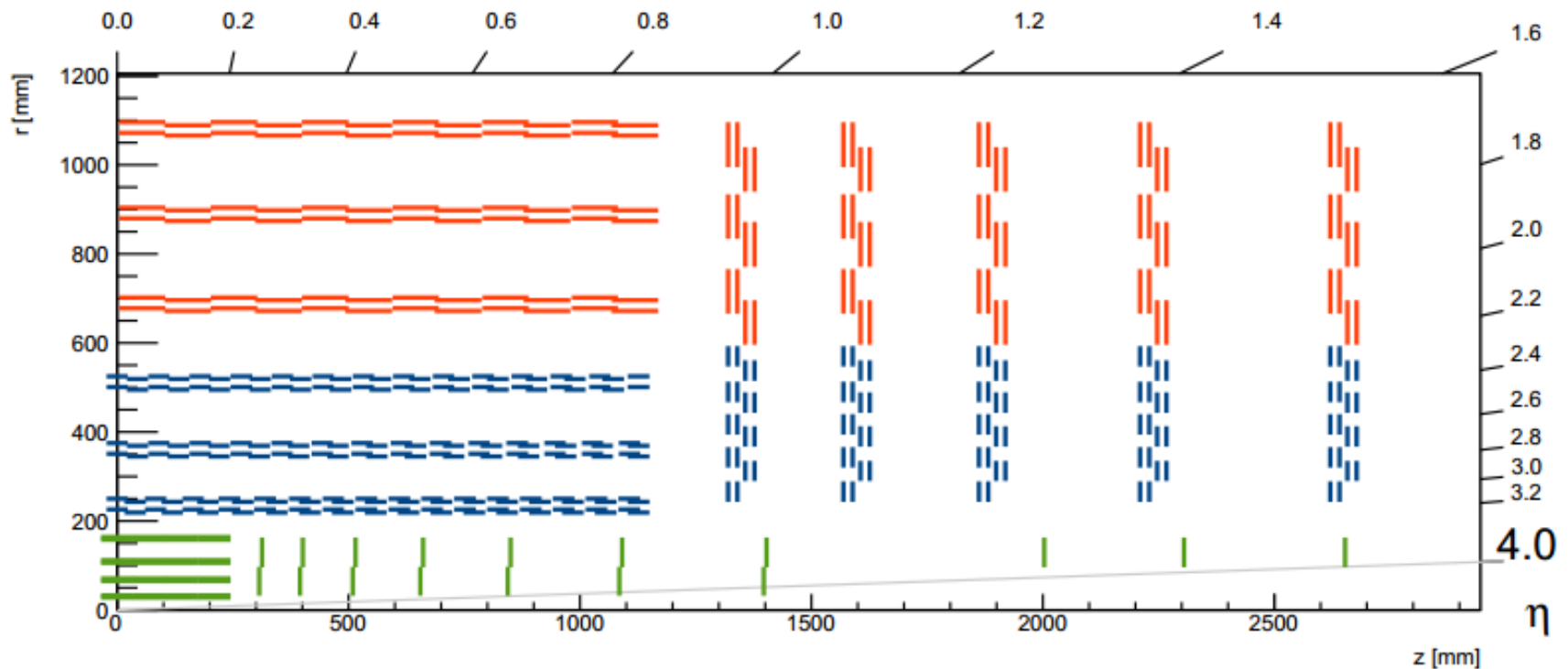
Outer Tracker: blue lines correspond to PS modules, red lines to 2S modules.
The Pixel Detector, with forward extension, is shown in green.

The boundary between the Pixel and Outer Tracker is at around R = 20 cm, the
same location as the interface between the Pixel detector and the Strip detector.

a) Correlation of signals in closely-spaced sensors enables rejection of low-pT particles; the channels shown in light green represent the "selection window" to define an accepted "stub".
b) The same transverse momentum corresponds to a larger distance between the two signals at large radii for a given sensor spacing.
c) For the end-cap disks, a larger spacing between the sensors is needed to achieve the same discriminating power as in the barrel at the same radius. The acceptance window can therefore be tuned along with the sensor spacing to achieve the desired pT filtering in different regions of the detector.
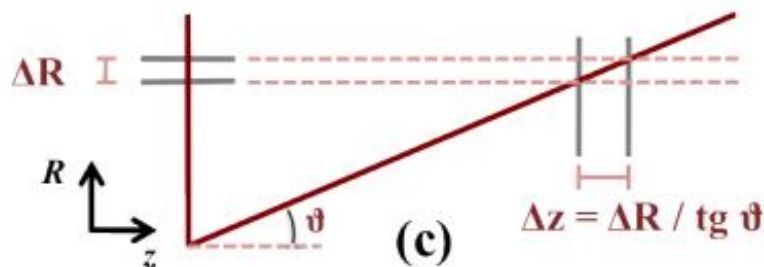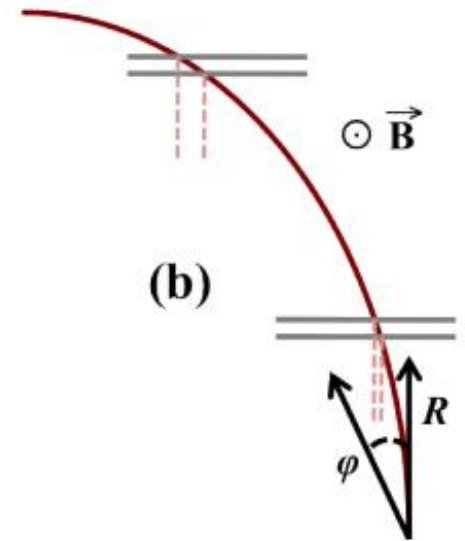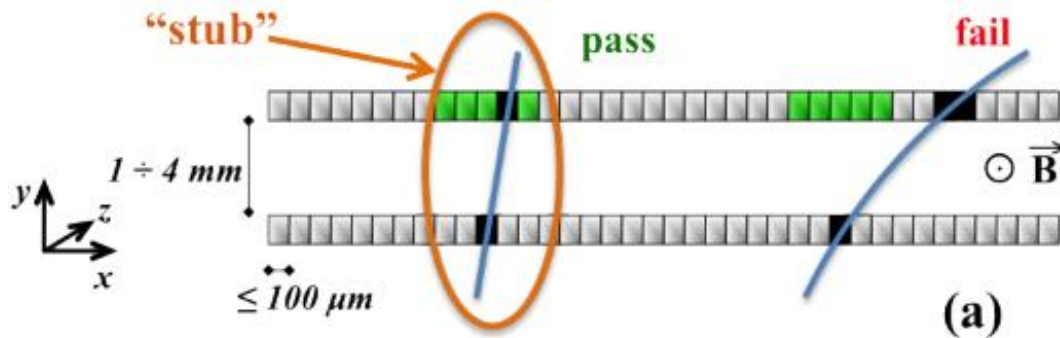
① The requirement of radiation tolerance is particularly demanding for the Pixel detector. Good results can be obtained by using thin planar silicon sensors, segmented into very small pixels. The detector resolution is much more robust with respect to radiation damage than the present detector, where the precision relies on the ability to reconstruct the tails of the charge deposited in a 300 µm thick sensor.

② The required improvement in two-track separation is also obtained. Pixel sizes of 25×100 µm2 or 50×50 µm2 are being considered, representing a factor of 6 reduction in surface area compared to the present pixel cells. For the readout chip, such a small pixel size can be achieved with the use of 65 nm CMOS technology and an architecture where a group of channels (pixel region) shares digital electronics for buffering, control and data formatting.

③ An alternative option that is being actively pursued is the possibility to use 3D silicon sensors, offering intrinsically higher radiation resistance because of the shorter charge collection distance. The use of 3D sensors could be limited to the small regions of highest particle fluence. (becacuse 3D sensor is very expensive.)

④ The new design will preserve the ease-of-access of the current detector that enables the possibility to replace degraded parts over an Extended Technical Stop.

⑤ The geometry of the Phase-1 detector with 4 barrel layers and 3 forward disks is taken as a starting point. The forward extension could be simply realized by increasing the number of forward disks from 3 to 10, out of which the last 3 consist of the outer part only, in order to be compatible with the conical section of the beam pipe. Such an extended pixel detector will have an active surface of approximately 4 m2, compared to 2.7 m2 for the Phase-1 detector.

3. Overview of the Outer Tracker detector design

① The Outer Tracker provides data both for the L1 reconstruction (for each bunch crossing), and for the global event processing upon reception of a L1 trigger decision. The L1 functionality depends upon local data reduction in the front-end readout electronics, in order to reduce the required bandwidth of the L1 data stream. This is achieved with modules that are themselves capable of rejecting signals from particles below a certain pT threshold, that are referred to as "pT modules". A threshold of around 2 GeV corresponds to a data volume reduction of roughly one order of magnitude, which is sufficient for the purposes of L1 data transmission.

② The modules are composed of two closely-spaced silicon sensors read out by a common front-end. The front-end ASICs correlate the signals collected in the two sensors, and select pairs that form "stubs" compatible with particles above the chosen pT threshold. The strong magnetic field of CMS provides sufficient sensitivity to measure pT over the small sensor separation, enabling the use of pT modules in the entire radial range above R ≈ 20 cm.

③ Stub data are sent out at every bunch crossing, while all other signals are stored in the front-end pipelines for reading out when a trigger is received.

④ To implement the same pT threshold for the stubs throughout the tracking volume, the acceptance window must be programmable in the front-end ASICs, and different sensor spacings must be implemented in different regions of the tracker. (see the figure in page 8)

⑤ Two types of pT modules are under development. "2S" modules are composed of two super imposed (上下層有重疊) strip sensors of approximately 10 × 10 cm2, mounted with the strips parallel to one another. They populate the outer regions, above R ≈ 60 cm (in red in the sketch in page7) which corresponds to a sensor surface area of approximately 150m2.

⑥ Wire bonds at opposite ends of the sensor provide the connectivity of both sensors to the readout hybrid. A single "service hybrid" carries a 5 Gb/s data link, an optical converter(光電倍增管??), and the DC/DC converter that provides power to the module electronics. The use of one optical link per module provides the bandwidth needed for the trigger functionality, and at the same time offers significant advantages in the overall system design by avoiding additional electrical interconnectivity in the tracking volume.

⑦ "PS" modules are composed of two sensors of approximately 5 × 10 cm2, one segmented in strips, and the other segmented in "macro-pixels" of size 100 μm × 1.5 mm. The chosen pixel size permits the use of the "C4" bump-bonding(凹凸結合) technology.

⑧ For the 2S module, wire bonds provide the connections from the strip sensor and from the macro-pixel readout chip to the front-end hybrid, and, in turn, to the auxiliary electronics for powering and readout, all of which is integrated in the module assembly

⑨ PS modules are deployed in the radial range between R ≈ 20 cm and R ≈ 60 cm (blue in the sketch in page 7), resulting in a sensor surface area of about 60 m2. The pixelated sensors provide sufficiently precise measurements of the z coordinate for tracking to enable primary vertex discrimination at L1.

- ⑩ Three additional layers of unambiguous 3D coordinates each with an associated estimate of the particle pT, are of particular use for track finding, offering enhanced robustness for the pattern recognition
- To remove heat from electronics and sensors, CO_2 two-phase cooling will be used. This choice of cooling technology helps to reduce the amount of passive material in the tracking volume.
- Noted that all end-cap disks are equipped down to the lowest radius, to be compatible with an extension of the tracking acceptance up to $|\eta| = 4$, while in the present tracker, rings located beyond $|\eta| \leq 2.5$ are not equipped.
- In summary, in the baseline layout the Outer Tracker consists of 15508 detector modules (8424 2S and 7084 PS), with a total active surface of 218 m2, 47.8 million strips and 218 million macro-pixels.
- Barrel pixel from 3 to 4 layers. Endcap pixel from 2 to 10 layers.

The Pixel Detector(2.2)

The target integrated luminosity of 3000 fb^{-1} corresponds to a hadron fluence of $2 \times 10^{16} n_{eq} \, cm^{-2}$ at 3 cm from the interaction region, roughly where the first layer of the Pixel Detector will be located as is the case for the Phase-1 detector. The fluence decreases rapidly with distance and is about $3 \times 10^{15} n_{eq} \, cm^{-2}$ at a radius of 11 cm. The latter is similar to the fluence foreseen for the ATLAS IBL (what?) and the innermost layers of the CMS Phase-1 pixel detector after 500 fb^{-1}.

1. Development of silicon sensors

① The n-in-n planar technology, developed for the current pixel detector and its Phase-1 replacement, is a valid baseline for instrumenting the outer layers of the barrel and the outer regions of the forward disks.

② Collection of electrons is advantageous because of their higher mobility compared to holes, leading to lower trapping probability and hence larger collection efficiency after heavy irradiation.

③ Adoption of n-in-p sensors could reduce the cost, as they are produced with single sided photolithography which is cheaper than the double sided processing required for n-in-n sensors. The n-in-p option requires the development of a robust scheme to protect against micro-discharges, in order to ensure safe operation at the high bias voltage required after heavy irradiation.

④ Thin sensors (150 µm or less) offer advantages in terms of lower bias voltage and lower leakage current. Moreover, the shorter drift distance results in smaller clusters which, when combined with a smaller pixel cell and a reduced signal threshold for the smaller charge that is produced, can achieve good resolution and improved two-track separation in high-energy jets.

⑤ For the innermost regions of the detector the 3D silicon sensor technology could offer advantages. For instance, an intrinsically lower bias voltage and shorter drift distance leads to lower trapping probability. For small pixel cells, however, 3D sensors may suffer from significant charge loss in the implant region.

⑥ Figure in page 15 displays a compilation of results of measured charge in planar silicon strip structures (left) and 3D silicon pixel structures from different vendors (right), after heavy irradiations; such results suggest that sufficient charge collection may be retained even at the innermost radii, and show the clear advantage of 3D silicon in regard to low bias voltage.

⑦ Cell configuration, sensor thickness, number of implants per cell, and implant aspect ratio are considered in the comparison of planar silicon and 3D silicon sensors. Diamond sensors, HV-CMOS and MAPs and other development plans are also taken into account to find the best performance and radiation tolerance, as well as the expected sensor cost.
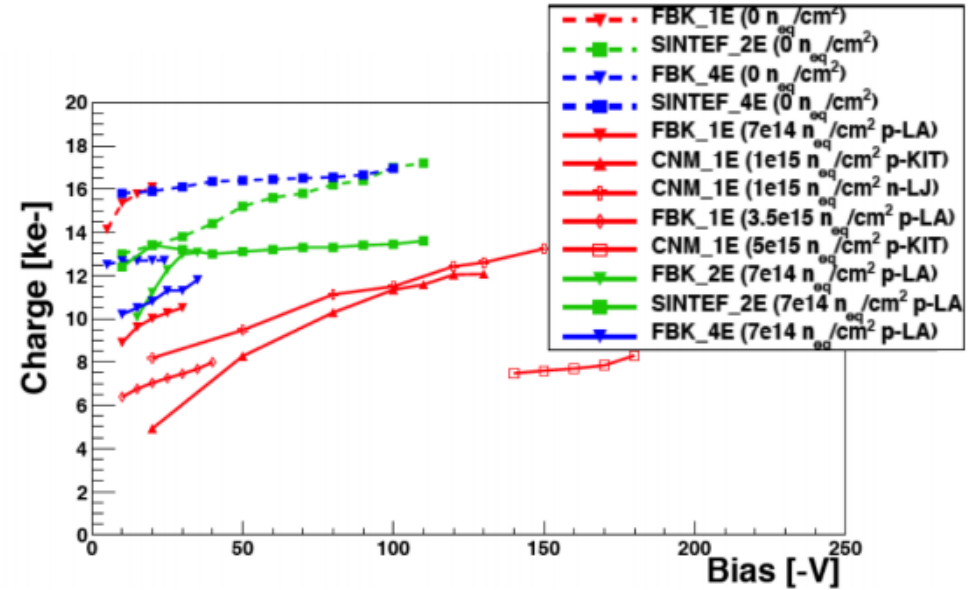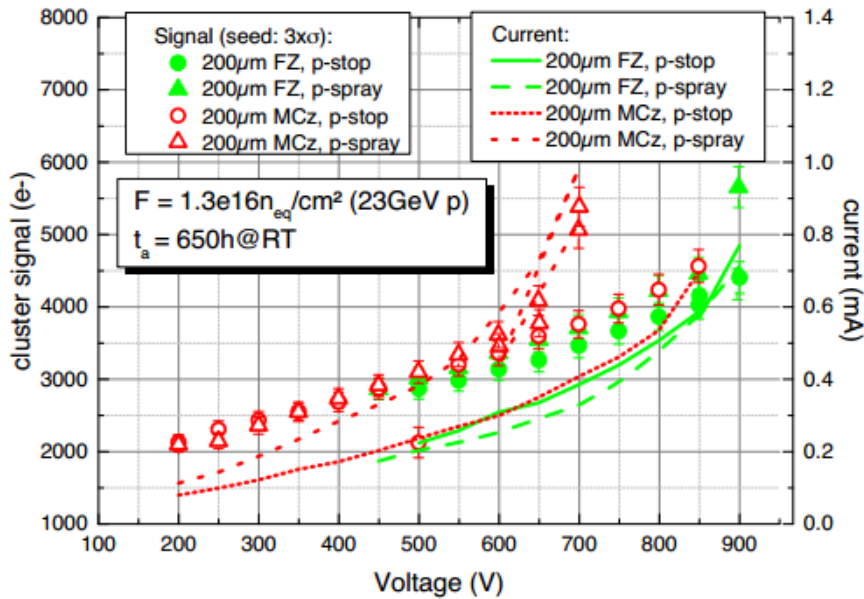
- Left: signal charge and leakage current measured in planar n-in-p strip structures in different materials and technologies, after irradiation to $1.3 \times 10^{16} n_{eq} cm^{-2}$ with 23GeV protons and annealing equivalent to 650 hours at room temperature.

- Right: signal charge in 3D n-in-p pixel structures from different vendors and with different column configurations, before irradiation (dashed lines) and after irradiation up to $5 \times 10^{15} n_{eq} cm^{-2}$ (solid lines).

2. Readout electronics

① Hybrid pixel detector modules are made from multiple pixel Read-Out Chips (ROC) bump-bonded to a single pixel sensor. Readout and control signals plus power are connected to the ROCs with wire bonding to a thin and light Printed Circuit Board (PCB) glued on the back side of the pixel sensor.

② Low mass cables connect the pixel modules to the global readout, control and powering systems. The heat generated by the pixel chips and sensor is removed via a heat distribution layer to thin CO_2 cooling pipes. The optional use of Through Silicon Vias (TSV), to get readout signals and power of the ROC out from its back side will also be investigated to build more compact pixel detector modules with less inactive surface and material.

③ A pixel surface of 2500 µm2 has been chosen as a target, to be implemented in two aspect ratios: 50 × 50 µm2 and 25 × 100 µm2. These sizes are the result of a compromise between the requirement of maintaining and possibly improving tracking and vertexing performance with thinner sensors, and the expected technology limitations in sensors, readout chips and bump-bonding technologies.

④ In the outer part of the detector, where the particle density is significantly smaller, a larger pixel size may bring advantages in terms of reduced power consumption. With an appropriate bump-bonding pattern the same ROC can be used for the two different pixel aspect ratios, and also for larger pixels with compatible dimensions by disabling the unused channels, as illustrated in the sketches in (right).
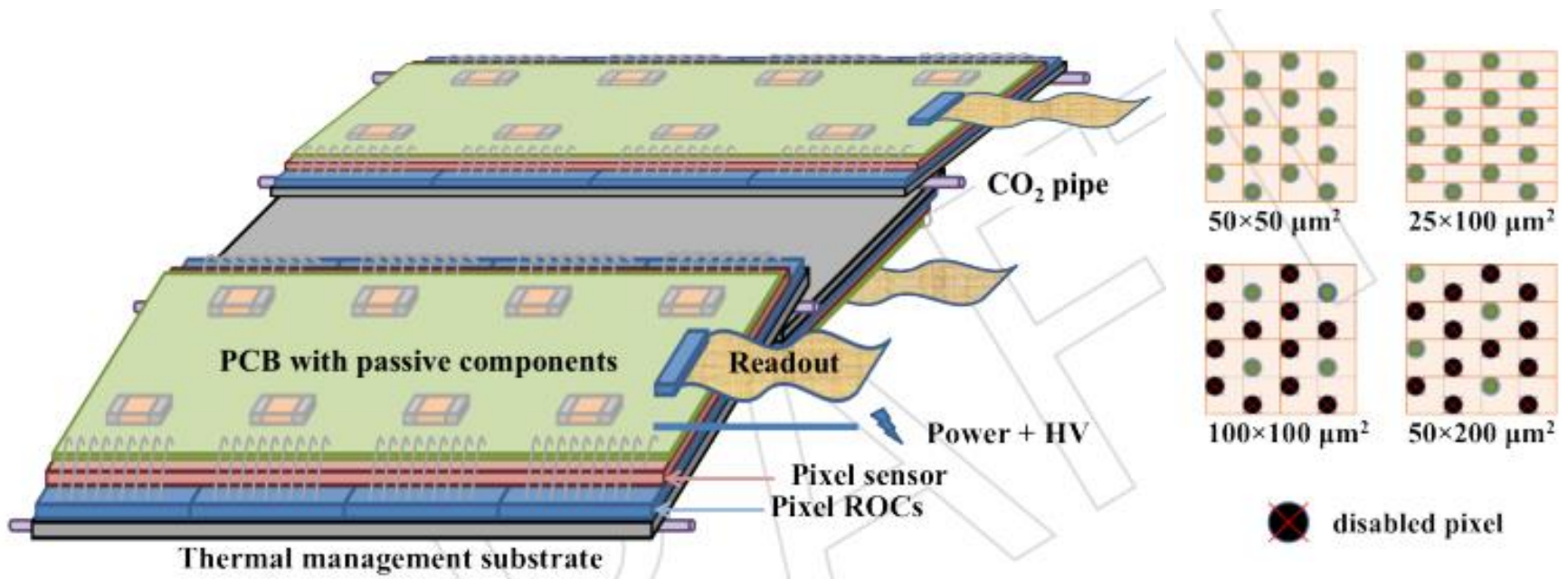
Left : the on-detector pixel electronics systems, shown for the barrel configuration.

Right : bump-bonding grid applied to different pixel aspect ratios and sizes.

1) The Readout Chip

① Compared to the Phase-1 implementation, the Phase-2 ROC will feature six times smaller pixels, will have to cope with about five times higher hit rates, five or ten times higher trigger rates, as well as longer trigger latency

② The work program of RD53 for the next three years includes the radiation qualification of the selected 65 nm CMOS IC technology, the development of all the basic circuits required to build the HL-LHC pixel ROCs, and the production of a large prototype chip with 50×50 µm2 pixels, which will serve as a common basis for the final designs of the ATLAS and CMS pixel ROCs.

③ A common pixel chip architecture, that is fully digital after the basic threshold detection and charge digitization in the analogue pixel cell, has been defined as shown in page 19.

④ Digital hit processing, including the critical trigger latency buffer, is implemented within the pixel array in local pixel regions (e.g. 2×2 or 4×4 pixels) followed by data merging, data formatting and readout after the first level trigger accept.

⑤ Buffering requirements have been verified to be compatible with the proposed extended CMS trigger latency of 12.5 µs. A buffer depth of 16 pixel clusters for a 4×4 pixel region is sufficient to guarantee a hit loss probability below 0.001 for the highest hit rate of 2 GHz/cm2.

⑥ A chip size of about 20×20 mm2 with about 90% active pixel area (with the remaining 10% being used for end of column readout, control interface and wire bonding pads), is currently believed to be an appropriate choice for the detector layout, compatible with reliable production in 65 nm technology and available bump-bonding technologies.
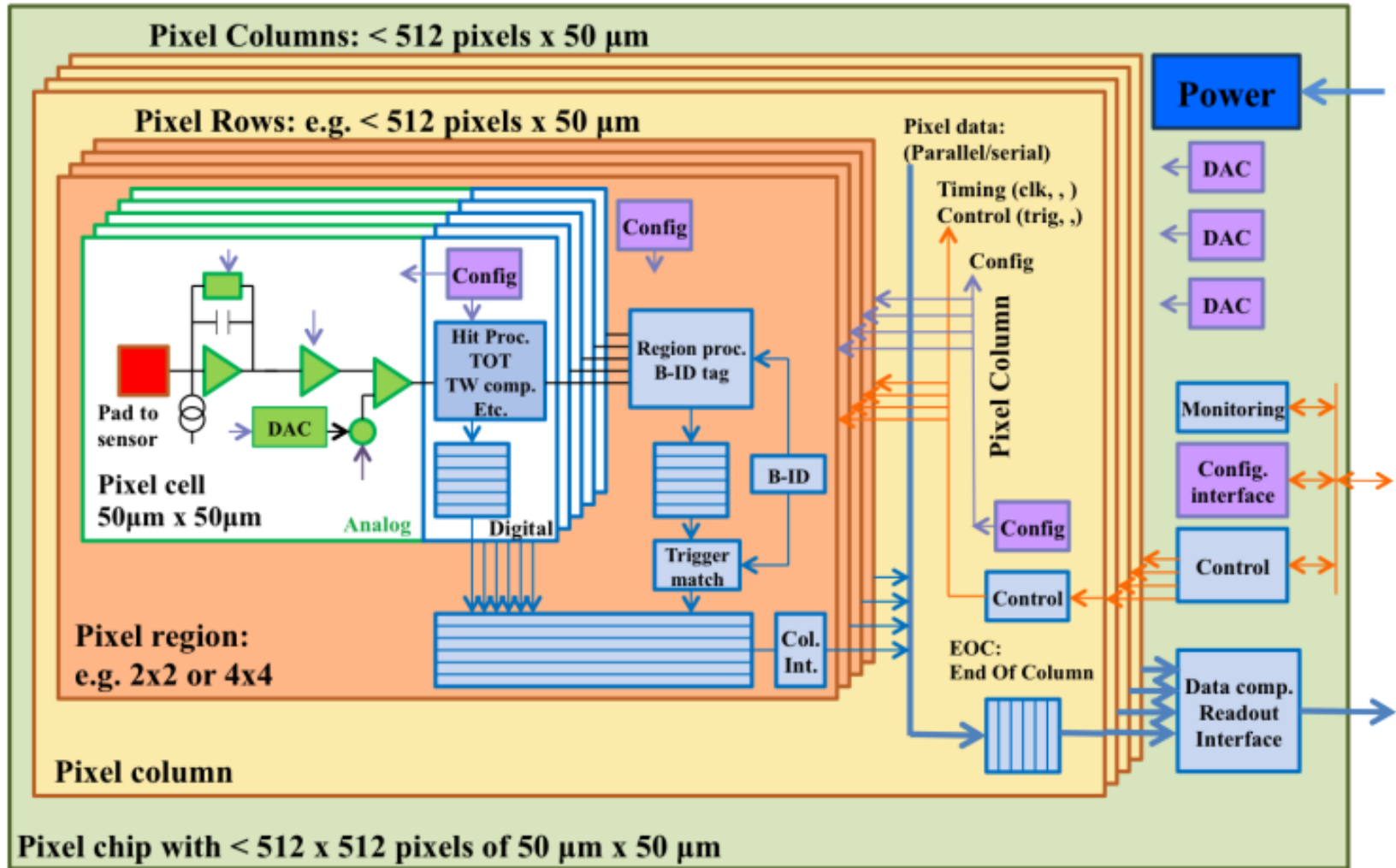
RD53 digital pixel chip architecture

2) System aspects

Rapidity(φ)

- Rapidity(φ) can be defined as the hyperbolic angle that differentiates two frames of reference in relative motion, each frame being associated with distance and time coordinates.

- $E = m\gamma c^2 = mc^2 \cos\varphi$, where $\cos\varphi = \gamma = \dfrac{1}{\sqrt{1-\frac{v^2}{c^2}}} = \dfrac{1}{\sqrt{1-v^2}}$ is the Lorentz factor (c=1).

- $p = m\gamma v = mc \sin\varphi$

- $\varphi = \tanh^{-1}\dfrac{|p|c}{E} = \dfrac{1}{2}\ln\dfrac{1+\frac{|p|c}{E}}{1-\frac{|p|c}{E}} = \dfrac{1}{2}\ln\dfrac{E+|p|c}{E-|p|c}$ $\left(\because \tan^{-1}x = \dfrac{1}{2}\ln\left(\dfrac{1+x}{1-x}\right)\right)$

Prove $\left(\tan^{-1}x = \dfrac{1}{2}\ln\left(\dfrac{1+x}{1-x}\right)\right)$: $\tanh x = \dfrac{e^x - e^{-x}}{e^x + e^{-x}} = \dfrac{1-e^{-2x}}{1+e^{-2x}}$

assume $y = \dfrac{1-e^{-2x}}{1+e^{-2x}} = -1 + \dfrac{2}{1+e^{-2x}}$ $\rightarrow$ $\dfrac{2}{y+1}=1+e^{-2x}$ $\rightarrow$ $\ln\dfrac{1-y}{1+y} = -2x$ $\rightarrow$ $x = \dfrac{1}{2}\ln\dfrac{1+y}{1-y}$

$$\therefore \tanh^{-1}\dfrac{1}{2}\ln\dfrac{1+y}{1-y}$$

- Pseudorapidity(η) : $\eta = -\ln\left(\tan\dfrac{\theta}{2}\right)$ Rapidity(φ) : $\varphi = \dfrac{1}{2}\ln\dfrac{E+p_z}{E-p_z}$

- $\varphi = \ln\left(\dfrac{\sqrt{m^2+p_T^2\cosh^2\eta}+p_T\sinh\eta}{\sqrt{m^2+p_T^2}}\right)$

Expected time

$Expected\ time = z/v_z$, where z is the value on z axis and Vz is the speed in z direction.

Pz=mVzR