<<Pixel detectors>>
Chapter 2 sensor-3

Processing of Silicon Wafers

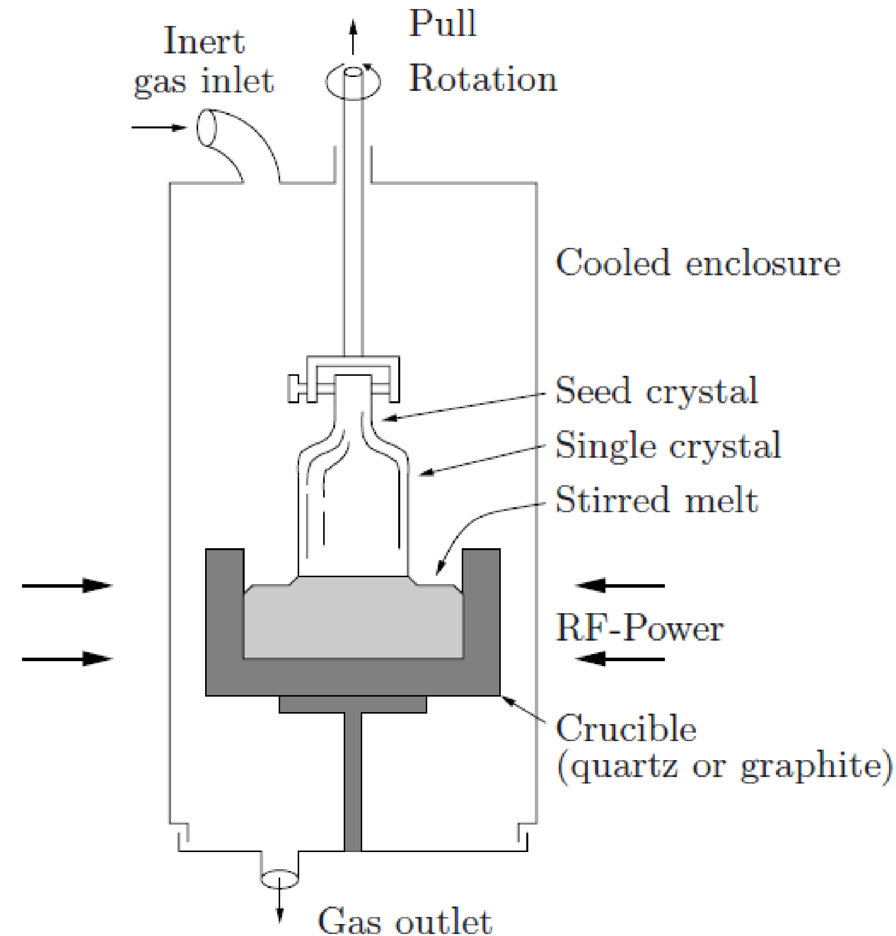
- special and challenging requirements in sensor processes
  - high-temperature steps was considered the most difficult problem
  - Any contamination of the wafer surfaces and the quartz tube in the furnace has to be avoided before and during the high-temperature steps
  - minimize the number of high-temperature steps
- Both sides of the wafer are important for processing.
- Large devices without defects are required.

Production and Cleaning of Silicon

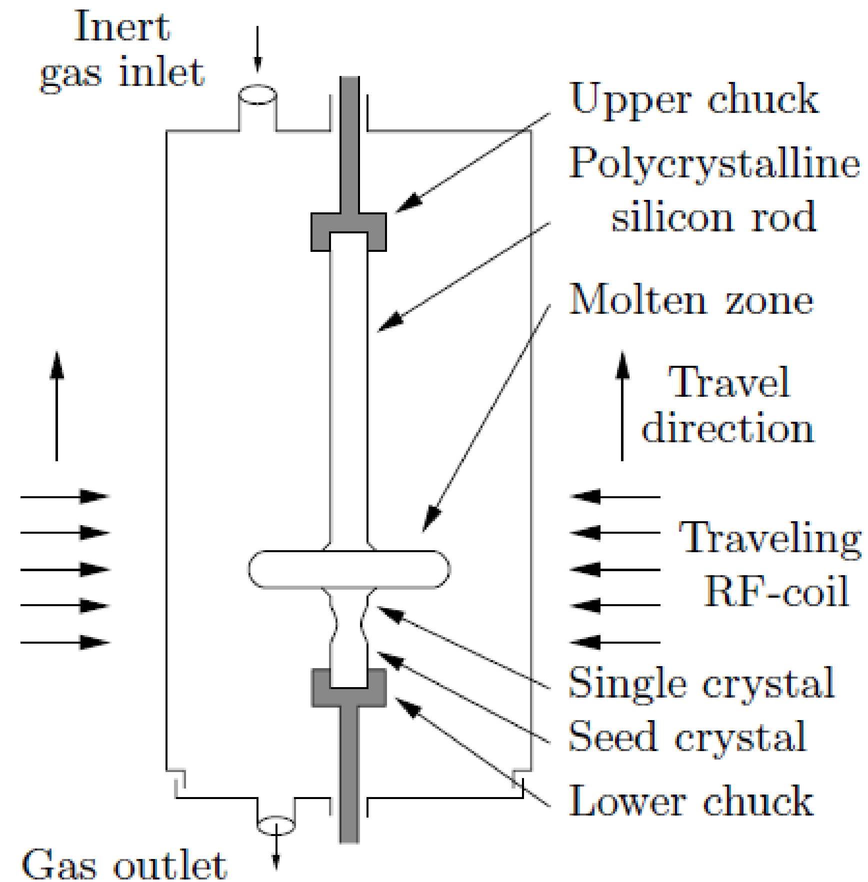
- Silicon is isolated from quartzite, which is a relatively pure form of sand (SiO_2)
- a reduction with carbon at temperatures above 1400 $\circ C.$
- The resulting solid silicon of about 98% purity is treated with hydrochloric acid (HCl) at roughly 300$\circ$C to form trichlorosilane ($SiHCl_3$), which has a boiling temperature (32$\circ$C) lower than that of the chlorine compounds of unwanted impurities, which allows a distillation
  - impurity concentration of better than 10^{-9} *can be reached*

Two growing methods
Czochralski process

- silicon contains many unwanted impurities, mostly oxygen atoms originating from the walls of the crucible with a concentration
- not used for resistivity more than 10Ωcm



float zone method



- **If a certain substrate doping is targeted, it can be mixed into the atmosphere**

Thermal Oxidation

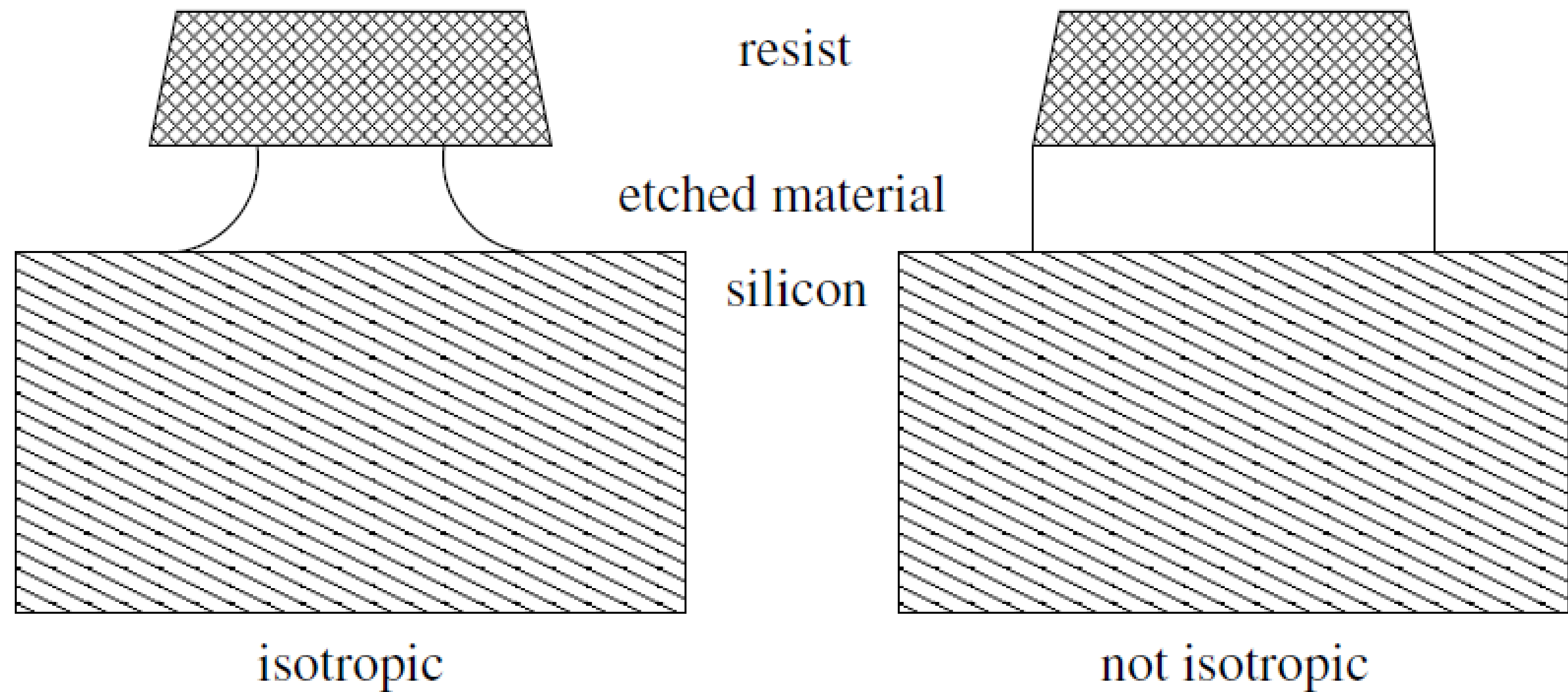
- protect the wafer surface with a thin (about 150nm to 2 µm) layer of $SiO2$
- storing the wafer at a temperature between 900 and 1200 ◦C in an oxygen atmosphere
- If water vapor is added to the oxide atmosphere, the oxidation process is called wet oxidation and reaches growth rates which exceed the ones obtained in dry oxidation by about a factor of 5
- The addition of chlorine during oxidation is useful in various aspects
  - volatile compounds with unwanted impurities especially sodium

Layer Deposition

- Chemical vapor deposited are used as covering insulation layers

Photolithographic Steps, Etching

- photoresist is spun onto the wafer surface
- For a good spatial resolution a short wavelength in the UV range is used.
- Etching is used to copy the structure of the photoresist into the underlying layers.
- The two most important properties of the process are its isotropy and its selectivity.
- Dry plasma etching, the most widely spread etching method in microelectronics, provides a high degree of anisotropy and therefore allows small structures but lower selectivity



- In an isotropic etching process the material is removed in all directions

Doping

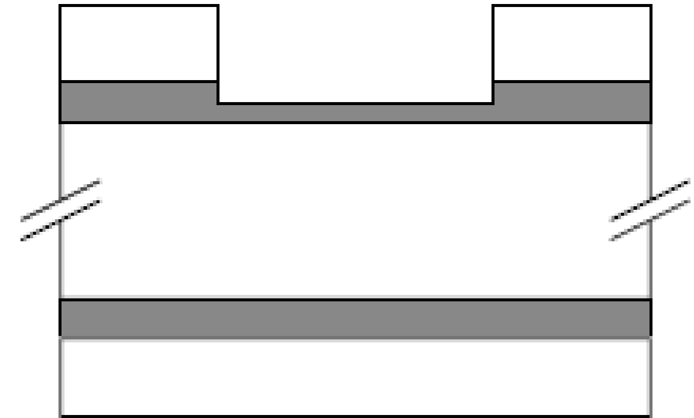
- **Diffusion**
  - The wafers are placed in a furnace rinsed with an inert carrier gas
- **Implantation**
  - In the implantation the doping atoms are ionized, accelerated, and shot directly into the silicon wafer
  - Implantation is performed at room temperature allowing photoresist to be used for masking the areas that are not doped
  - The penetration depth of the ions and hence the shape of the doping profile can be adjusted by choosing the energy

Metallization

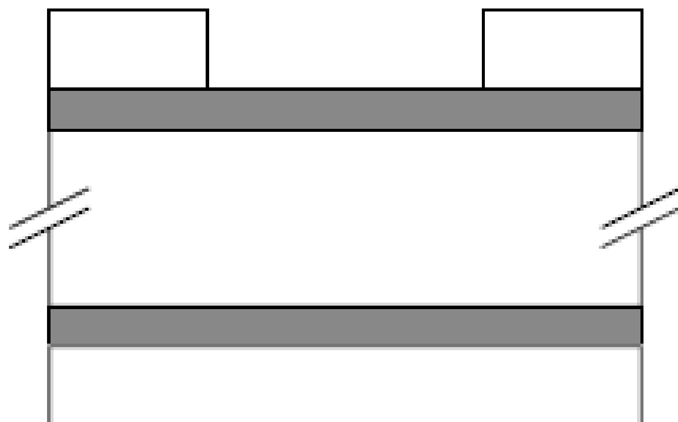
- provide a low resistivity connection between several devices on the same silicon substrate or to form bond pads
- common metal used is aluminum because of its low resistance and its good adhesion on silicon oxide

Example of a p+-in-n pixel

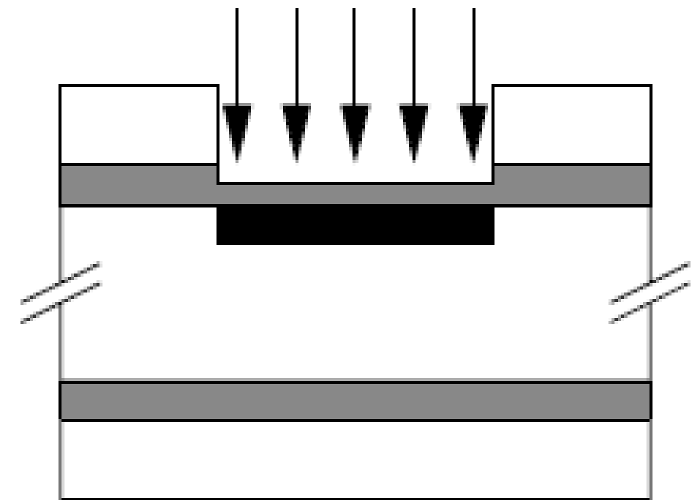
1. Thermal oxidation



3. Etch oxide step for alignment

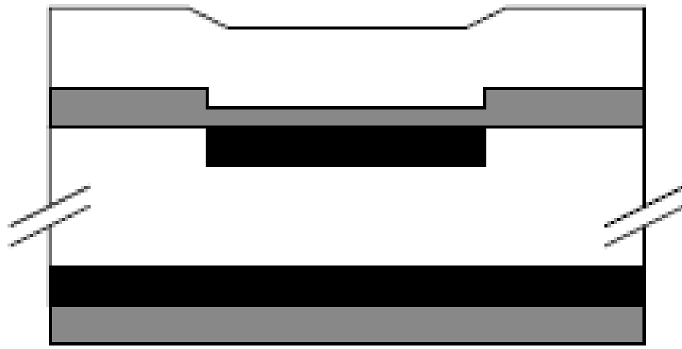


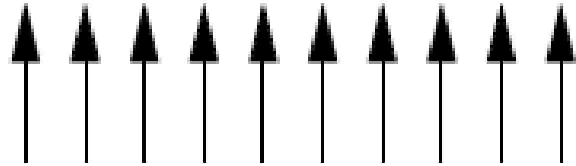
2. Photoresist for implant



4. Boron implantation

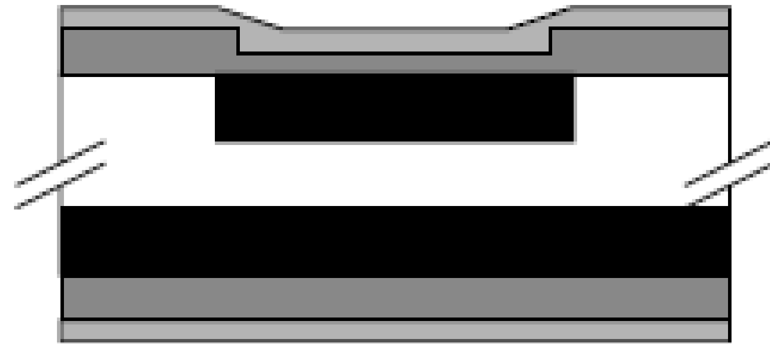
- **The thickness (1 µm) has to be small enough to allow implantation and large enough to display the necessary electrical strength**



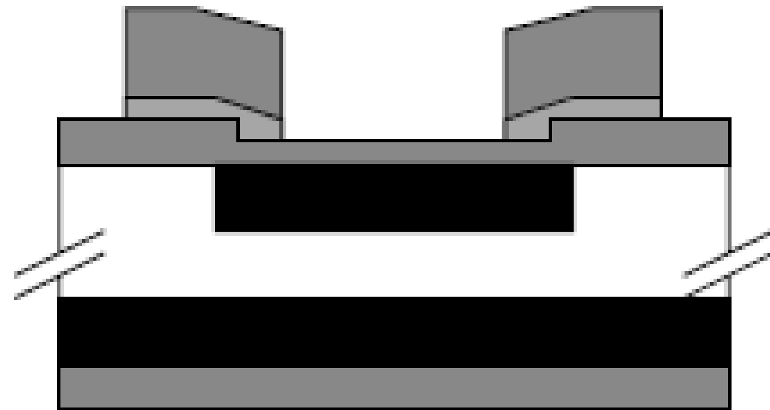


5. Phosphorus implantation

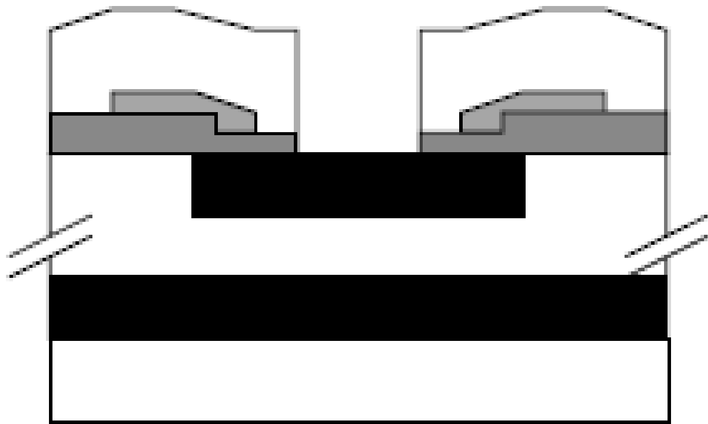
6. Annealing and drive–in



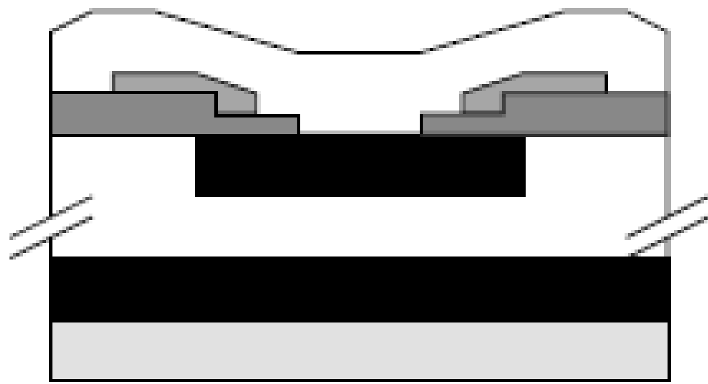
7. Nitride deposition



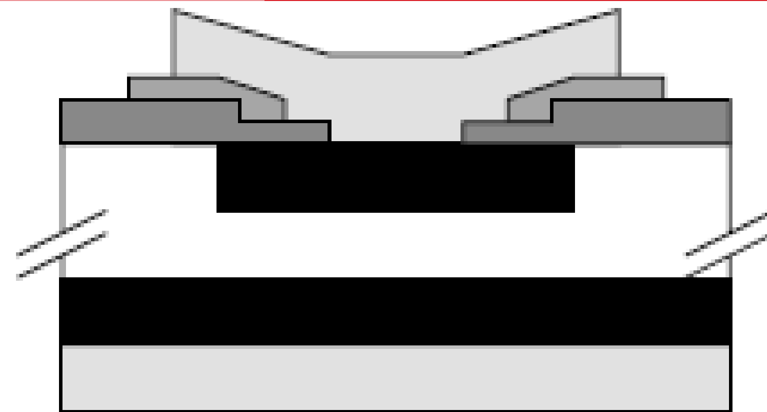
8. Etch nitride openings



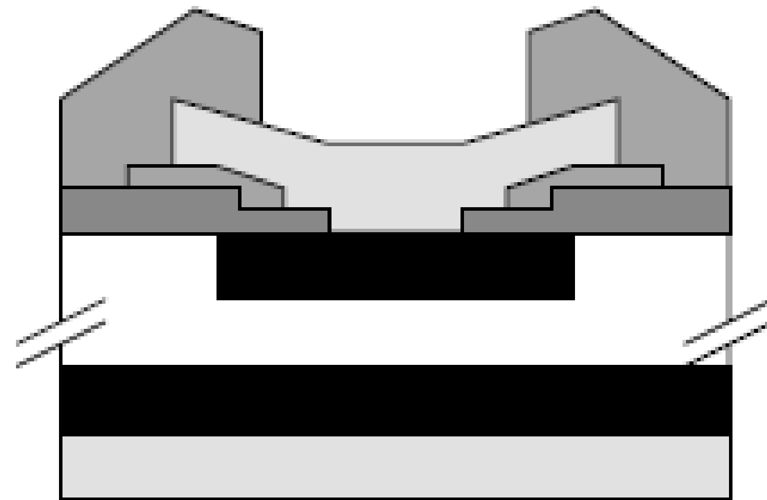
9. Etch oxide openings



10. Back side aluminization



11. Front side aluminization



12. Passivation

The advantages of silicon

1. Its relatively low density and low radiation length *X0* which is particularly important for particle physics
2. The fact that large silicon crystals can be grown as a substrate material without large inhomogeneities or impurities resulting in large charge carrier lifetimes of *≈100 µs.*
3. The fact that silicon can be doped with specifically tailored doping profiles allowing to shape the potential inside the detector for best charge collection.
4. Its low price and good availability. Its industrial fabrication and processing has been matured over decades.

Table 2.2. Characteristic properties of some semiconductors

Semi conductor	Density (g/cm^3)	Band gap (eV)	Intrinsic carrier concentration (cm^{-3})	Average Z	$w_{e,h}$ (eV)	Mobility ($cm^2/(Vs)$)		Carrier lifetime
						e	h	
Si	2.3	1.12	1.45×10^{10}	14	3.61	1,415	480	∼250 µs
Ge	5.3	0.66	2.4×10^{13}	32	2.96	3,900	1,800	250 µs
GaAs	5.4	1.42	1.8×10^{6}	32	4.35	8,800	320	1–10 ns
CdTe	6.1	1.44	10^{7}	50	4.43	1,050	100	0.1–2 µs
CdZnTe	5.8	∼1.6	10^{7}	49.1	4.6	∼1,000	50–80	∼µs
CdS	4.8	2.42		48/16	6.3	340	50	
HgI_2	6.3	2.13		62	4.2	100	4	∼µs
InAs	5.7	0.36		49/33		33,000	460	
InP	4.8	1.35	1.3×10^{7}	49/15		4,600	150	
ZnS	4.1	3.68		30/16	8.23	165	5	
PbS	7.6	0.41		82/16		6,000	4,000	
Diamond	3.5	5.48	$<10^{3}$	6	13.1	1,800	1,200	∼1 ns

Gallium Arsenide

- carrier lifetime of only 10 ns as compared to 250 µs in silicon
- The intrinsic carrier density of undoped GaAs is already small, n_{intr} =10^6 cm^−3
  - already depleted
- potential radiation hardness due to the large band gap of 1.43 eV as compared to silicon

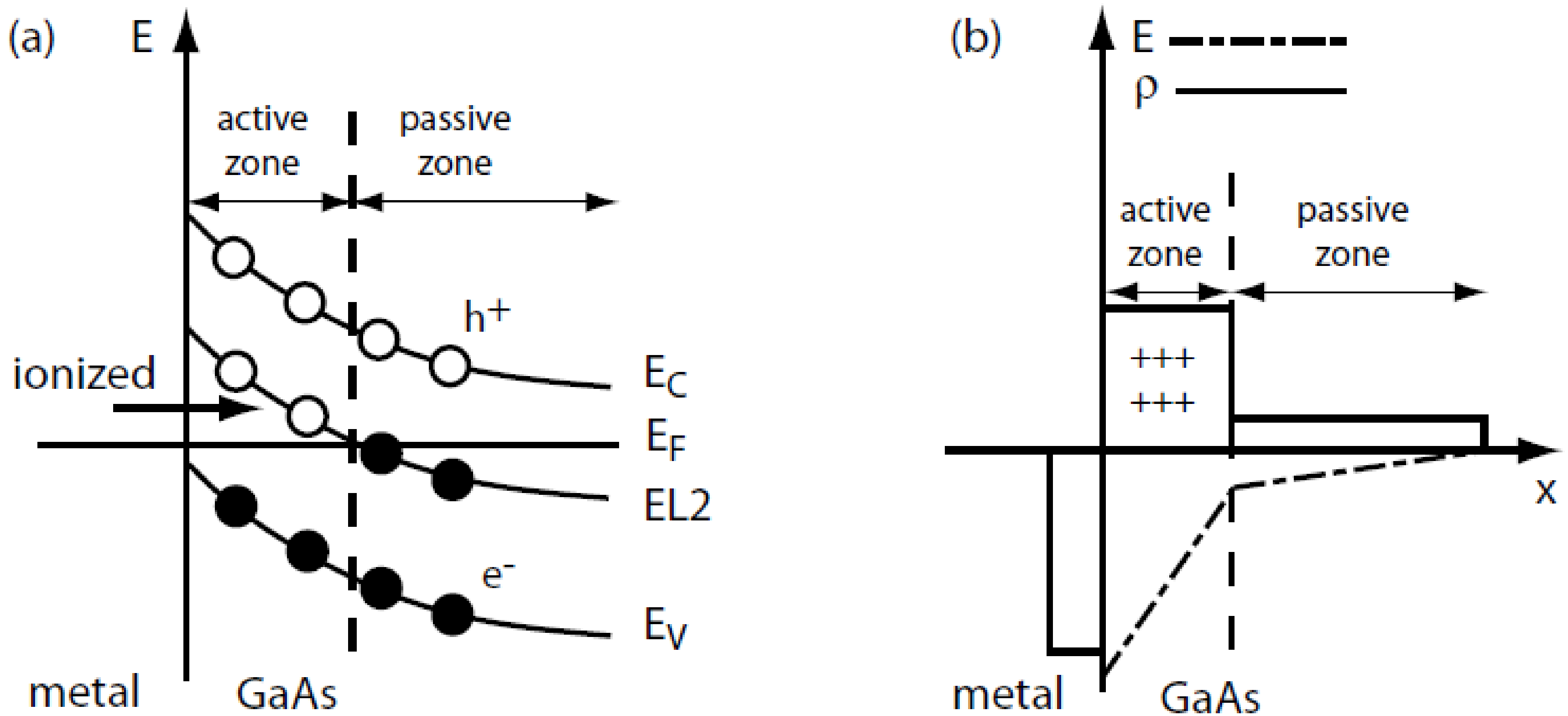


Fig. 2.56. (**a**) Simplified band diagram of a GaAs Schottky diode. (**b**) The resulting space charge density and electric field dependence inside the substrate material

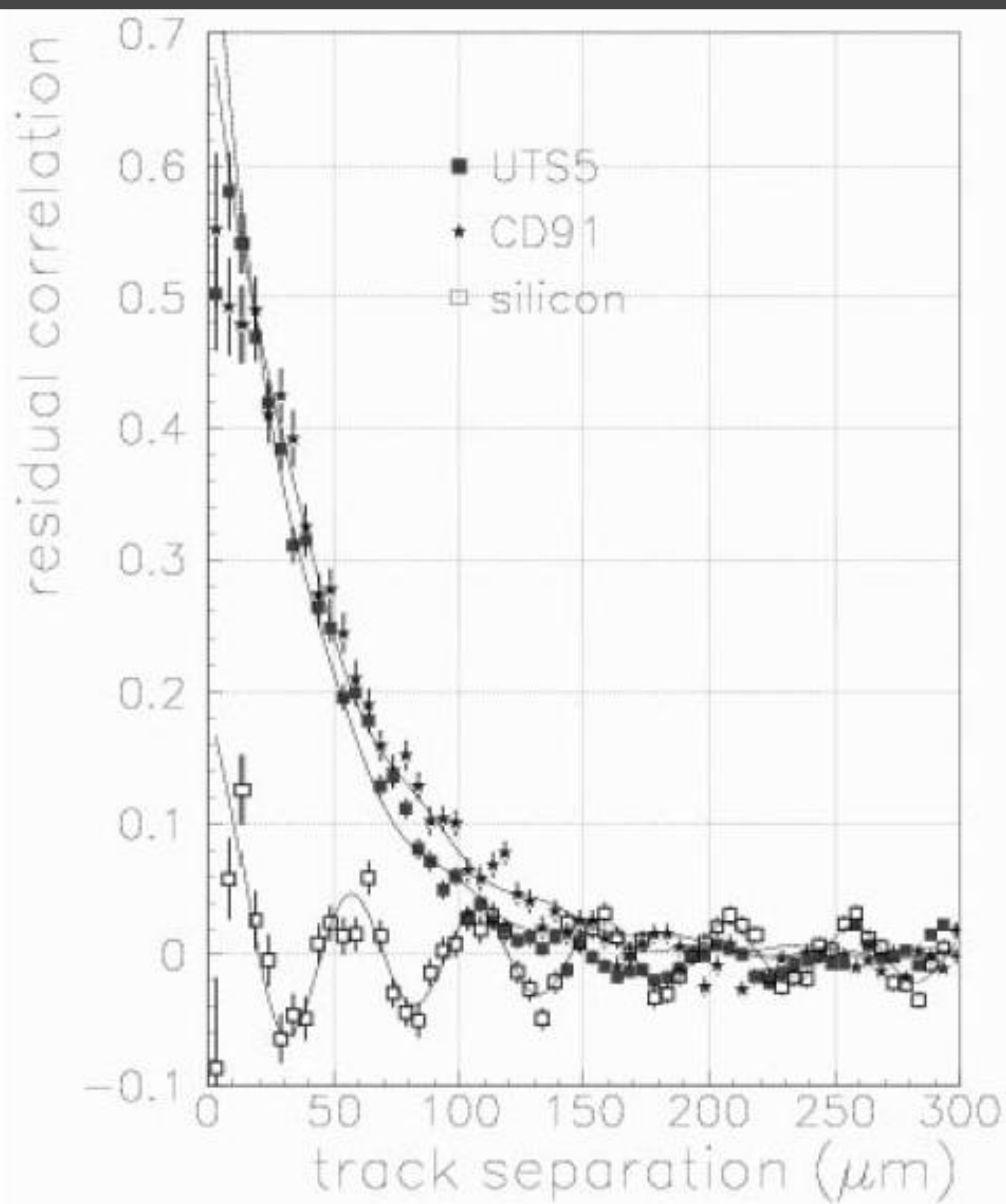
- **charge collection behavior is largely influenced by the EL2- ionization leading to high and low electric field regions in the substrate**

CdTe and CdZnTe

- intrinsic carrier concentration n_{intr} is of the order of 10^7
- charge collection behavior: in CdTe the shape of the electric field depends on the filling state of traps and hence the time the sensor is exposed to radiation
- In particular the poor hole charge transport results in position-dependent charge collection properties
- sometimes reported deficiency is the poor homogeneity of CdTe devices

Diamond

- The reason for this interest is the apparent radiation hardness of diamond even for radiation doses in excess of those experienced at LHC
- a large band gap, a close to zero intrinsic charge carrier concentration resulting in a high resistivity
- can therefore be operated at room temperature even after intense radiation exposure
- Energy deposits by impinging radiation create one electron–hole pair per 13.*1 eV*
- While the mobilities of electrons and holes have values well above 1,000 $cm^2/(Vs)$ the carrier lifetime is very short (a few nanoseconds).



residual correlation
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
−0.1
0
50
100
150
200
250
300
track separation (μm)
UTS5
CD91
silicon