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SCT Barrel Module FDR Document

SCT Barrel Module : MODULE QA

Abstract

This document describes the quality assurance procedure to be applied for the SCT barrel module production.

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Distribution List

Table of Contents

1 SCOPE OF THE DOCUMENT

This document describes the QA procedure to be applied to barrel modules during the construction process. The QA procedures for the individual components are dealt with in other documents (see SCT-BM-FDR-5). Tests are made during assembly to check that the components have not been damaged, for example in transport or in the first stages of module construction. Post-assembly testing validates the quality of the completed module: most tests will be performed on all produced modules, but some destructive or very time-consuming tests are performed on a sample subset of modules.

The procedures and tests described here aim to investigate a wide range of potential failures and problems. This extensive testing will be applied during the first part of the module series production, but is time consuming. In the later parts of the production, where the production rate is higher and experience of previously produced modules has been gained, the procedures will be reduced in areas that do not show failures.

The results of all tests will be logged to the SCT database. In some cases a simple yes/no result is obtained, for most tests characteristic performance data will be logged in addition to the flag of whether the module passes the relevant QA criteria.

The aim of the QA procedures is to ensure that each SCT Barrel Module fulfils all aspects of the specification. The same QA procedures and criteria will be applied at all the four barrel module production sites.

2 QA DURING MODULE ASSEMBLY

The following QA steps are performed during the assembly of a module. The criteria for accepting a module as 'good' are for initial use, and will evolve with experience.

2.1 Assembly of ASICs onto hybrids

Before delivery to the assembly site, the individual components have already been subject to QA procedures as described in SCT-BM-FDR-5.3 for the Hybrids and in SCT-MB-FDR-5.4 for the ASICs.

2.1.1 Tests of Distributed Passive-Component Mounted Hybrids

Hybrids with passive components mounted but without ASICs are distributed to the hybrid assembly sites. After transport a subset of the acceptance tests for hybrids are repeated to check that no damage has occurred in transport. For similar reasons, a visual check is made of each hybrid. The glass fan-in on the hybrid is also checked visually for any damage.

Before ASIC attachment, pull-tests are also made on each hybrid, requiring pull strength values of 6 gm for 30% height to distance ratio setting.

2.1.2 Electrical Tests of Hybrids after ASIC Attachment

After attachment of ASICs to the hybrids all wire bonds between hybrid and ASICs are made. At this stage an electrical test is made of the hybrid to ensure that all ASICs perform properly and that all wire bonds are functional. This is done by performing a Characterisation Sequence (see section 3.3).

2.1.3 Long Term Test of Hybrids with ASICs

In addition to the full ASIC characterisation on the hybrids, a longer duration test is performed on assembled hybrids. The aim of this test is to catch infant mortality problems in the front-end ASICs. The test is therefore performed at the first feasible stage, i.e. immediately after the ASICs are mounted on to the hybrids. (It should be noted that experience to-date has shown no long-term failures of ASICs).

The test consists of a long duration run at elevated temperature. The temperature and length of the run will be adjusted during production in the light of experience gained, but initially a 100 hour test will be made with a temperature measured by the hybrid thermistors of 45^{o}C. During the test the hybrids are powered, clocked and configured and triggered at the nominal L1A trigger frequency of 100kHz. The currents drawn by, and the temperatures of, the hybrids are monitored every few minutes. Every few hours a test to establish correct functionality of the hybrid is performed, so that if problems do develop the time structure of the failures can be observed.

2.1.4 Final Electrical Test of Hybrids

After the long term test, the ASICs are bonded to the hybrid pitch adapter. A final electrical Confirmation Sequence (see section 3.3) is performed to ensure that no inadvertent damage has been caused.

2.2 Construction of the Baseboard – Detector Sandwich

Before delivery to the assembly site, the individual components have already been subject to QA procedures as described in SCT-BM-FDR-5.1 for the Detectors and in SCT-BM-FDR-5.2 for the Baseboards.

2.2.1 Visual Inspection

Before use, the four silicon detectors and the baseboard are all visually inspected to ensure that no damage has occurred in transit. The criteria for detector acceptance is the same as on their first delivery from the contractor. The baseboard is checked to ensure that it is free from any cracks or defects.

Following the gluing of the detectors to the baseboard, the assembly is checked visually.

2.2.2 Detector Leakage Currents

After the detectors are glued to the baseboard, the I-V curve is recorded for each detector individually up to a bias of 500V. If any current (normalised to 20°C) at 500V bias differs by more than 1μA from that last recorded in the database for the detector, the assembly is put to one side for further visual checks and current stability measurements.

2.2.3 Metrology

The full set of metrology survey measurements (see section 3.2) is performed on the baseboard-detector assembly. If the results are outside specification the assembly is rejected.

2.3 Mounting the Hybrid

2.3.1 Electrical Check of Hybrid

On receipt at the module assembly site, the hybrid is checked for its continued correct electrical functionality before mounting on the module. This is done with the Confirmation Sequence as described in Section 3.3.

The glass fan-in on the hybrid is also checked visually for any damage.

2.3.2 Detector Leakage Current Check

After the hybrid is mounted on the module, the detector bias is bonded, and the leakage current checked up to 500V bias. This is a diagnostic step, to establish whether any subsequent leakage current problems that may be observed have occurred before or after the detector strip bonding.

3 QA OF THE COMPLETED MODULE

The following QA steps are performed on fully assembled modules. The criteria for accepting a module as 'good' are for initial use, and will evolve with experience.

3.1 Leakage Current Tests of Each Completed Module

3.1.1 I-V Scan to 500V

With the ASICs unpowered, the detector I-V curve of the completed module is recorded up to 500V bias at room temperature. For a good module, the total leakage current of the module will differ from the sum of those for the four individual detectors by no more than 4μA at 500V. Outside this limit, the module will be visually inspected for any signs of damage to the detectors, and subjected to long-term current tests at a range of bias voltages.

3.1.2 Long Term Leakage Current Stability

All modules will be tested for long-term leakage current stability over a 24 hour period in an environmental chamber containing cold dry air (nitrogen). The ASICs are powered, clocked and triggered, and the detector bias is maintained at 150V, with the

current monitored every 15 minutes over the period. The temperature is adjusted so that it is -10°C measured by the hybrid thermistors. The maximum increase in leakage current over the period should be less than 4μA for a good module, after an initial settling time of 5 minutes.

This test can be performed in parallel with the long-term electrical test on modules, section 3.5 below.

3.2 Metrology

After completing the detector-baseboard assembly or the assembly of module, the object will be surveyed for mechanical precision. The precision is characterised by in-plane and out-of-plane parameters. For the in-plane survey, a well-defined set of fiducial marks on the sensors is used. For the out-of-plane survey, a matrix of points with equal spacing is measured. A 3D measuring machine is required for the out-of-plane survey

3.2.1 In-Plane Survey

The in-plane survey characterises the relative positions of the four sensors and the dowel hole/slot of the baseboard. Figure 1 shows a typical setup for the measurement. A module is placed on a frame and is held at three points. The frame has a number of transparent fiducials so that the measurements of the front and the back sides can be correlated.

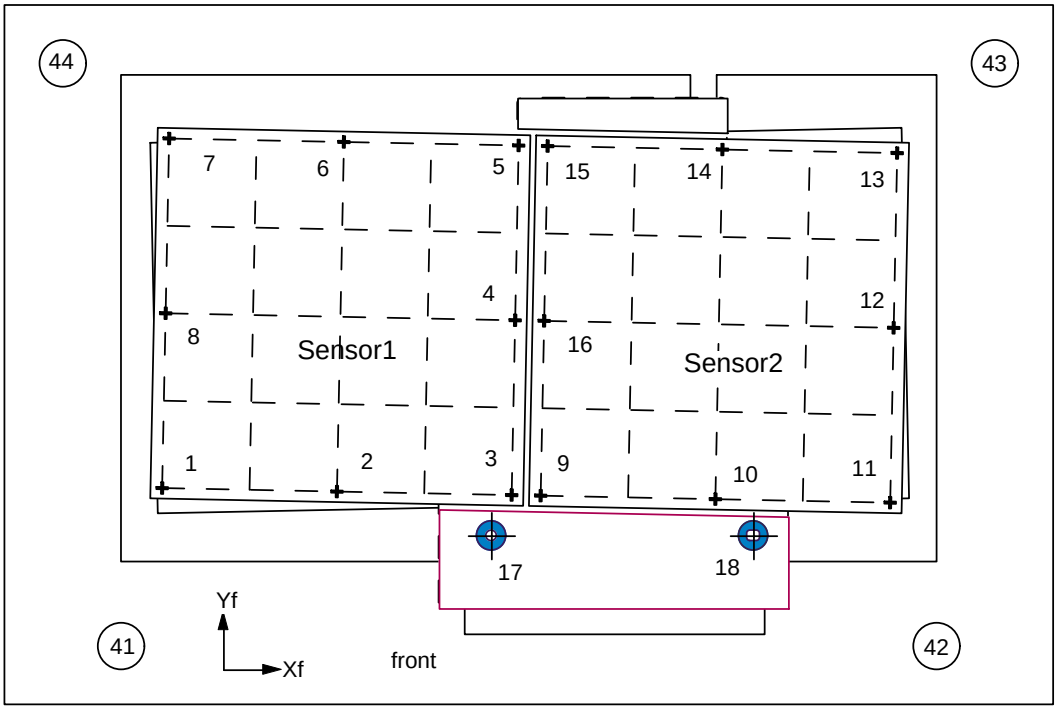
The x and y coordinates of a sensor are obtained from the measurements of the nine fiducial marks *A* (see SCT-BM-FDR-5.2 for their description). The reduced parameter set, however, does not rely in the end on which fiducial marks are used. For the front side, the centres of the dowel hole and slot are obtained from the measurements of the perimeter of the hole and the slot.

From the 34 (x,y) coordinates measured, the module coordinate and a reduced parameter set are obtained as shown in Figure 2. The coordinate origin is the geometrical centre of four sensors. The stereo angle is that between the axis of the front pair, C1C2, and the back pair, C3C4, where C1 to C4 are the geometrical centres of sensors1 to 4, respectively. The half-stereo angle defines the x coordinate, X_m, and then the y coordinate, Y_m. In this coordinate system, the reduced parameter set is listed in Table 1, with the design values and the tolerances specified.

3.2.2 Out-of-Plane Survey

The surface of the module is measured at a matrix of 5x5 points for each sensor with a 3D measuring machine having a z measurement precision of better than 10 μm. In addition to the surface points on the sensors, three points Z1, Z2, and Z3 are measured on the surfaces of the cooling contact and the far-end BeO facings on the back side of the module, as shown in Figure 1. The three points define the *module plane* as mounted on the bracket on the barrel cylinder. The locations of Z1 and Z2 are close to the dowel hole and slot, while Z3 is near the third module mounting point. The front-back correlation is made through the measurement of the transparent fiducials on the frame. There are in total 100 (x, y, z) data points for which the (x,y) module coordinates are defined in the in-plane survey, and the z coordinate with the origin at the centre of the module calculated from the *module plane*.

The out-of-plane tolerances are constrained by two factors; the requirement to keep at least a 1mm `stay clear' distance between modules mounted on the barrel (see SCT-BM-FDR-4, section 4), and the physics tracking requirement for the residuals in z-flatness. These are discussed in Appendix 1. For the `stay clear' distance, the requirements for a good module is



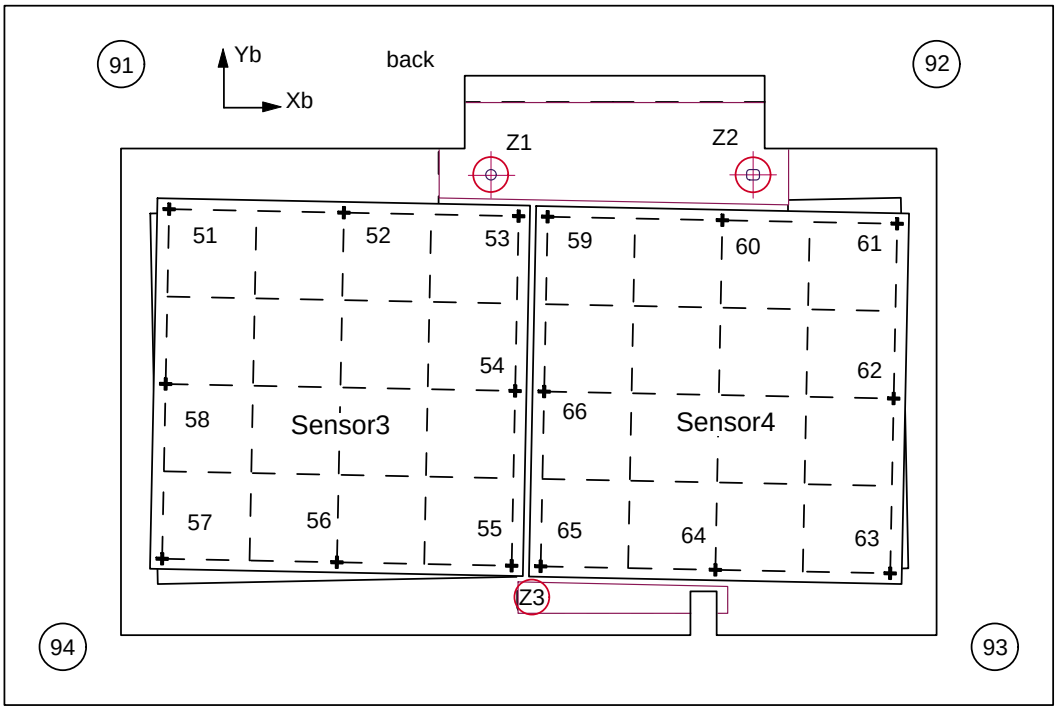


Figure 1 Survey points on a barrel module. Sensors 1 and 3 are on the left when the module is drawn in the conventional orientation. "+" represents the fiducial mark A on the sensors. Points 1-18, 41-44, and 51-66 are for the in-plane survey. Point 17 is the centre of the mounting hole and Point 18 of the mounting slot. For the out-of-plane survey, points on a 5x5 matrix are measured for a sensor, in addition to the points Z1, Z2, and Z3 in the back in order to define the module reference plane. Points 41-44 and 91-94 are transparent fiducials to correlate the measurements of the front and the back sides.

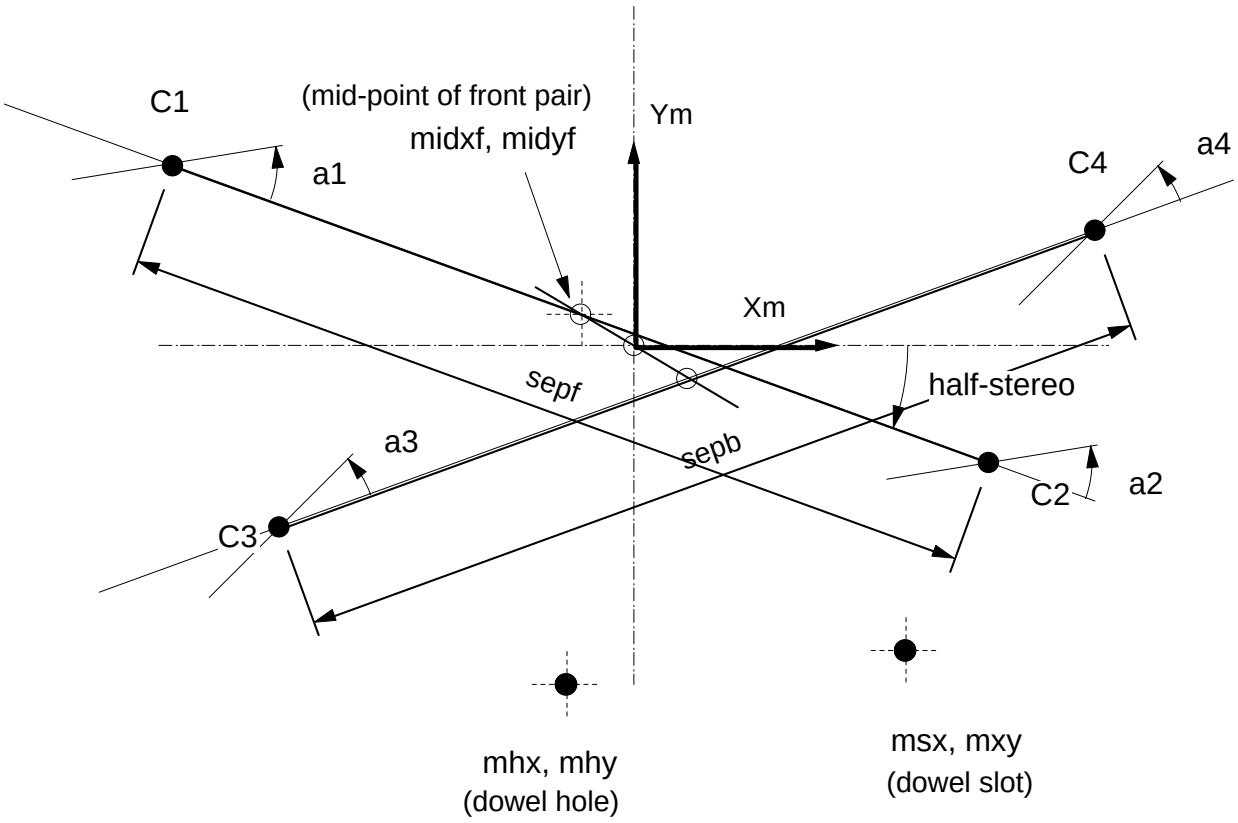


Figure 2 Definition of the parameters which describe the geometry of a module. The black circles C1 to C4 are the measured centres of the four sensors. The dashed line through each centre gives the measured orientation of each sensor. Open circles are the centre points of lines. The module is described in the database by 13 numbers: the coordinate pairs of the dowel hole, slot, and centre of front/back pair: (mhx, mhy), (msx, msy) and (midxf, midyf), the sensor separations: sepf, sepb, sensor angles: a1, a2, a3, a4, and the half-stereo angle. The stereo angle is measured from the X_m axis and sensor angles from the stereo axis, with anti-clockwise rotation being positive.

that the maximum height of a sensor surface from the nominal should be < 200 μm. The requirement on the residuals in z-flatness, after `minimal use' (see Appendix 1) of z data, is that the value should be < 50 μm.

Parameter	Design Value	Tolerance
Dowel hole, mhx [µm]	-6500	30
Dowel hole, mhy [µm]	-37000	30
Dowel slot, msx [µm]	38500	100
Dowel slot, msy [µm]	-37000	30
Mid-point of front pair, midxf [µm]	0	10
Mid-point of front pair, midyf [µm]	0	5
Separation of front pair, sepf [µm]	64090	10
Separation of back pair, sepb [µm]	64090	10
Sensor1 angle, a1 [mrad]	0	0.13
Sensor2 angle, a2 [mrad]	0	0.13
Sensor3 angle, a3 [mrad]	0	0.13
Sensor4 angle, a4 [mrad]	0	0.13
Half stereo angle, half-stereo [mrad]	-20	0.13

Table 1: Module in-plane geometry parameters

3.3 Electrical Tests

An extensive suite of both hardware and software[1] has been developed to facilitate module testing. The readout system is based around the VME modules CLOAC, MuSTARD and SLOG. The prototype low voltage and high voltage modules, SCTLV and SCTHV, are also part of the system.

Two largely automated series of tests[2] have been devised to simplify the testing procedure, as outlined in table 1. The *Characterisation Sequence* aims to perform the full characterisation of a hybrid or module whereas the shorter *Confirmation Sequence* provides a reduced set of information. The *Confirmation Sequence* ensures that the digital part of the ASICs is functioning, none of the critical wire-bonds have been damaged and that the basic analogue performance of a module has not deteriorated. It is anticipated that the *Confirmation Sequence* would be repeated at regular intervals during the long-term tests and each time that a hybrid or module is shipped between institutes.

[1] http://sct.home.cern.ch/sct/sctdaq.html

[2] The tests are described fully in http://hepwww.rl.ac.uk/atlas-sct/documents/Electrical_Tests.htm

	Characterisation	Confirmation
Power On Tests / Verification of Response to Hard Reset	√	
Clock and Command Reception Test	√	√
Bypass Functionality Test	√	√
Pipeline Efficiency Test	√	
Strobe Delay Scan	√	√
Three Point Estimation of Gain, Noise and Offset	√	√
TrimRange Scan	√	
Determination of the Response Curve	√	
Noise Occupancy Scan	√	
Timewalk Scan	√	

Table 1: The Characterisation and Confirmation Sequences

In general, the analogue performance of a module/hybrid is measured with respect to the internal calibration circuitry of the ABCD3T chip. Hence it is necessary to make a correction for the variation of the calibration capacitance between batches of ASIC wafers.

There follows a brief description of the individual tests to be performed as part of the electrical QA procedure. The description contains the method in general terms, the purpose of the tests and in quantitative terms the criteria for PASS/FAIL cuts. A summary of the results of each test will be recorded in the SCT database.

A module is classed as `good' if at least 99% of its readout strips will operate efficiently with low noise occupancy at 1fC threshold.

3.3.1 Power on Tests / Verification of Response to Hard Reset

The module/hybrid is clocked and the power is switched on. The operator must verify that each data-link responds with CLK/2 and that, after the chips have been configured, the clock feed-through signal stops. The analogue and digital currents are then recorded. Finally Hard Reset is issued to bring back the CLK/2 signal.

This test verifies that the Clock, Command and Hard Reset signals are received correctly, that the chips can be configured and that the current consumption is reasonable. The test will identify modules/hybrids with severe failures. Every module must pass this test without error.

This is the only test that would normally require operator intervention.

3.3.2 Clock and Command Reception / Addressing Error Test

The chips are configured to return the contents of the Mask Register and a burst of triggers is issued for each of the Primary and Redundant Clock and Command options. Prior to each event, a different bit pattern is loaded in the Mask Register such that consecutive events are not the same.

By comparing the received data with expectation it is verified that both the Primary and Redundant Clock and Command signals are received correctly and that the top address bit of each chip changes as the Clock/Command source is varied, as specified in the

module design. This test will identify modules/hybrids with faulty command reception or addressing errors. Modules/hybrids with such defects would be considered to have failed pending further investigation and possible rework.

3.3.3 Bypass Functionality Test

A trigger burst is recorded with the module/hybrid programmed to each of a number of different configurations, sufficient to exercise all data/token passing links between the chips. In each case the chips are configured to return the contents of the Mask Register such that the expected data is accurately known. The test is repeated across a range of digital supply voltages.

This test determines the minimum value of the digital supply voltage needed for each of the data/token passing links to work. Any link that did not work at the designated supply voltage, and which could not be identified as being due to a missing wirebond and subsequently repaired, would cause a module/hybrid to be rejected.

3.3.4 Pipeline Efficiency Test

For this test, a Soft Reset command is sent to reset the pipeline followed a certain number of clock periods later by a Pulse Input Register command and L1A trigger. In this way, a known pattern is injected into a given location in the pipeline. By varying the distance between the Soft Reset and Pulse Input Register commands it can be verified that each of the eleven blocks within the pipeline is free of defects.

Zero occupancy for a particular number of clock periods between the Soft Reset and Pulse Input Register commands would indicate a dead cell in the corresponding block of the pipeline. Zero occupancy for all values would indicate a dead channel. Modules/hybrids with a large number of dead Pipeline cells or dead channels will be rejected.

3.3.5 Strobe Delay Scan

This scan is performed to determine the correct Strobe Delay setting, corresponding to the timing of the charge injection pulse, to be used during the Analogue Tests.

3.3.6 Three Point Estimation of Gain, Noise and Offset

Threshold scans are taken for three injected charges to facilitate a quick measurement of gain, noise and the discriminator offset. Pathological channels are categorised as FAULTY if the defect would result in the channel having a reduced but non-zero detection efficiency in ATLAS, or as LOST if the defect would result in the channel having zero efficiency:

- **Lost: Dead, Stuck, Unbonded or Noisy channels**
- **Faulty: Inefficient, Low Gain or Partially Bonded channels**

Modules/hybrids having any chips with abnormal gain or high noise will be rejected, for potential re-work, as will those with large numbers of pathological channels.

3.3.7 Trim Range Scan

For each of the four possible TrimRange settings, a series of Threshold scans are performed for a subset of the sixteen possible TrimDAC settings, all with 1fC injected charge. For each TrimRange setting a straight line is fitted to the data for each channel to characterise the TrimDAC response and to determine the TrimDAC slope. The number of trimmable channels and the spread of the resultant trimmed thresholds are also recorded. The optimised TrimDAC settings and a list of channels to be masked are produced for use in the subsequent analogue tests.

The chips used to build modules will have been selected such that all channels may be trimmed using the smallest TrimRange. Modules which do not meet this specification on at least 99% of channels will be rejected, for potential rework, as will those where a particular TrimRange has a slope other than that expected.

3.3.8 Response Curve

Threshold scans are performed for a series of input charges and, for each channel, an appropriate function is fitted to the resulting response curve. From this the Gain, Noise and discriminator Offset are extracted.

The parameters from the fit are stored since they describe the correspondence between the Threshold, in mV, and input charge, in fC. The categorisation of pathological channels is repeated as described for the Three Point Gain. Modules/hybrids with a large number of pathological channels will be rejected.

3.3.9 Noise Occupancy Scan

A high statistics Threshold scan is performed at the nominal ATLAS trigger rate of 100kHz, without any injected charge, to determine the Noise Occupancy of each channel as a function of Threshold. The analogue and digital current consumption as a function of Threshold is recorded.

Channels with high Noise Occupancy will be added to the list of masked channels.

3.3.10 Timewalk Scan

This test performs a series of Strobe Delay scans with the Threshold set to 1 fC, varying the input charge from 1.25 to 10 fC. In each case a fit is made to the rising edge of the pulse to determine the Strobe Delay value needed to obtain 50% occupancy.

The Timewalk is defined as the time variation in the crossing of a threshold of 1fC over a signal range of 1.25 to 10.0fC. This parameter is calculated and recorded.

3.4 Thermal cycling

For every module a thermal cycle from -30^{o} to +50^{o}C will be carried out ten times, in an inert atmosphere. The module(s) will be placed inside an environmental test chamber and purged with nitrogen for sufficient time to achieve at least 3 volume changes within the chamber. During the test, each module will be clocked and triggered and the ASIC currents will be checked. The test cycle will start and end at room temperature and the first temperature excursion will be to +50^{o}C. The ramp up/down times will be approximately 30 minutes (2-3^{o}C/minute) and the soak time about 30 minutes at each temperature. The total test time will therefore be about 20 hours. This test could also be extended to carry out long-term electrical tests at the operating temperature.

3.5 Long-term electrical test

In addition to detailed electrical testing and characterisation, a longer duration test will be performed on assembled modules at the ATLAS operating temperature. This test verifies that modules will function electrically at reduced temperatures.

The test consists of an extended (24 hour) run at reduced temperature, defined to be –10^{o}C as measured by the hybrid thermistors. During the test the hybrids are clocked and triggered. The currents drawn by, and the temperatures of, the hybrids are monitored continuously. Every few hours a *Confirmation Sequence* is performed. At the end of the test, a *Characterisation Sequence* is performed while the modules are kept cold.

This test may be performed in parallel with the long-term leakage test (section 3.1.2).

4 SAMPLING QA ON COMPLETED MODULES

The fraction of modules to be used initially for the sub-sample tests is indicated in each of the following sections.

4.2 Irradiation Tests

A very small sample of the completed barrel modules (approximately 10 per annum during the construction period) will be fully and uniformly irradiated in the SCT facility at the CERN PS to a fluence of 3x10^{14} pcm^{-2} 24 GeV/c protons. They will be annealed for 7 days at 25^{o}C following the irradiation and then checked for mechanical integrity and for noise performance, for full ASIC functionality and for detector leakage current when run cold at the SCT operating temperature. Several of these modules will also be tested in the beam for signal:noise and efficiency performance.

4.3 Readout Performance with Particles

4.3.1 Beam Tests

A small number (approximately 20 per annum during the construction period) of the barrel modules will be fully tested in the H8 beam at CERN, with a magnetic field and

with varying angles of incidence of the particles to check their continued performance characteristics. Modules will also be tested in the beam at KEK.

4.3.2 Source Tests

It is anticipated that a fraction of the modules will, at least initially, be read out in the laboratory when exposed to a Ru^{106} beta source. This will allow signal:noise values to be confirmed for the different batches of delivered ASICs.

4.3.3 Laser Tests

A subset of the produced modules may also be submitted to scanning Laser tests. A focused LASER of wavelength e.g. 1050 nm is mounted on a x-y stage and scanned over the module. This test provides very precise position information, hence the correct functionality of all channels can be verified.

5 SUMMARY

The QA procedures for the Barrel SCT module are designed to ensure the quality and performance for each individual module produced. They should cover all aspects of the module, such as mechanical tolerances, electrical performance and long-term stability. These goals should be achieved uniformly during the production cycle, regardless of production site, for all batches of constituent components and for the assembled modules..

Appendix 1: Tolerances on Out-of-Plane Metrology Data

One limitation on the out-of-plane data comes from the `stay clear' distance required between the surfaces of adjacent modules, see SCT-BM-FDR-4, section 4. To ensure a 1.0 mm stay clear distance, the maximum allowed out-of-plane deviation of a module from the nominal is 200 μm.

With the `optimal use' of the 100 metrology data points per module in a reconstruction program, i.e., 100 points times 2112 barrel modules, no further requirement is necessary for the out-of-plane tolerance. However, this cannot be regarded as practical solution.

`No use' of the z metrology data would require the module z-deviations from perfect flatness to be limited to the value allowed from the physics requirements, which is less than about 50 μm. From the experience of the modules so far constructed, `no use' is not a practical solution as there is intrinsic bowing in the sensors and in the baseboards.

The `minimal use' of z data is the procedure adopted, and this is carried out in two steps:

(1) The `mid-plane' calculated from the top and the bottom surface of the sensors is fitted (separately in the left and the right side sensors) to a plane, $z = ax + by + c$. These 6 parameters per module express any asymmetry in the construction or non-planar properties of the baseboard for the module.

(2) The `common profile' of the surface is calculated at the 100 measured points. Thus, 100 points express the bowing of the sensors, common to all modules which use sensors from a particular vendor.

After the above two corrections, the residual is regarded as the error in z-flatness, which has to be smaller than the tolerance from the physics requirements.