SCT Barrel Module FDR Document

SCT Barrel Module : ASICs

Abstract

This document summarises the requirements and target design specifications for the front-end ASIC (ABCD3T), procedures and criteria used for qualification of the ABCD3T chips and parameters of the ABCD3T chips delivered to the SCT Production Database.

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History of Changes

Rev. No.	***Date***	***Pages***	***Description of Changes***
1	22/04/01	30	
2	30/04/01	31	Brief description of ABCD2T, ABCD3T and ABCD3TA versions added.

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1 SCOPE OF THE DOCUMENT

In this document we summarise:

- **the requirements and target design specifications for the front-end ASIC (ABCD3T) to be used in the binary readout architecture of silicon strip detectors in the ATLAS Semiconductor Tracker (SCT),**
- **procedures and criteria used for qualification of the ABCD3T chips,**
- **parameters and characteristics of the ABCD3T chips delivered to the SCT Production Database.**

The content of this document is based on two working documents on ASICs, in which more detailed information is available:

1. **ABCD Chip, Project Specification, Version V1.2.**
2. **Testing specification for the wafer screening. Project Name: ABCD3T ASIC. Version: V1.4, 20 April, 2001.**

The ABCD3T design is based upon the ABCD2T prototype chip which was a major step in development of the front-end ASIC. Satisfactory matching of thresholds, a critical parameter for the binary architecture, has been achieved in the ABCD2T design by implementation of individual threshold correction in every channel using 4-bit digital-to-analogue converter (TrimDAC) per channel. The ABCD2T version has met all basic requirements of the ATLAS SCT, however, in the front-end circuit we have identified two points which compromised performance of that prototype, namely: (i) the internal calibration circuitry showed non-linearity for low input charges, (ii) TrimDACs response curves appeared to be non-linear and exhibited large spread from channel-to-channel. Furthermore, extensive radiation tests showed that after proton irradiation up to a fluence of 3×10^{14} cm^{-2} the spread of the threshold offsets increased by a factor of 3 and exceeded the range of the TrimDACs.

The sources of non-linearity of the calibration circuit and of the TrimDAC circuit have been identified and the designs of these two blocks have been corrected in the ABCD3T version. The resolution of the TrimDAC in the ABCD3T design remains 4 bits. In order to not compromise the resolution of the TrimDAC, i.e. achievable uniformity of thresholds for non-irradiated chips, and to guarantee that for fully irradiated chips all the channels can be corrected, 4 selectable ranges of the TrimDAC have been implemented in the ABCD3T design.

Irradiation tests of the ABCD3T chips showed that the circuitry responsible for loading the range of the TrimDAC was not sufficiently robust and in some fraction of chips the required ranges could not be loaded correctly. A minor correction in the design, resulting in the ABCD3TA version, has been implemented after receiving two batches of the pre-production series. In the second part of the pre-production series the ABCD3TA version was manufactured. The correction implemented in the ABCD3TA has absolutely no impact on the chip performance before irradiation and it is not visible for the users at all as long as the basic range of the TrimDAC is used.

2 DESIGN SPECIFICATION OF THE ABCD3T IC.

2.1 REQUIREMENTS

2.1.1 GENERAL

The chip must provide all functions required for processing of signal from 128 strips of a silicon strip detector in the ATLAS experiment employing the binary readout architecture. The simplified block diagram of the chip is shown in Figure 2.1. The main functional blocks are:

front-end, input register, pipeline, derandomizing buffer, command decoder, readout logic, threshold&calibration control.

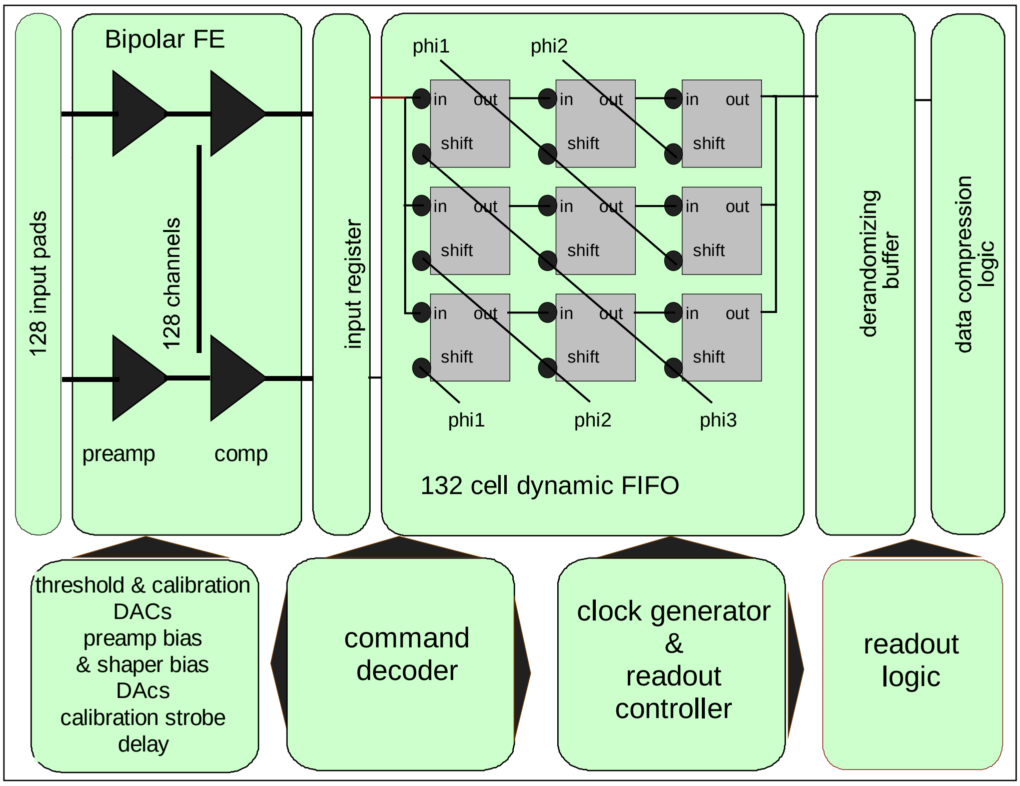

Figure 2.1: Block diagram of the ABCD3T IC.

2.1.2 SIGNAL PROCESSING.

The chip must contain following functions:

- **Charge integration**
- **Pulse shaping**
- **Amplitude discrimination. The threshold value for the amplitude discrimination is provided as a differential voltage either from internal programmable DAC or from an external source.**
- **The outputs of the discriminators must be latched either in the edge sensing mode or in the level sensing mode.**
- **At the start of each clock cycle the chip must sample the outputs from the discriminators and store these values in a pipeline until a decision can be made whether to keep the data.**
- **Upon receipt of a L1 Trigger signal the corresponding set of values together with its neighbours are to be copied into the readout buffer serving as a derandomizing buffer.**
- **The data written into the readout buffer is to be compressed before being transmitted off the chip.**
- **Transmission of data from the chip will be by means of token passing and must be compatible with the ATLAS protocol.**
- **The chip is required to provide reporting of some of the errors that occur:**
- **Attempt to read out data from the chip when no data is available.**
- **Readout Buffer Overflow: The readout buffer is full and data from the oldest event(s) has been overwritten.**
- **Readout Buffer Error: The readout buffer is no longer able to keep track of the data held in it. (Chip reset required).**

- **Configuration error (ChipID sent).**
- **The chip shall incorporate features that will enable the system to continue operating in the event of a single chip failure.**

It is a system requirement that the fraction of data which is lost due to the readout buffer on the chip being full is less than 1%. This assumes that on average only 1% of the silicon strip detectors are hit during any particular beam crossing.

2.1.3 CALIBRATION AND TESTABILITY.

Each channel has an internal Calibration Capacitor connected to its input for purposes of simulating a "hit" strip. The Calibration Capacitors are charged by an internal chopper circuit which is triggered by a command. Every fourth channel can be tested simultaneously with group selection determined by two binary coded Calibration Address inputs (CALD0, CALD1). The strobe and the address signals are delivered from the control circuitry. The voltage applied to the Calibration Capacitors by the chopper is determined by an internal DAC. The four calibration bus lines, each of which connects the calibration capacitors of every fourth channel, are also brought out to pads which can be directly driven with an AC coupled voltage step. This is intended for use during IC testing. A tuneable delay of the calibration strobe with respect to the clock phase covering at least two clock periods must be provided. The chip must incorporate such features that will enable to test and calibrate it either on the wafer level or in situ.

2.2 DESIGN SPECIFICATION

2.2.1 DETECTOR PARAMETERS

The parameters of the analogue front-end part are specified for the electrical parameters of 12.8 cm long p-type silicon strip detector. The assumed detector parameters are listed in Table 1.

Table 2.1: Assumed detector electrical parameters.

	Unirradiated	Irradiated
Coupling type to amplifier	AC	AC
Coupling capacitance to amp Total for 12 cm strips	20 pF/cm 240 pF	20 pF/cm 240 pF
Capacitance of strip to all neighbour strips	1.03 pF/cm	1.40 pF/cm
Capacitance of strip to backplane	0.30 pF/cm	0.30 pF/cm
Metal strip resistance	15 Ω/cm	15 Ω/cm
Bias Resistor	0.75 MΩ	0.75 MΩ
Max leakage current per strip for shot noise	2.0 nA	2.0 μA
Charge collection time	< 10 ns	< 10 ns

2.2.2 FRONT-END

2.2.2.1 ELECTRICAL REQUIREMENTS:

Note that notation convention for currents used in the entire specification is "+" for current going into (sunk by) the chip and "-" for current going out of (sourced from) the chip.

2.2.2.2 INPUT CHARACTERISTICS:

Input Signal Polarity: **Positive signals from p-type strips.**

Crosstalk: **< 5% (via detector interstrip capacitance)**

Input Protection: **Must sustain voltage step of 450 V of either polarity with a cumulative charge of 5 nC in 25 ns.**

Open Inputs: **Any signal input can be open without affecting performance of other channels.**

Max Parasitic Leakage Current: **100 nA DC per channel with < 10 % change in gain at 1 fC input charge.**

2.2.2.3 PREAMPLIFIER-SHAPER CHARACTERISTICS

Gain at the discriminator input: **50 mV/fC for the nominal shaper current of 20 μA and the nominal process parameters**

Linearity: **better than 5% in the range 0 - 4 fC**

Peaking time: **20 ns**

Noise: Maximum rms noise for nominal components as measured on fully populated modules

<= 1500 electrons rms for unirradiated module

<= 1800 electrons rms for irradiated module

Gain Sensitivity to VCC for 1 fC signal: 1%/100mV

2.2.2.4 COMPARATOR STAGE:

A threshold is applied as a differential voltage offset to the comparator stage. This threshold voltage is applied from an internal DAC in the normal operation mode or can be applied from the external pads for test purposes.

Threshold setting range: **0 fC to 12.8 fC , nominal setting at 1 fC**

Threshold setting step: **0.05 fC of input charge around nominal threshold of 1 fC**

Threshold variation at 1 fC: **(1 sigma) channel to channel matching within one chip vs Range Set of TrimDACs by 2 bits in the Configuration Register.**

min (00)	**2.5%**
x2 (01)	**5.0%**
x3 (10)	**7.5%**
x4 (11)	**10%**

2.2.2.5 TIMING REQUIREMENTS:

Timewalk: **<= 16 ns. This specification depends on the precision of the digital acquisition latch edge. Good alignment, 1 or 2 ns over a common clocked array of channels implies a longer timewalk assignment to the rising edge of the shaped signal.**

Timewalk defined: **The maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 to 10 fC, with the comparator threshold set to 1 fC.**

Double Pulse Resolution: **<= 50 ns for a 3.5 fC signal followed by a 3.5 fC signal**

Max recovery time for a 3.5 fC signal following a 80 fC signal: 1 μs

2.2.2.6 THRESHOLD GENERATION CIRCUIT

Differential voltage for the discriminator threshold is generated by an internal DAC circuit (Threshold DAC). The threshold voltages generated by the internal circuit are applied to the same pads VTHP and VTHN to which the external threshold is applied. When the external threshold is not applied the internal threshold voltage can be measured at pads VTHP and VTHN.

Range: **0 - 640 mV**

Step value: **2.5 mV**

Absolute accuracy: 1%

2.2.2.7 CALIBRATION CIRCUIT CHARACTERISTICS

Calibration signal can be applied to one of the four calibration lines via the external pads or from the internal calibration circuit. In the later case the address of the calibration line, the amplitude of the calibration signal and its delay is set via the control logic.

Calibration Capacitors:	**100 fF ±20% (3 sigma) over full production skew ±2% (3 sigma) within one chip.**
Calibration signal:	
amplitude range:	**0 - 160 mV (charge range: 0 - 16 fC)**
amplitude step:	**0.625 mV (charge step: 0.0625 fC)**
Absolute accuracy of amplitude:	**5% (full process skew)**
Relative accuracy of amplitude:	**< 2 % (for known values of calibration capacitors, amplitude range 0.8 to 4 fC, across one chip, including switching pickup, etc.)**
Relative accuracy of amplitude:	**< 10 % (for known values of calibration capacitors, amplitude range 0.8 to 8 fC, across one chip, including switching pickup, etc.)**

Calibration Strobe signal pickup at comparator should be less than 0.1 fC equivalent sensor input.

For test purposes, a voltage step can be applied directly to any one of the four groups of calibration capacitor via the input pads (CAL0, CAL1, CAL2, CAL3). When not used, these four pads must be left floating.

2.2.2.8 THRESHOLD CORRECTION CIRCUIT

In order to compensate channel-to-channel variation of the discriminator offset each channel is provided with a trim DAC of 4-bit resolution. Each channel can be addressed individually and the threshold correction can be applied channel by channel. The range of the trim DAC can be selected with two bits in the configuration register. This is to cover the offset spread which is expected to increase after irradiation. The selectable ranges and corresponding steps of the TrimDAC are:

Trim DAC range	**Trim DAC step**
0 mV - 60 mV	**4 mV**
0mV -120 mV	**8 mV**
0mV -180 mV	**12 mV**
0mV -240 mV	**16 mV**

2.2.3 DATA READOUT AND REDUNDANCY

The figure below shows the data and token interconnections on a typical silicon detector module. The module has 6-ABCD chips on each side. The datalink outputs of 2 of these chips are connected to a fibre-optic interface and are configured to act as Masters in controlling the readout of data from each side of the module. On the diagrams the Master chips are denoted by a “M” and all the other chips are configured to act as slaves as denoted by a “S” or "E' on the diagram.

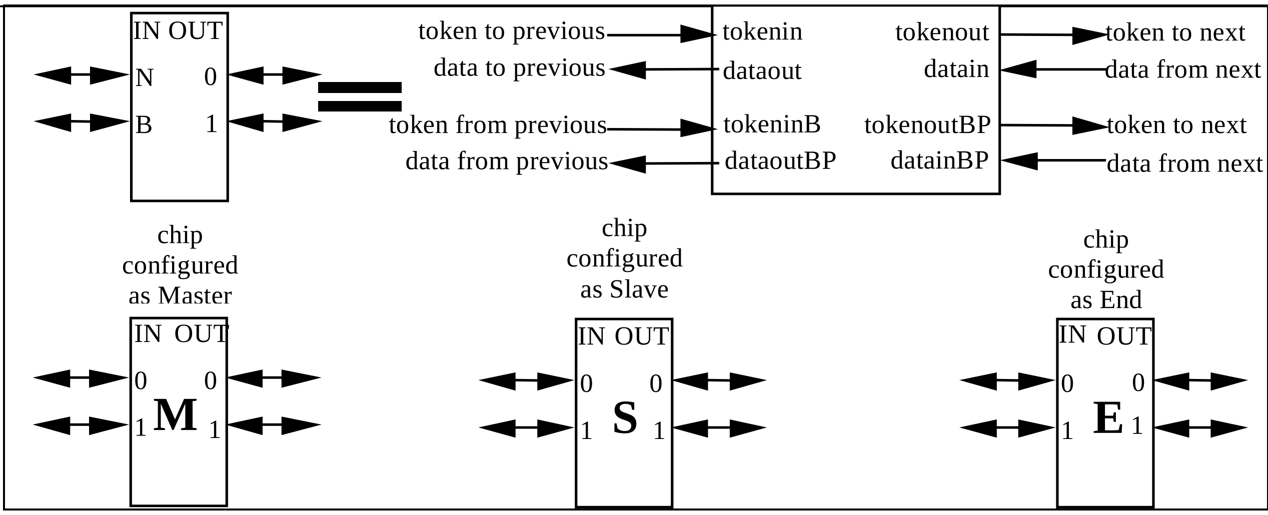

Figure 2.2: Key to symbols used in following Diagrams.

After the receipt of a L1 Trigger, the Master chip initiates a readout cycle by sending the pre-amble bits at the start of each data block to the optical link driver. It then appends its data bits to the output stream sent to the optical link driver. A few clock cycles before the last bit has been sent, it sends a token to the slave chip on it's right. The slave chip on the right responds by sending its data packet to the Master which in turn is appended to the pre-amble and data bits from the Master already sent to the optical link driver.

Once this slave chip has finished sending its data, it also passes on the token to the next chip on the right. The next chip on the right passes its data onto the previous chip on the left which in turn passes it back to the Master chip for transmission to the LED driver. This process continues until the last chip in the chain has sent its data.

A bit is set in the last chip in the chain to inform it that it is the last chip (these chips are shown as 'E' on the diagrams). When this chip has sent its data it appends a trailer to the end of the data stream. While the Master chip is outputting data, it is constantly looking for the trailer pattern which has been carefully chosen to be distinct from the data. Once it finds the trailer pattern, it knows that all the data from the event has been sent and it can start processing the next event.

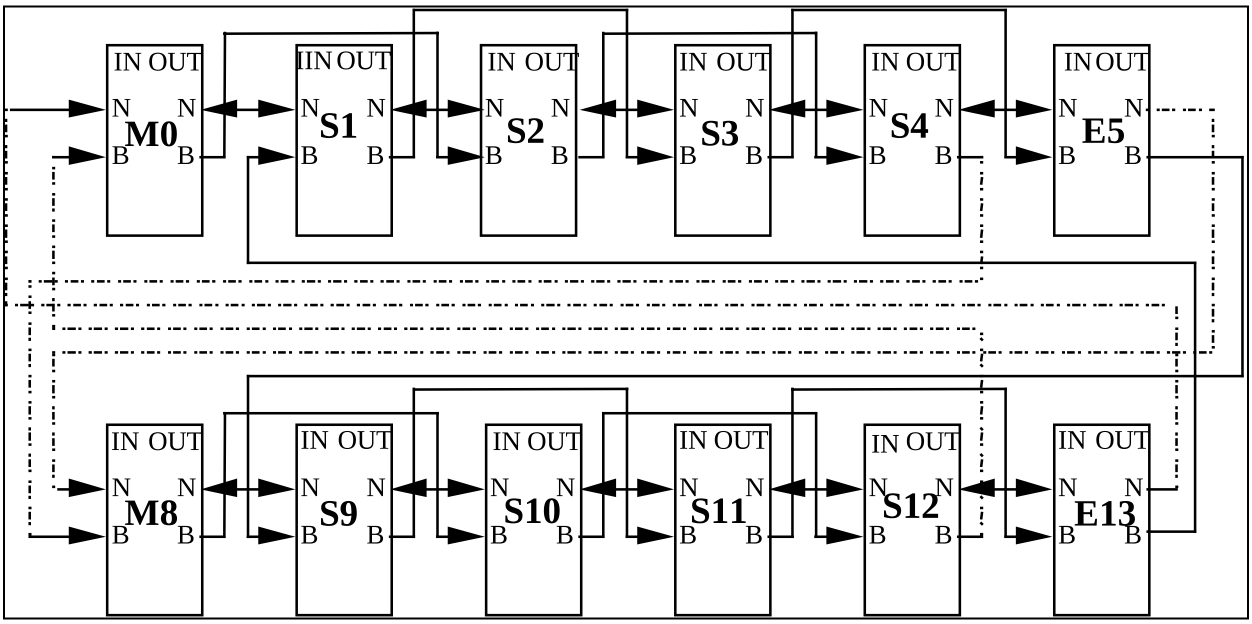

Figure 2.3: Diagram Showing the Interconnection of ABCD chips on a Silicon Detector Module.

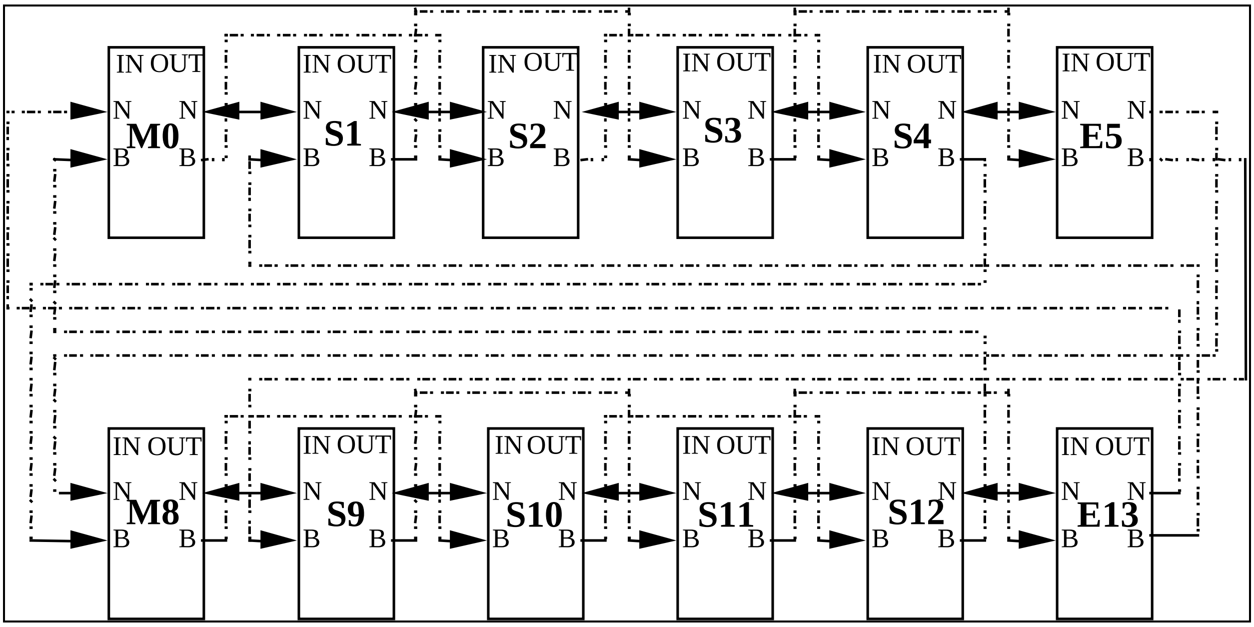

Figure 2.4: Diagram Showing the normal flow of Data and Tokens between chips. (Active links are highlighted with solid lines.)

In the event of the failure of one of the Slave chips, the previous and next slave chips in the chain are programmed to route their data and tokens around the failed chip. If the last chip in the chain should fail, then the penultimate chip in the chain is programmed to perform the operation of the "End chip".

In the event of the failure of a Master chip in the chain, the data and tokens from the chain with the failed Master chip are routed to the working master chip as shown in the next diagram .

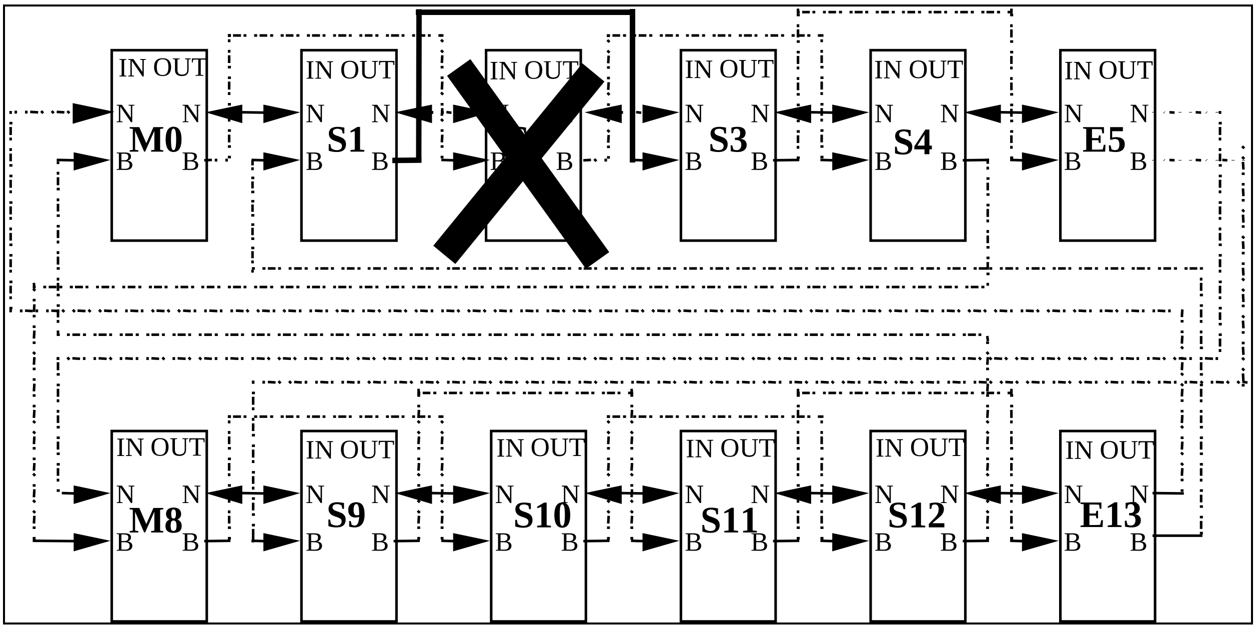

Figure 2.5: Diagram Showing the flow of Tokens and Data in the event of the failure of a Slave ABCD chip.

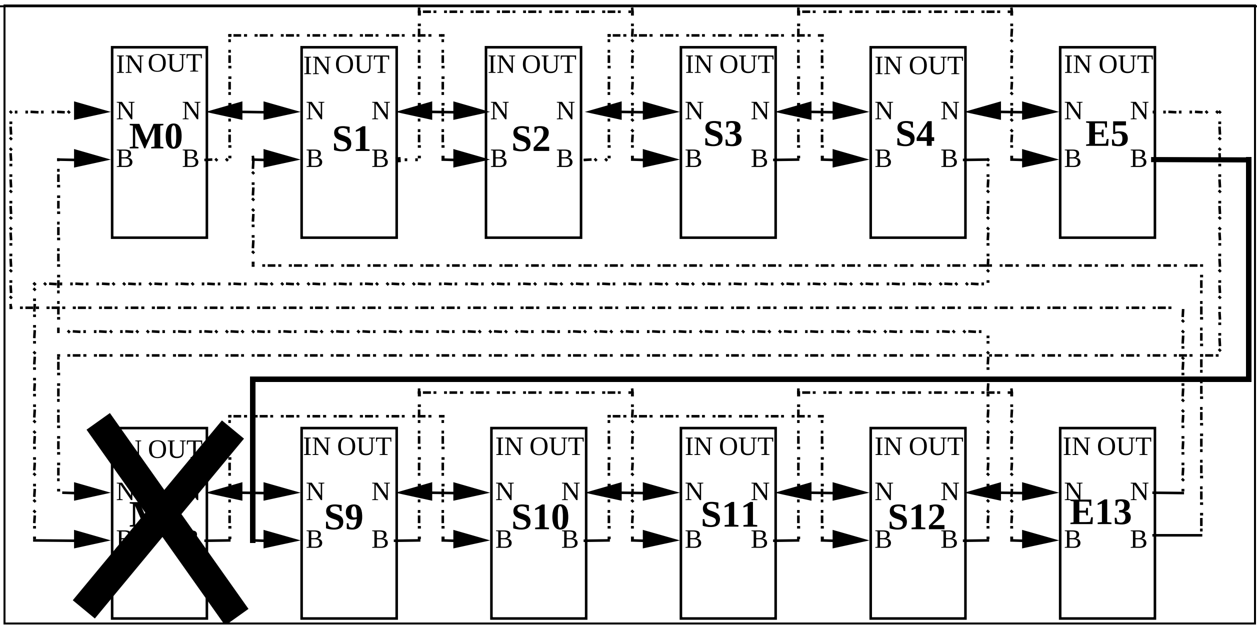

Figure 2.6: Diagram Showing the flow of Tokens and Data in the event of the failure of a Master ABCD chip.

2.2.3.1 MASTER/SLAVE SELECTION

The default state of the chip on power up is determined by the state on the masterB input pin. If this pin has been left unconnected or tied high, the chip will power-up as a Slave. If this pin has been tied to ground, the chip will power up as a Master. If the chip is configured as a Mater on power up it may be re-configured as a slave. However if the chip has been configured as a slave on power up it may not be re configured as a master.

2.2.4 INPUT/OUTPUT CONNECTIONS

The following tables describes the names and function of the various Input/Output connections to the chip.

Table 2.2: Input Signals.

Name	**Function**	**Type**
clk0 & clk1	Clock input	LVDS
clk0B & clk1B	Complement of above signal	LVDS
com0 & com1	Command Input	LVDS
com0B & com1B	Complement of above signal	LVDS
tokenin & tokeninBP	Token Input	Current Mode
tokeninB & tokeninBPB	Complement of above signal	Current Mode
datain & datainBP	Data Input	Current Mode
datainB & datainBPB	Complement of above signal	Current Mode
ID<5:0>	Geographical address of chip	CMOS
masterB	Sets chip default to master	CMOS
select	Selects clock/command inputs	CMOS
resetB	Resets Chip	CMOS

Table 2.3: Default settings of CMOS input signals.

Name	Function	Default setting
ID<4>	Geographical address of chip	Low, pull-down with 300 kOhm
ID<3:0>	Geographical address of chip	High, pull-up with 100 kOhm
masterB	Sets chip default to master	High, pull-up with 100 kOhm
select	Selects clock/command inputs	Low, pull-down with 300 kOhm
resetB	Resets Chip	High, pull-up with 300 kOhm

Table 2.4: Output Signals.

Name	Function	Type
tokenout, tokenoutBP	Token Output	Current Mode
tokenoutB, tokenoutBPB	Complement of above	Current Mode
dataout, dataoutBP	Data Output	Current Mode
dataoutB, dataoutBPB	Complement of above	Current Mode
datalink	Data Output to optical link driver	LVDS
datalinkB	Complement of above	LVDS

2.2.5 DC SUPPLY AND CONTROL CHARACTERISTICS:

Table 2.5: DC supply voltages.

	Pad Name	**Absolute Min**	**Min**	**Nominal**	**Max**	**Absolute Max**
Analogue Supply	VCC	0 V	3.3 V	3.5 V	3.7 V	5.5 V
Analogue Ground	GNDA			0 V		
Input transistor current*	Set by internal DAC	0 µA	100 µA	200 µA	300 µA	400 µA
Input transistor current monitor	IP_PR	$V_{ip} = I_p$ x 250 Ω				
Shaper current *	Set by internal DAC	0 µA	10 µA	15 µA	30 µA	50 µA
Shaper current monitor	IS_PR	$V_{is} = I_{sh}$ x 10 kΩ				
Discriminator threshold	VTHP	0 V	3.3 V	3.5 V	3.7 V	VCC
Discriminator threshold	VTHN	0 V	3.25 V	3.45 V	3.65 V	VCC
(VTHP - VTHN)		0 V	0 V	0.05 V	0.5 V	1.0 V
Digital Supply **	VDD	0 V	3.8 V	4.0 V	4.2 V	5.5 V
Digital Ground	DGND			0 V		

*** The Min/Max values define the range of the bias currents for which the front-end circuit will be biased correctly and will amplify the input signal. The absolute Min/Max values are the values which can be delivered from the internal DACs. The absolute Max values cover the worst case combination of corner process parameters and operating conditions.**

**** For the on chip power-up reset to operate correctly the VDD power supply must be ramped up to 90% of its final value in less than 10 ms.**

The current draw at each DC input is as follows.

Table 2.6: DC supply currents for the nominal voltage supplies (VCC=3.5V, VDD=4.0V) and nominal operating conditions.

		Min	**Nominal**	**Max**
Analogue Supply	VCC	50 mA	75 mA	100 mA
Analogue Ground	GNDA	-50 mA	-75 mA	-100 mA
Digital Supply*	VDD	32 mA	36 mA	41 mA
Digital Ground	DGND	-32 mA	-36 mA	-41 mA
Discriminator threshold**	VTHP	0.3 µA	0.5 µA	1.5 µA
Discriminator threshold**	VTHN	0.3 µA	0.5 µA	1.5 µA

***In the Master chip the current draw at VDD power supply will be approximately 20 mA higher compared to the values shown in the table.**

**** If threshold voltages applied from external pads and the TrimDACs are set to zero.**

Table 2.7: Current draws at power supply inputs: nominal and absolute min/max values which may occur in non-standard operating conditions, e.g. all bias DACs set at zero or to full range, clock not supplied to the chips.

		Absolute Min	Nominal	Absolute Max
Analogue Supply	VCC	2 mA	75 mA	110 mA
Digital Supply	VDD	10 mA (30 mA)*	36 mA (56 mA)*	43 mA[#] (63 mA)*[#]

[#]Maximum current expected for the VDD power supply of 4.2 V

***Current draws by the Master chip**

Table 2.8: Current draws by the fully loaded module: nominal and min/max values are specified for the normal operating conditions and nominal supply voltages, absolute min/max values may occur in non-standard operating conditions, e.g. all bias DACs set at zero or to full range, clock not supplied to the chips.

		Absolute Min	Min	Nominal	Max	Absolute Max
Analogue Supply	VCC	24 mA*	600 mA	900 mA	1200 mA	1320 mA
Digital Supply	VDD	140 mA*	360 mA	400 mA	450 mA	470 mA[#]
Total power		0.58 W*	3.54 W	4.75 W	6.0 W	7.0 W

*** For the absolute minimum values it is assumed that all 12 chips on the module are connected to the power lines and none of them is damaged. The power consumption is calculated for the minimum supply voltages: VCC = 3.3V and VDD = 3.8V**

[#]Maximum current expected for the VDD power supply of 4.2 V.

2.2.6 BOND PAD ARRANGEMENT

Table 2.9: Bond Pad Position with respect to the origin at the lower left corner (detgnd pad).

Pad Name	Pad Centre (x,y)	Pad Size (x x y)	Pad Name	Pad Centre (x,y)	Pad Size (x x y)
INPUT PADS					
detgnd	(65,6266)	120x43	in<127>	(266,6218)	120x43
in<126>	(65,6170)	120x43	in<125>	(266,6122)	120x43
in<124>	(65,6074)	120x43	in<123>	(266,6026)	120x43
in<122>	(65,5978)	120x43	in<121>	(266,5930)	120x43
in<120>	(65,5882)	120x43	in<119>	(266,5834)	120x43
in<118>	(65,5786)	120x43	in<117>	(266,5738)	120x43
in<116>	(65,5690)	120x43	in<115>	(266,5642)	120x43
in<114>	(65,5594)	120x43	in<113>	(266,5546)	120x43
in<112>	(65,5498)	120x43	in<111>	(266,5450)	120x43
in<110>	(65,5402)	120x43	in<109>	(266,5354)	120x43
in<108>	(65,5306)	120x43	in<107>	(266,5258)	120x43
in<106>	(65,5210)	120x43	in<105>	(266,5162)	120x43
in<104>	(65,5114)	120x43	in<103>	(266,5066)	120x43
in<102>	(65,5018)	120x43	in<101>	(266,4970)	120x43

in<100>	(65,4922)	120x43	in<99>	(266,4874)	120x43
in<98>	(65,4826)	120x43	in<97>	(266,4778)	120x43
in<96>	(65,4730)	120x43	in<95>	(266,4682)	120x43
in<94>	(65,4634)	120x43	in<93>	(266,4586)	120x43
in<92>	(65,4538)	120x43	in<91>	(266,4490)	120x43
in<90>	(65,4442)	120x43	in<89>	(266,4394)	120x43
in<88>	(65,4346)	120x43	in<87>	(266,4298)	120x43
in<86>	(65,4250)	120x43	in<85>	(266,4202)	120x43
in<84>	(65,4154)	120x43	in<83>	(266,4106)	120x43
in<82>	(65,4058)	120x43	in<81>	(266,4010)	120x43
in<80>	(65,3962)	120x43	in<79>	(266,3914)	120x43
in<78>	(65,3866)	120x43	in<77>	(266,3818)	120x43
in<76>	(65,3770)	120x43	in<75>	(266,3722)	120x43
in<74>	(65,3674)	120x43	in<73>	(266,3626)	120x43
in<72>	(65,3578)	120x43	in<71>	(266,3530)	120x43
in<70>	(65,3482)	120x43	in<69>	(266,3434)	120x43
in<68>	(65,3386)	120x43	in<67>	(266,3338)	120x43
in<96>	(65,3290)	120x43	in<65>	(266,3242)	120x43
in<64>	(65,3194)	120x43	in<63>	(266,3146)	120x43
in<62>	(65,3098)	120x43	in<61>	(266,3050)	120x43
in<60>	(65,3002)	120x43	in<59>	(266,2954)	120x43
in<58>	(65,2986)	120x43	in<57>	(266,2858)	120x43
in<56>	(65,2810)	120x43	in<55>	(266,2762)	120x43
in<54>	(65,2714)	120x43	in<53>	(266,2666)	120x43
in<52>	(65,2618)	120x43	in<51>	(266,2570)	120x43
in<50>	(65,2522)	120x43	in<49>	(266,2474)	120x43
in<48>	(65,2426)	120x43	in<47>	(266,2378)	120x43
in<46>	(65,2330)	120x43	in<45>	(266,2282)	120x43
in<44>	(65,2234)	120x43	in<43>	(266,2186)	120x43
in<42>	(65,2138)	120x43	in<41>	(266,2090)	120x43
in<40>	(65,2042)	120x43	in<39>	(266,1994)	120x43
in<38>	(65,1946)	120x43	in<37>	(266,1898)	120x43
in<36>	(65,1850)	120x43	in<35>	(266,1802)	120x43
in<34>	(65,1754)	120x43	in<33>	(266,1706)	120x43
in<32>	(65,1658)	120x43	in<31>	(266,1610)	120x43
in<30>	(65,1562)	120x43	in<29>	(266,1514)	120x43
in<28>	(65,1466)	120x43	in<27>	(266,1418)	120x43
in<26>	(65,1370)	120x43	in<25>	(266,1322)	120x43

in<24>	(65,1274)	120x43	in<23>	(266,1226)	120x43
in<22>	(65,1178)	120x43	in<21>	(266,1130)	120x43
in<20>	(65,1082)	120x43	in<19>	(266,1034)	120x43
in<18>	(65,986)	120x43	in<17>	(266,938)	120x43
in<16>	(65,890)	120x43	in<15>	(266,842)	120x43
in<14>	(65,794)	120x43	in<13>	(266,746)	120x43
in<12>	(65,698)	120x43	in<11>	(266,650)	120x43
in<10>	(65,602)	120x43	in<9>	(266,554)	120x43
in<8>	(65,506)	120x43	in<7>	(266,458)	120x43
in<6>	(65,410)	120x43	in<5>	(266,362)	120x43
in<4>	(65,314)	120x43	in<3>	(266,266)	120x43
in<2>	(65,218)	120x43	in<1>	(266,170)	120x43
in<0>	(65,122)	120x43	detgnd	(266,74)	120x43
detgnd	(65,26)	120x43			
FRONT-END SERVICE PADS					
detgnd	(596,74)	200x140	detgnd	(596,6221)	200x140
GNDA	(896,74)	200x140	GNDA	(896,6221)	200x140
VCC	(1196,74)	200x140	VCC	(1196,6221)	200x140
VTHN	(1446,74)	100x140	VTHN	(1446,6221)	100x140
VTHP	(1646,74)	100x140	VTHP	(1646,6221)	100x140
ring_a	(1846,74)	100x140	ring_a	(1846,6221)	100x140
D_ISH	(2046,74)	100x140	cal0	(2046,6221)	100x140
IP_PROBE	(2246,74)	100x140	cal1	(2246,6221)	100x140
IS_PROBE	(2446,74)	100x140	cal2	(2446,6221)	100x140
			cal3	(2646,6221)	100x140
BYPASS PADS					
			tokenoutBPB	(5211,6211)	100x160
			tokenoutBP	(5543,6211)	100x160
			datainBPB	(5875,6211)	100x160
			datainBP	(6207,6211)	100x160
tokeninBPB	(6522,84)	100x160	**Spare digital bias pads**		
tokeninBP	(6854,84)	100x160	DGND	(6540,6211)	100x160
dataoutBPB	(7186,84)	100x160	VDD	(6872,6211)	100x160
dataoutBP	(7518,84)	100x160			
OUTPUT PADS					
VDD	(8069,6187)	160x180			
DGND	(8069,5914)	160x180			

tokenoutB	(8069,5688)	160x100			
tokenout	(8069,5508)	160x100			
datainB	(8069,5328)	160x100			
datain	(8069,5148)	160x100			
clk0B	(8069,4968)	160x100			
clk0	(8069,4788)	160x100			
clk1B	(8069,4608)	160x100			
clk1	(8069,4428)	160x100			
ID<4>	(8069,4238)	160x140			
ID<3>	(8069,4038)	160x140			
ID<2>	(8069,3838)	160x140			
ID<1>	(8069,3638)	160x140			
ID<0>	(8069,3438)	160x140			
masterB	(8069,3238)	160x140			
com1B	(8069,3048)	160x100			
com1	(8069,2868)	160x100			
com0B	(8069,2688)	160x100			
com0	(8069,2508)	160x100			
select	(8069,2318)	160x140			
resetB	(8069,2118)	160x140			
datalinkB	(8069,1928)	160x100			
datalink	(8069,1748)	160x100			
dataout	(8069,1568)	160x100			
dataoutB	(8069,1388)	160x100			
tokenin	(8069,1208)	160x100			
tokeninB	(8069,1028)	160x100			
DGNG	(8069,848)	160x100			
DGND	(8069,621)	160x180			
VDD	(8069,395)	160x100			
VDD	(8069,169)	160x180			

2.2.7 PHYSICAL REQUIREMENTS

The die size of the ABCD3T chip is 6550 µm x 8400 µm.

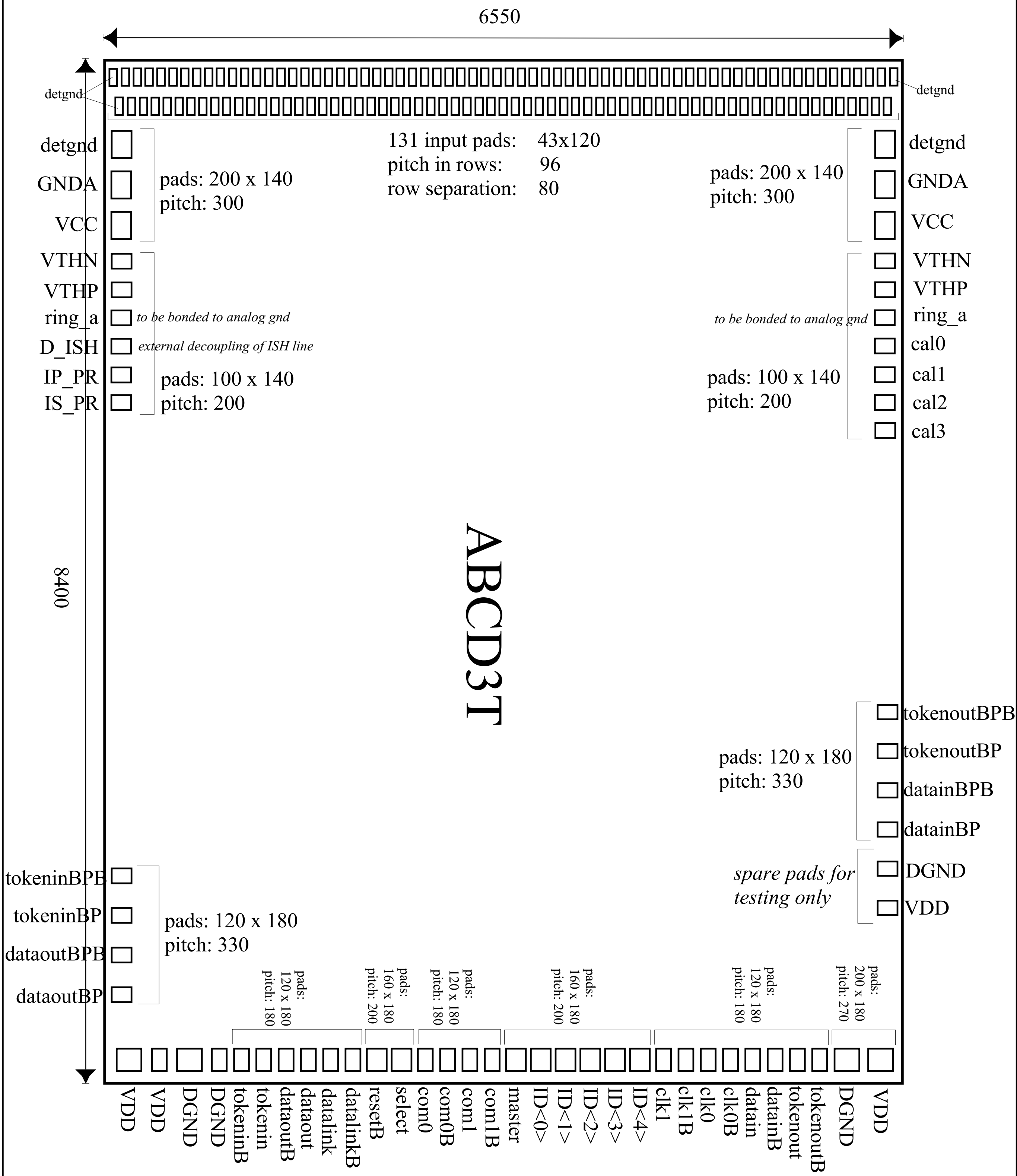

Figure 2.7: Pad Layout of the ABCD3T IC.

3 QUALIFICATION TESTING

The ABCD3T ICs are received from the foundry on untested wafers. Therefore all the chips needs to be fully tested and parameterised before dicing the wafers in order to select the chips which fulfil the SCT requirements with respect to:

- **correct functionality**
- **analogue performance**
- **speed performance of digital circuitry.**

The acceptance limits for various parameters are defined with sufficient margins allowing for degradation of parameters after full irradiation in the SCT environment

All chips are put through the full test procedure, even if they fail at some intermediate tests. The test data are then used for failure mode analayasis.

3.1 TEST FLOW

The test flow at wafer screening is shown in Figure 3.1. The test starts with the configuration register test. All the chips passing this basic digital test for the nominal condition of power supply and speed are examined and the results are saved for off-line analysis and tagging.

The following tables define the test conditions for each test.

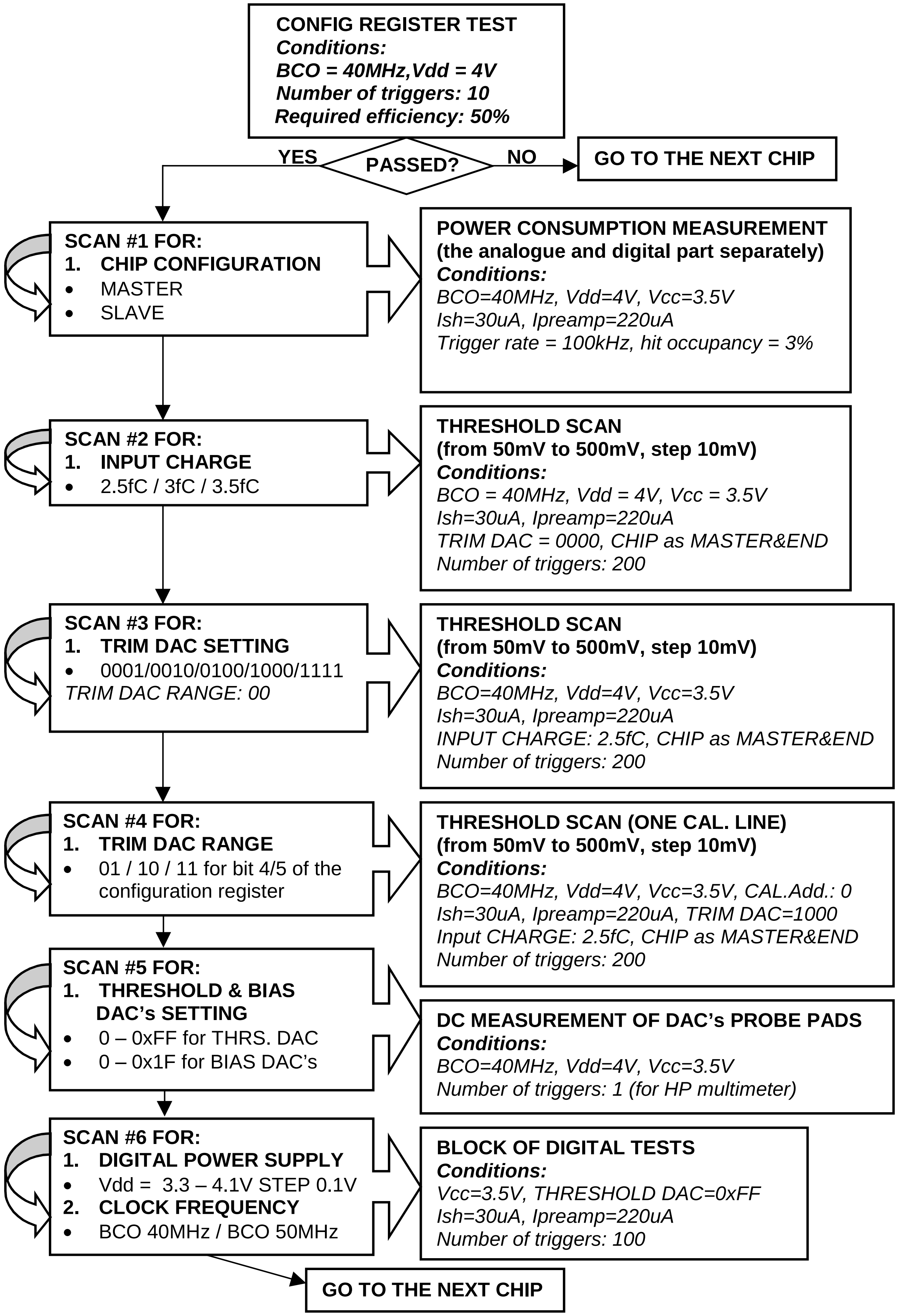

Figure 3.1: Test flow at screening of ABCD3T wafers.

3.1.1 POWER CONSUMPTION MEASUREMENT

The power consumption of both digital and analogue parts of the chip is measured. To simulate the nominal working conditions for the ATLAS SCT occupancy and L1 trigger rate, the measurement is done applying a 100kHz trigger with an occupancy of 3% (hits in 4 channels).

Table 3.1: Power consumption measurement.

<table>
<tr><td rowspan="10">SETTINGS</td><td>CHIP configuration</td><td colspan="2">END | EDGE_ON | DATA_COMPRESSION_01X | DATA_TAKING_MODE | SELECT_0</td></tr>
<tr><td rowspan="6">CHIP bias</td><td>Ipreamp</td><td>220 μA</td></tr>
<tr><td>Ishaper</td><td>30 μA</td></tr>
<tr><td>Vcc</td><td>3.5 V</td></tr>
<tr><td>Vdd</td><td>4 V</td></tr>
<tr><td>BCO</td><td>40 MHz</td></tr>
<tr><td>Threshold DAC</td><td>0xFF</td></tr>
<tr><td rowspan="2">TRIM DAC</td><td>Value</td><td>0000</td></tr>
<tr><td>Range</td><td>00</td></tr>
<tr><td>CHIP address</td><td colspan="2">Programmed = 1</td></tr>
<tr><td></td><td>COMMAND</td><td colspan="2">Issue Calibration Pulse + 131 BCO delay + L1 trigger</td></tr>
<tr><td rowspan="2">SCANS</td><td colspan="2">LOOPS</td><td>1. Chip configuration = {MASTER, SLAVE}</td></tr>
<tr><td colspan="2">Trigger rate</td><td>100 kHz</td></tr>
</table>

3.1.2 ANALOGUE TESTS

3.1.2.1 MEASUREMENT OF GAIN, OFFSET AND NOISE

The goal of the test is to determine the basic analogue parameters of the front-end: gain, noise and discriminator offset for each electronic channel. For this purpose threshold scans for three values of input charge are performed for each channel.

Table 3.2: Gain, noise and offset measurement.

<table>
<tr><td rowspan="10">SETTINGS</td><td>CHIP configuration</td><td colspan="2">MASTER | END | EDGE_ON | DATA_COMPRESSION_01X | DATA_TAKING_MODE | SELECT_0</td></tr>
<tr><td rowspan="5">CHIP bias</td><td>Ipreamp</td><td>220 µA</td></tr>
<tr><td>Ishaper</td><td>30 µA</td></tr>
<tr><td>Vcc</td><td>3.5 V</td></tr>
<tr><td>Vdd</td><td>4 V</td></tr>
<tr><td>BCO</td><td>40 MHz</td></tr>
<tr><td rowspan="2">TRIM DAC</td><td>Value</td><td>0000</td></tr>
<tr><td>Range</td><td>00</td></tr>
<tr><td>CHIP address</td><td colspan="2">Programmed = 1</td></tr>
<tr><td>COMMAND</td><td colspan="2">Issue Calibration Pulse + 131 BCO delay + L1 trigger</td></tr>
<tr><td rowspan="2">SCANS</td><td>LOOPS</td><td colspan="2">INPUT CHARGE = {2.5fC, 3fC, 3.5fC}
CALIBRATION ADDRESS = {0,1,2,3}
THRESHOLD = [50mV – 500mV] step 10mV</td></tr>
<tr><td>No. of triggers</td><td colspan="2">200</td></tr>
</table>

3.1.2.2 CHARACTERIZATION OF THE TRIMDAC.

The TrimDAC response curve is measured for each channel for the basic range (00).

Table 3.3: : Characterisation of the TrimDAC.

<table>
<tr><td rowspan="10">SETTINGS</td><td>CHIP configuration</td><td colspan="2">MASTER | END | EDGE_ON | DATA_COMPRESSION_01X | DATA_TAKING_MODE | SELECT_0</td></tr>
<tr><td rowspan="5">CHIP bias</td><td>Ipreamp</td><td>220 µA</td></tr>
<tr><td>Ishaper</td><td>30 µA</td></tr>
<tr><td>Vcc</td><td>3.5 V</td></tr>
<tr><td>Vdd</td><td>4 V</td></tr>
<tr><td>BCO</td><td>40 MHz</td></tr>
<tr><td>Input Charge</td><td colspan="2">2.5 fC</td></tr>
<tr><td>TRIM DAC</td><td>Range</td><td>00</td></tr>
<tr><td>CHIP address</td><td colspan="2">Programmed = 1</td></tr>
<tr><td>COMMAND</td><td colspan="2">Issue Calibration Pulse + 131 BCO delay + L1 trigger</td></tr>
<tr><td rowspan="2">SCANS</td><td>LOOPS</td><td colspan="2">1. TRIM DAC VALUE = {0001, 0010, 0100, 1000, 1111}
2. CALIBRATION ADDRESS = {0,1,2,3}
3. THRESHOLD = [50mV – 500mV] step 10mV</td></tr>
<tr><td>No. of triggers</td><td colspan="2">200</td></tr>
</table>

3.1.2.3 CHARACTERIZATION OF THE TRIMDAC RANGE

The scan for the TRIM DAC RANGE setting is performed for one TRIM DAC value (1000). The TRIM DAC RANGE is calculated as an average of the values obtained from 32 scanned channels.

Table 3.4: Characterisation of TRIM DAC range.

SETTINGS	CHIP configuration	MASTER | END | EDGE_ON | DATA_COMPRESSION_01X | DATA_TAKING_MODE | SELECT_0	
	CHIP bias	Ipreamp	220 μA
		Ishaper	30 μA
		Vcc	3.5 V
		Vdd	4 V
		BCO	40 MHz
	CALIBRATION address	0	
	Input Charge	2.5 fC	
	TRIM DAC	Value	1000
	CHIP address	Programmed = 1	
	COMMAND	Issue Calibration Pulse + 131 BCO delay + L1 trigger	
SCANS	LOOPS	1. TRIM DAC RANGE = {01, 10, 11} 2. THRESHOLD = [50mV – 500mV] step 10mV	
	No. of triggers	200	

3.1.2.4 MEASUREMENT OF THE CHARACTERISTICS OF THE DIGITAL-TO-ANALOGUE CONVERTERS

Full response curves are measured for three DACs which provide common voltage/current for all channels in the chip:

- **Threshold DAC (8 bits)**
- **Input transistor current DAC (Ipreamp - 5 bit)**
- **Shaper current DAC (Ishaper – 5 bit).**

3.1.3 DIGITAL TESTS

Digital tests are designed to verify all digital circuitry in the ABCD3T chips and in particular to test the important functions: chip control, chip-to-chip communication and data compression. In order to determine the speed margins the digital tests are performed for different values of clock frequency and power supply.

3.1.4 TEST #1, CONFIGURATION REGISTER INPUT/OUTPUT TEST

The configuration register is written with random values, keeping the chip always as MASTER and END. The values are then compared with the data returned by the chip in the send identification mode.

Table 3.5: Configuration register input/output test.

SETTINGS	CHIP configuration	MASTER | END | SEND_ID_MODE | SELECT_0	
	CHIP bias	Ipreamp	220 µA
		Ishaper	30 µA
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
	CHIP address	Universal address in command	
	COMMAND	L1 trigger	
SCANS	LOOPS	Random setting of the remaining configuration register bits	
	No. of triggers	100	

3.1.5 TEST #2, ADDRESSING TEST

The chip is given a random address and is configured using that address. The value is compared with the one returned in the chip data.

Table 3.6: Addressing test.

SETTINGS	CHIP configuration	MASTER | END | EDGE_ON | DATA_COMPRESSION_01X | SEND_ID_MODE | SELECT_0	
	CHIP bias	Ipreamp	220 µA
		Ishaper	30 µA
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
	CHIP address	Random	
	COMMAND	L1 trigger	
SCANS	LOOPS	1. Random setting of address bits	
	No. of triggers	100	

3.1.6 TEST #3, INPUT REGISTER TEST

Four different patterns are loaded in the mask register and the input register is pulsed. Pulsing the input register issues one clock pulse to the channels allowed by the mask register. The data patterns read out from the chip are compared with the ones which are expected.

Table 3.7: Input register test.

SETTINGS	CHIP configuration	MASTER | END | EDGE_ON | DATA_COMPRESSION_01X | DATA_TAKING_MODE | SELECT_0	
	CHIP bias	Ipreamp	220µA
		Ishaper	30µA
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
	CHIP address	Programmed = 1	
	COMMAND	Pulse Input Register + 129 BCO delay + L1 trigger	
SCANS	LOOPS	1. MASK = {mask#1, mask#2,mask#3,mask#4}	
	No. of triggers	100	

3.1.7 TEST #4, INPUT LINES TEST

The functionality of both input lines for the chip (basic 0 and redundant 1) is tested by injecting the four patterns through the mask register and sending the clocks and commands through both lines. The delay between SoftReset and L1 trigger is scanned in order to examine each row of the pipeline. The data output is compared with the injected patterns.

Table 3.8: Input lines test

SETTINGS	CHIP configuration	MASTER | END | EDGE_OFF | DATA_COMPRESSION_X1X | MASK | DATA_TAKING_MODE | SELECT_0	
	CHIP bias	Ipreamp	220µA
		Ishaper	30µA
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
	CHIP address	Programmed = 1	
	COMMAND	SoftReset + Delay + L1 trigger	
SCANS	LOOPS	1. SELECT LINE = {0,1} MASK = {mask#1, mask#2,mask#3,mask#4} Delay = [150BCO - 161BCO] step 1BCO	
	No. of triggers	10	

3.1.8 TEST #5, FAKE SLAVE TEST

The chip is set as a master and middle chip. The token transmission for both lines (0 and 1) is checked.

Table 3.9: Fake slave test.

SETTINGS	CHIP configuration	MASTER | MIDDLE | EDGE_ON | DATA_COMPRESSION_01X | DATA_TAKING_MODE | SELECT_0	
	CHIP bias	Ipreamp	220µA
		Ishaper	30µA
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
	CHIP address	Programmed = 1	
	COMMAND	Pulse Input Register + 129 BCO delay + L1 trigger + 5BCO delay + appended data pattern	
SCANS	LOOPS	1. {DATA_IN_0 & TOKEN_OUT_0, DATA_IN_1 & TOKEN_OUT_1}	
	No. of triggers	100	

3.1.9 TEST #6, SLAVE TEST

The chip is set as slave and end chip. The four patterns are injected through the mask register and the 8 tokens are sent after each 8 triggers through both input lines.

Table 3.10: Slave test.

SETTINGS	CHIP configuration	SLAVE | END | EDGE_OFF | DATA_COMPRESSION_X1X | MASK | DATA_TAKING_MODE | SELECT_0	
	CHIP bias	Ipreamp	220µA
		Ishaper	30µA
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
	CHIP address	Programmed = 1	
	COMMAND	8xL1 trigger + 8xTOKEN	
SCANS	LOOPS	1. {TOKEN_IN_0 & DATA_OUT_0, TOKEN_IN_1 & DATA_OUT_1} 2. MASK = {mask#1, mask#2,mask#3,mask#4}	
	No. of triggers	10	

3.2 FAILURE ANALYSIS

In addition to the qualification of chips for the modules the wafers screening data are used for failure mode analysis. The results of failure analysis will be compared against the foundry data on Process Controll Monitor and will serve for monitoring of yield during production.

All tested chips are classified in such a way that each chip is assigned to a unique bin. The bin definitions are shown in Table 3.11. The algorithm used for assigning the chips to given bins is shown schematically in Figure 3.2.

Table 3.11: Definition of bins

BIN	DEFINITION
0	Good chip (after all tests)
2	failed DIGITAL TEST#1 @ 3.8V & 50MHz
3	failed DIGITAL TEST#2 (ADDRESSING) @ 3.8V & 50MHz
4	failed DIGITAL TEST#2 (L1 counter) @ 3.8V & 50MHz
5	failed DIGITAL TEST#4 (reading the mask) @ 3.8V & 50MHz
6	failed DIGITAL TEST#5 @ 3.8V & 50MHz
7	failed DIGITAL TEST#6 @ 3.8V & 50MHz
8	failed DIGITAL TEST#4 (reading the token) @ 3.8V & 50MHz
9	defect(s) in analog part #2 (channel offset out of the Trim DAC range 1 **or** gain different from the avarage by more than 25% **or** channel noise is 3 times higher than average noise of the chip **or** difference between average gain of the chip and average gain from the wafer is higher than 30%)
10	defect(s) in analog part #1 (no response to the calibration pulses)
11	[1 - 10] defects in the pipeline (low analog efficiency)
12	[10-100] defects in the pipeline (low analog efficiency)
13	> 100 defects in the pipeline (low analog efficiency)
14	high power consumption in digital part (Slave mode) (> 30% average)
15	high power consumption in analog part (Slave mode) (> 30% average)
16	low power consumption in digital part (Slave mode) (<30% average)
17	low power consumption in analog part (Slave mode) (<30% average)
18	Non-linear Threshold DAC (MAX ERR>10%)
19	Non-linear Bias1 (Preamp) DAC (MAX ERR>25%)
20	Non-linear Bias2 (Shaper) DAC (MAX ERR>25%)
21	Defect in the TRIM DAC (MAX ERR>25% **or** discrepancy between Trim DAC range 0 for a given channel and **TrDACRange0** is higher than 40%)
22	Defect in Trim DAC ranges (discrepancies between **TrDACRange0 ÷ TrDACRange3** and averages from the wafer are higher than 40%)
23	Chip noise is outside of wafer noise distribution
24	Strict digital test failed at Vdd = 3.8 and 40MHz
25	Strict digital test failed at Vdd = 3.8 and 50MHz

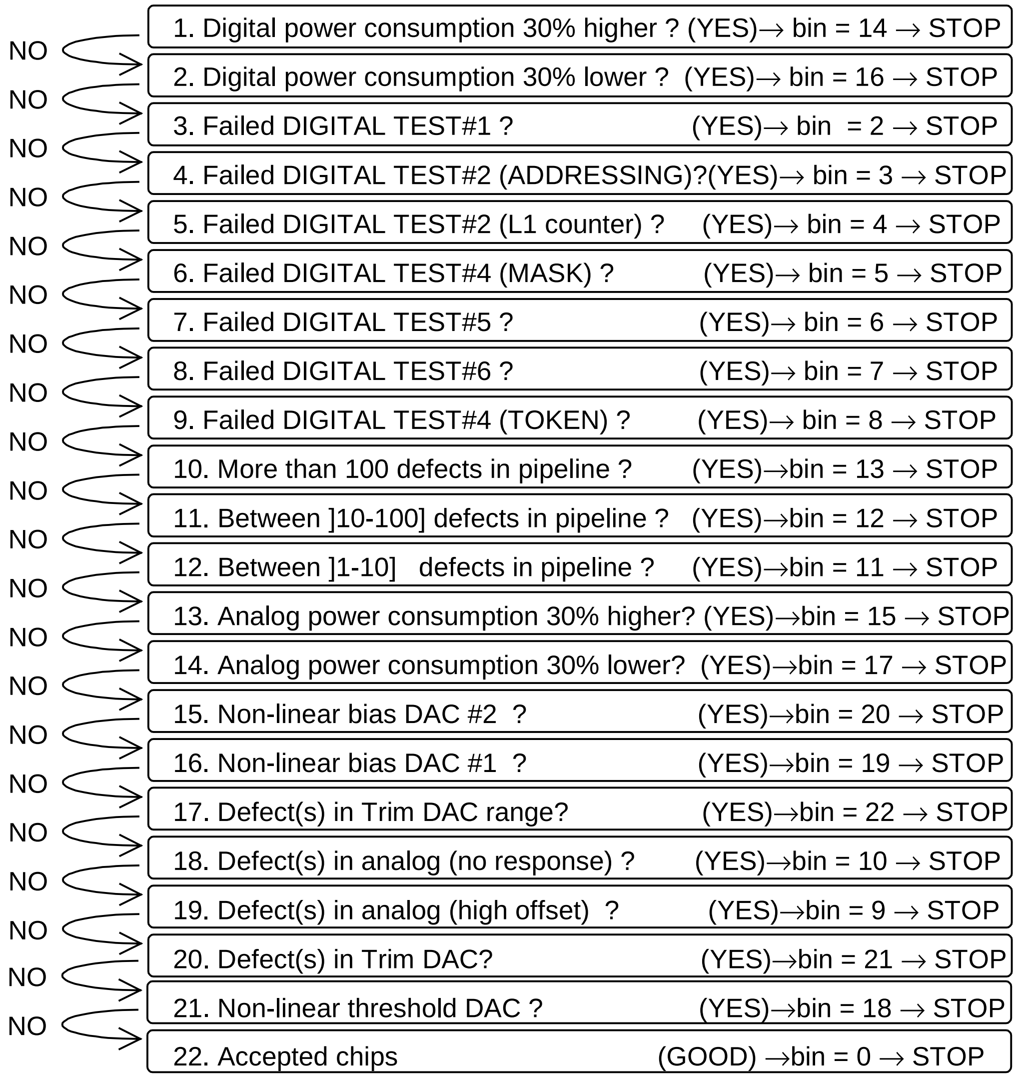

Figure 3.2: Algorithm for binning the test results.

4 INTERFACE TO THE SCT PRODUCTION DATABASE

4.1 PARAMETERS TRANSFERRED TO SCT DATABASE

Test parameters of all tested chips will be transferred to the ATLAS SCT production database. The parameters extracted from the wafer screening data and transferred to the database are listed in the following tables. All fields are mandatory.

Table 4.1: List of parameters transferred to the SCT database for the ITEM/ABCD article.

ITEM/CHIP unit	
MFR_SER_NO	BATCH-WAFER-XPOS-YPOS (example Z34685-W01-X05-Y05) – manufacturer serial number consist of number of batch, wafer number and x,y position of chip on the wafer
RECEIPT_DATE	Date of reception of material (wafers)
LOCATION	Location of the material (for example CERN)

Table 4.2: List of parameters transferred to the SCT database for the TEST_ABCD article.

TEST_ABCD unit	
MachineName	Name of the machine used for wafer screening
OnlineSoftRev	On-line software revision
OfflineSoftRev	Off-line software revision
PreampBias	Value of bias for the preamplifier stage used in the test [μA]
ShaperBias	Value of bias for the shaper stage used in the test [μA]
PrfFlg	Perfect flag – for absolutely perfect chips (depends on software revision)
DigFlg	Digital flag - for digitally perfect chips equal to 1
DppFlg	Digital Perfect Pattern flag (internal use)
Vdd0	Minimum Vdd [V] for which the chip is fully efficient for all digital tests @ 50MHz
Vdd0strict	Minimum Vdd [V] for which the chip is fully efficient for all **STRICT** digital tests @ 50MHz
VddTest1F0 (VddCnf0)	Minimum Vdd [V] for digital TEST vector #1 @ 50MHz
VddTest2F0 (VddAddr0)	Minimum Vdd [V] for digital TEST vector #2 @ 50MHz
VddTest3F0 (VddL1C0)	Minimum Vdd [V] for digital TEST vector #3 @ 50MHz
VddTest4F0 (VddInpReg0)	Minimum Vdd [V] for digital TEST vector #4 @ 50MHz
VddTest5F0 (VddInpLin0)	Minimum Vdd [V] for digital TEST vector #5 @ 50MHz
VddTest6F0 (VddFakeS0)	Minimum Vdd [V] for digital TEST vector #6 (
VddTest7F0 (VddSlave0)	Minimum Vdd [V] for digital TEST vector #7
VddTest8F0 (VddToken0)	Minimum Vdd [V] for digital TEST vector #8
Vdd1	Minimum Vdd[V] for which the chip is fully efficient for all digital tests @ 40MHz
Vdd1strict	Minimum Vdd[V] for which the chip is fully efficient for all **STRICT** digital tests @ 40MHz
VddTest1F1 (VddCnf1)	Same test as VddTest1F0 @ 40MHz
VddTest2F1 (VddAddr1)	Same test as VddTest2F0 @ 40MHz
VddTest3F1 (VddL1C1)	Same test as VddTest3F0 @ 40MHz
VddTest4F1 (VddInpReg1)	Same test as VddTest4F0 @ 40MHz
VddTest5F1 (VddInpLin1)	Same test as VddTest5F0 @ 40MHz
VddTest6F1 (VddFakeS1)	Same test as VddTest6F0 @ 40MHz
VddTest7F1 (VddSlave1)	Same test as VddTest7F0 @ 40MHz
VddTest8F1 (VddToken1)	Same test as VddTest8F0 @ 40MHz
ThrsDACSlope	Threshold DAC slope [mV/bit] obtained from linear fit to the measurement points.
ThrsDACErr	Maximum non-linearity error for Threshold DAC (maximum dispersion of the measurement point from the linear fit [mV])
PreampDACSlope	Preamplifier bias DAC slope [mV/bit] obtained from linear fit to the measurement points (direct values in mV readout from the probe pad)
PreamDACErr	Maximum non-linearity error for Preamplifier bias DAC (maximum dispersion of the measurement point from the linear fit [mV])
ShaperDACSlope	Shaper bias DAC slope [mV/bit] obtained from linear fit to the measurement points (direct values in mV readout from the probe pad)
ShaperDACErr	Maximum non-linearity error for Shaper bias DAC (maximum dispersion of the measurement point from the linear fit [mV])

MDigC	Power consumption (current) of the digital part in MASTER mode [A]
SDigC	Power consumption (current) of the digital part in SLAVE mode [A]
MAnaC	Power consumption (current) of the analogue part in MASTER mode [A]
SAnaC	Power consumption (current) of the analogue part in SLAVE mode [A]
NdNoResp	Number of channels not responding to calibration pulses (bin10)
NdPipeline	Number of channels with low analogue efficiency (pipeline defects)
NdNoise	Number of noisy channels (bin 9)
NdGain	Number of channels with degraded gain (bin9)
NdTrim	Number of channels with defects in TRIM DACs. Defects in the Trim DACs are verified for range 0 (data available for all channels of the chip). Conditions for verification are the same as for calculation of bin number 21.
NdHOffset0	Number of channels with offset out of the Trim DAC range 0
NdHOffset1	Number of channels with offset out of the Trim DAC range 1 (bin 9)
NdHOffset2	Number of channels with offset out of the Trim DAC range 2
NdHOffset3	Number of channels with offset out of the Trim DAC range 3
Ndead	Total number of unusable channels (channels with defects in analogue part).
Status	BIN status of the chip
StatusValid	Validation word for Status
AuxFlags	Auxiliary flags
AvGain	Average gain of the chip [mV/fC]
SGain	Sigma deviation of the channel gains on the chip [mV/fC]
MaxGain	Maximum channel gain in the chip [mV/fC]
MinGain	Minimum channel gain in the chip [mV/fC]
AvOffset	Average offset of the chip [mV]
SOffset	Sigma deviation of the channel offsets on the chip [mV]
MaxOffset	Maximum channel offset in the chip [mV]
MinOffset	Minimum channel offset in the chip [mV]
MaxTrDACErr	Maximum nonlinearity error for Trim DAC range 0 [mV]
MaxTrSlope	Maximum Trim DAC slope [mV/bit] of the Trim DAC characteristic (Range 0)
MinTrSlope	Minimum Trim DAC slope [mV/bit] of the Trim DAC characteristic (range 0)
TrDACRange0	Average of the ranges 0 of the trim DACs in the chip [mV]
TrDACRange1	Average of the ranges 1 of the trim DACs in the chip [mV]
TrDACRange2	Average of the ranges 2 of the trim DACs in the chip [mV]
TrDACRange3	Average of the ranges 3 of the trim DACs in the chip [mV]
AvNoise	Average output noise of the chip [mV] (extracted from point #1)
SNoise	Sigma deviation of the channel output noise on the chip [mV] (point #1)
MaxNoise	Maximum channel output noise in the chip [mV] (point #1)
MinNoise	Minimum channel output noise in the chip [mV] (point #1)
Qfactor	Quality factor defined as: gain/SQRT(soffset^2+sgain^2)
Bin	Result of bin analysis (number from 0 to 28)

Table 4.3: List of the parameters transferred to the SCT database for the TSTABCDCHANNELS entity.

TSTABCDCHANNELS unit	
Chann_number	Channel number – primary key for this table
Gain	Gain for a given channel [mV/fC]
Offset	Offset for a given channel [mV]
Noise	Output noise for a given channel [mV]
TrDACSlope	Slope of the Trim DAC characteristic (Range 0) in [mV/bit]
TrDACErr	Maximum non-linearity error for Trim DAC (maximum dispersion of the measurement point from the linear fit [mV]) for Range 0
ChStatus	BIN status of channel

4.2 LOADING THE WAFER SCREENING RESULTS TO THE SCT DATABASE.

Uploading the chips to the database is done via a java application provided by the manager of the database. The encoding scheme for ITEMS.mfr_ser_no will be kept as a function of wafer_ser_no, XChipcoordinate, Ychipcoordinate.

Since the primary key of ITEMS is based only on the ITEMS.ser_no and no more constraints will be added to the ITEMS table, the application will be responsible for informing the user that the chips have not already been inserted into the database. The application will do that by checking the unique state of the ITEMS.MFR_SER_NO attribute before inserting the item chip.

An optional function to populate the SHIPS and SHIP_ITEMS automatically during the chips registration will also be implemented in this new java application. A special report will be generated to allow the users to make a shipment of a set of selected chips. The criteria for selecting the chips will be defined in future.

The report will give the possibility to automatically populate the SHIPS and SHIP_ITEMS tables with the record set by the criteria.

The web application already allow the users who are the owner of the shipped items and shipments to delete or update ITEMS, SHIPS and SHIP_ITEMS records.

When all the ship_items have been inserted (using the java application or the Web interface or else), the user is able “to send” (from a database point of view) the items to the destination person and institute, by updating the “Send Confirmation Date” field of the current shipment using his web browser.