Temperature and Vcc Study on "Large Gain Spread" chips

Select 3 hybrids with "Large Gain Spread (LGS)" chips

- Mfr ID = 720, 736, 749

Vary environment temperature to change the hybrid/ ASIC temperature

- Hybrid temp ~ 0, 27, 37 C

Vary Vcc from 3.3V to 3.8V by a step of 0.1V

Hybrid temp ~27 C

	ID=720	ID=736	ID=749
3.3[V]	E05	S11	S11
3.4[V]	OK	OK	OK
3.5[V]	OK	OK	OK
3.6[V]	OK	OK	OK
3.7[V]	OK	OK	S11(HighGain)
3.8[V]	OK	OK	S11(HighGain)

Hybrid temp ~0 C

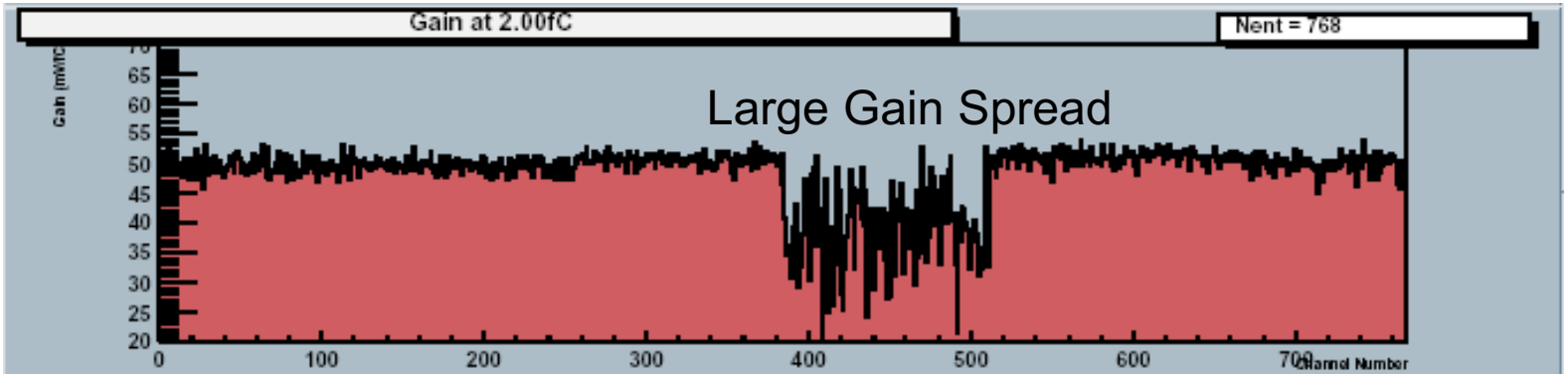
	ID=720	ID=736	ID=749
3.3[V]	E05	S01+S3+E5+M08 +S09+S10+S11	S11+others?
3.4[V]	E05	S10+S11	S11
3.5[V]	E05	S11	S11
3.6[V]	OK	OK	OK
3.7[V]	OK	OK	OK
3.8[V]	OK	OK	S11(HighGain)

Hybrid temp ~37 C

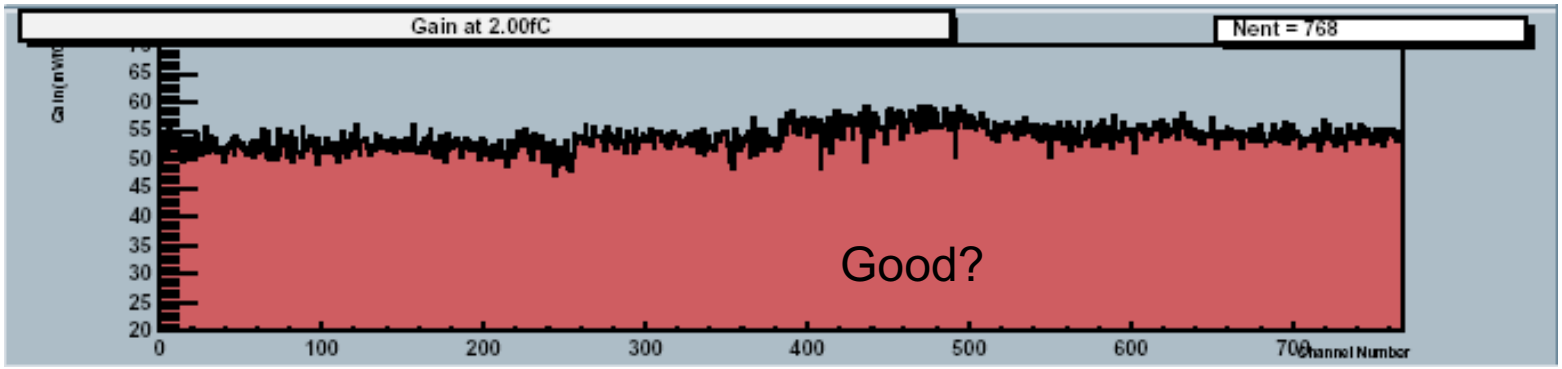
	ID=720	ID=736	ID=749
3.3[V]	E05	S11	S11
3.4[V]	OK	OK	OK
3.5[V]	OK	OK	OK
3.6[V]	OK	OK	OK
3.7[V]	OK	OK	S11(HighGain)
3.8[V]	OK	OK	S11(HighGain)

ID=749 Hybrid temp ~27 C

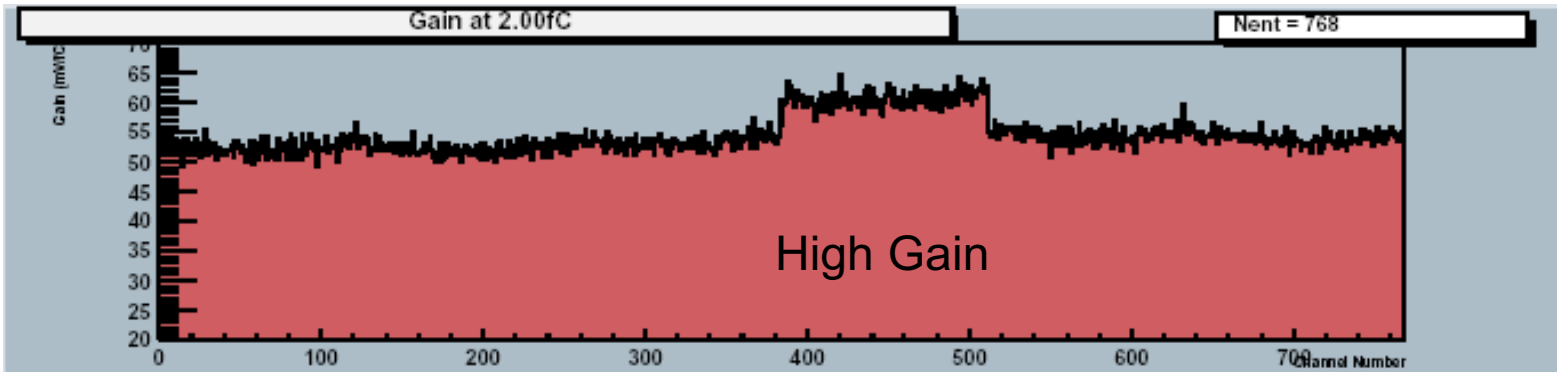
Vcc=3.3V



Vcc=3.5V
(Nominal)

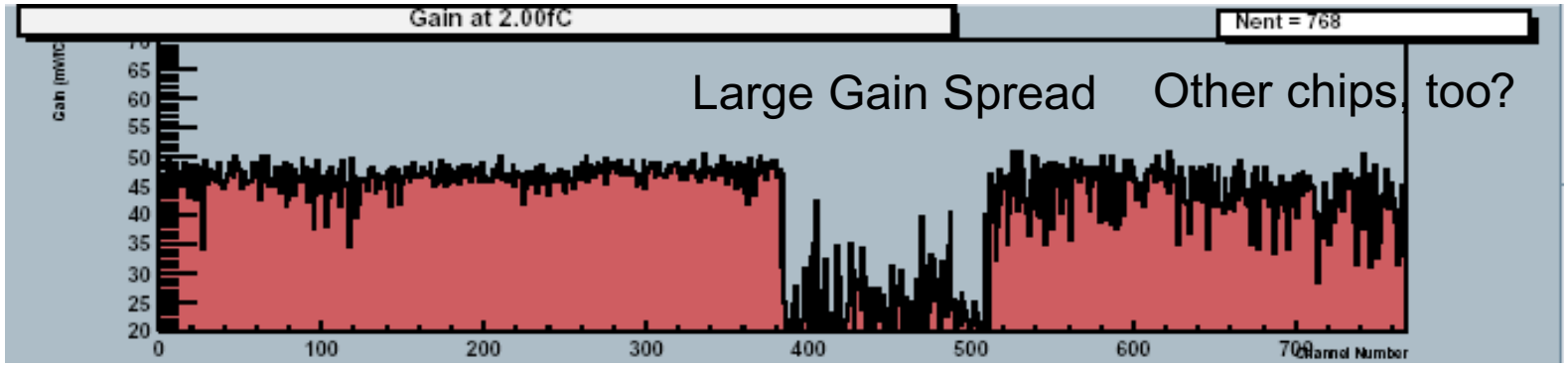


Vcc=3.8V

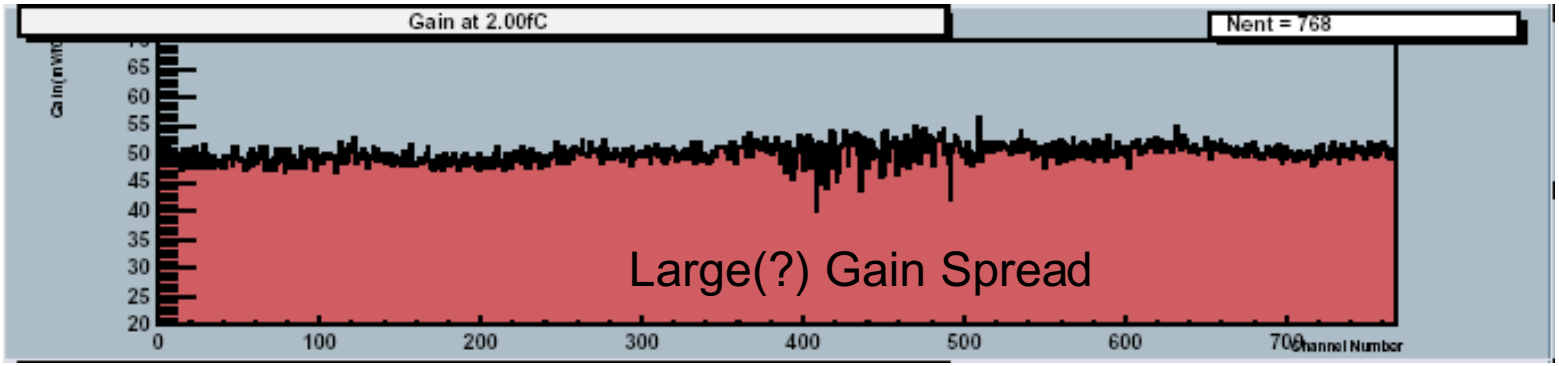


ID=749 Hybrid temp ~0 C

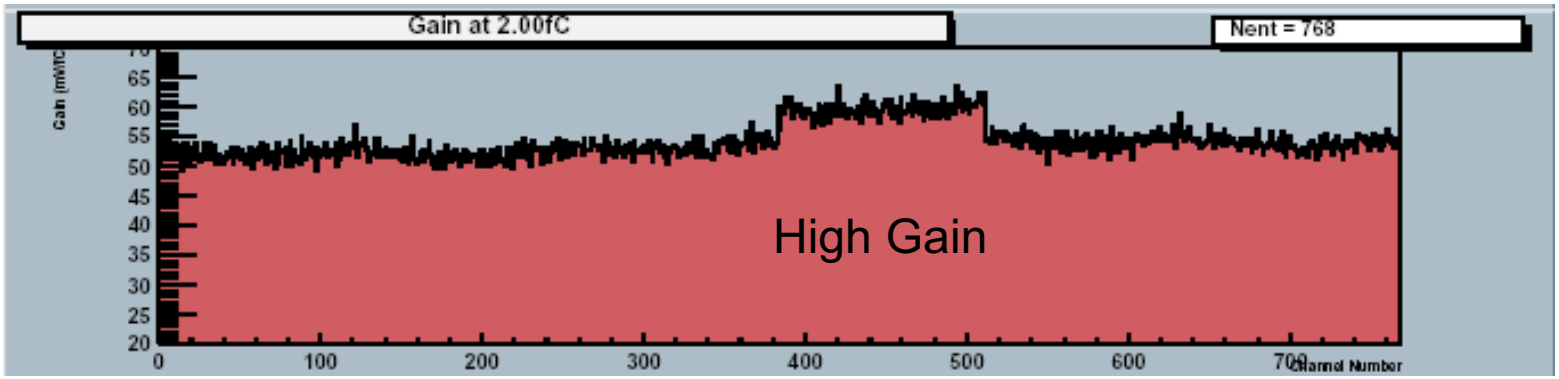
Vcc=3.3V



Vcc=3.5V
(Nominal)

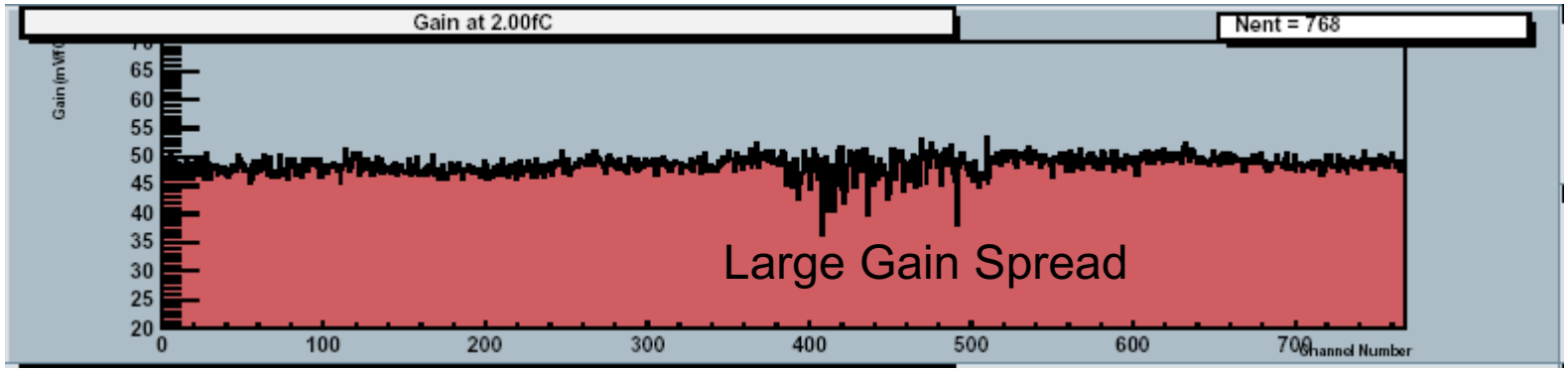


Vcc=3.8V

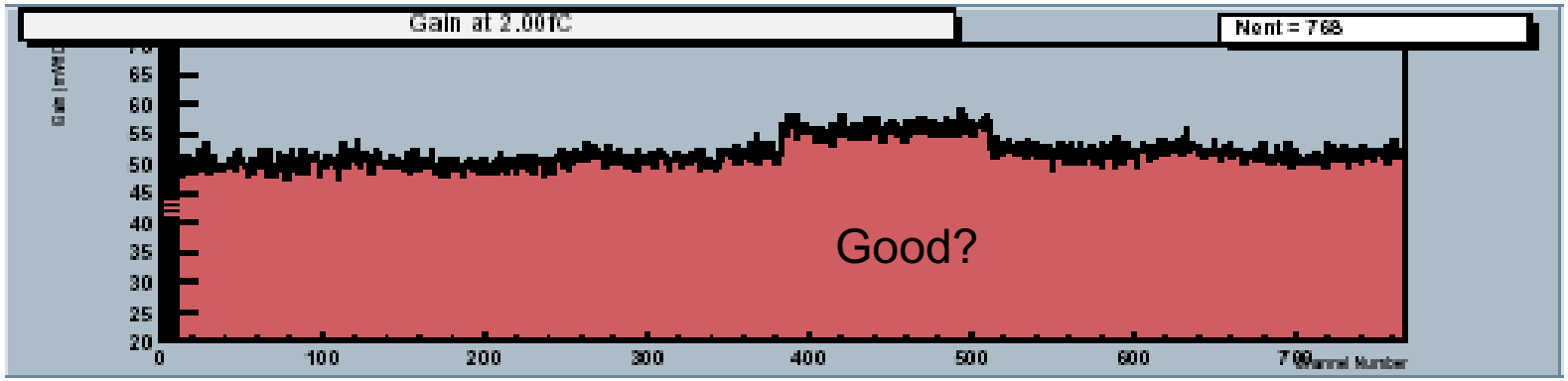


ID=749 Hybrid temp ~37 C

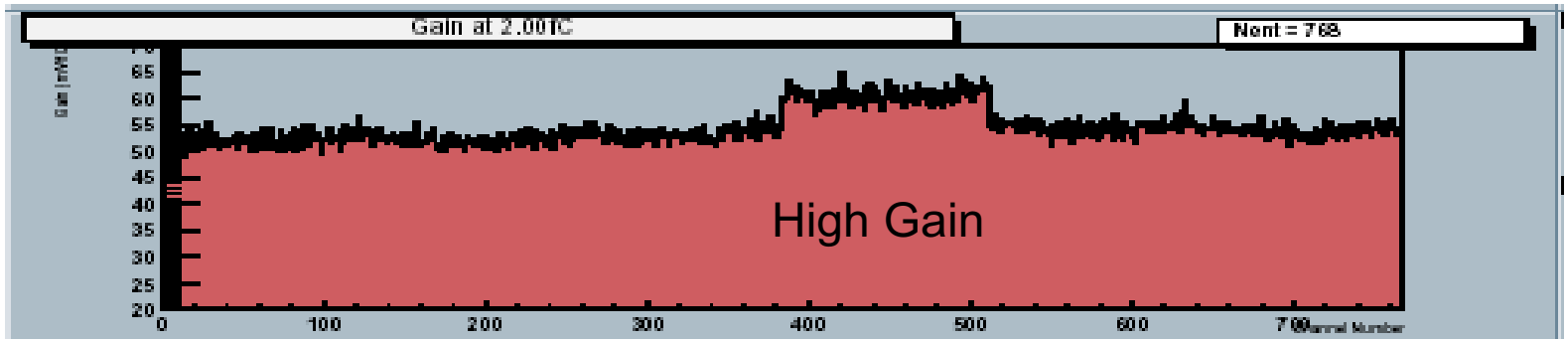
Vcc=3.3V



Vcc=3.5V
(Nominal)



Vcc=3.8V



Conclusions?

- ✓ The effect seems ASIC/chip intrinsic
- ✓ The LGS chips are more sensitive to the temperature and Vcc
- ✓ The problem is severer in lower temp.
- ✓ Wafer testing at Vcc = 3.3V may detect the problematic chips easily