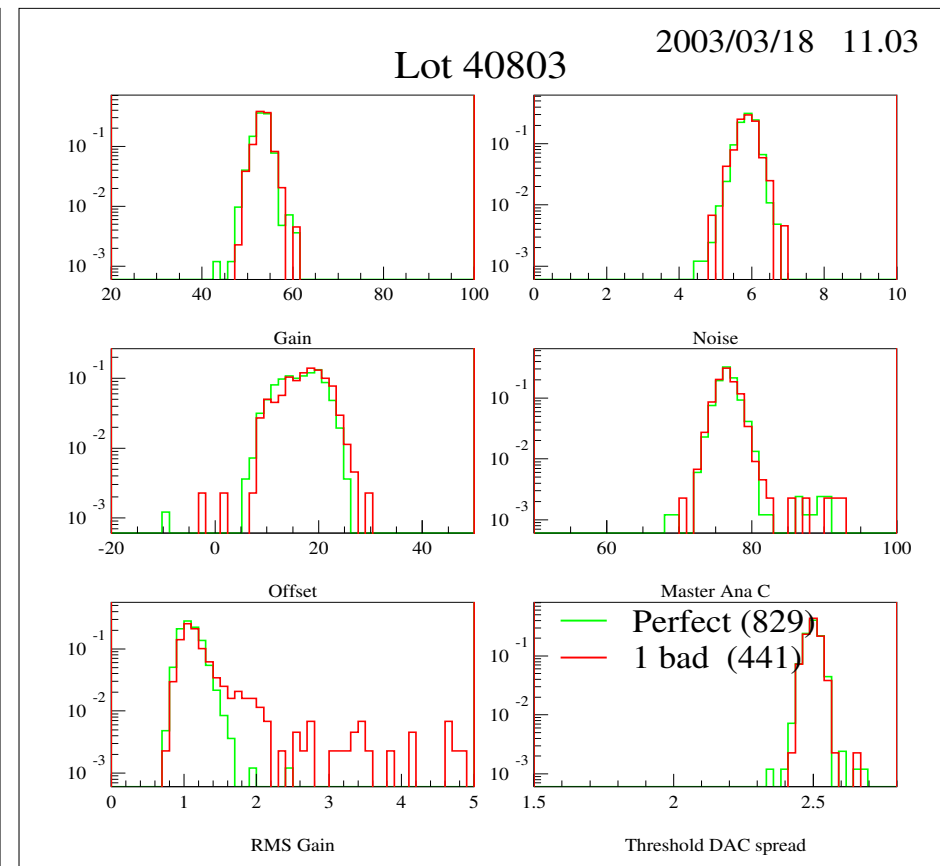
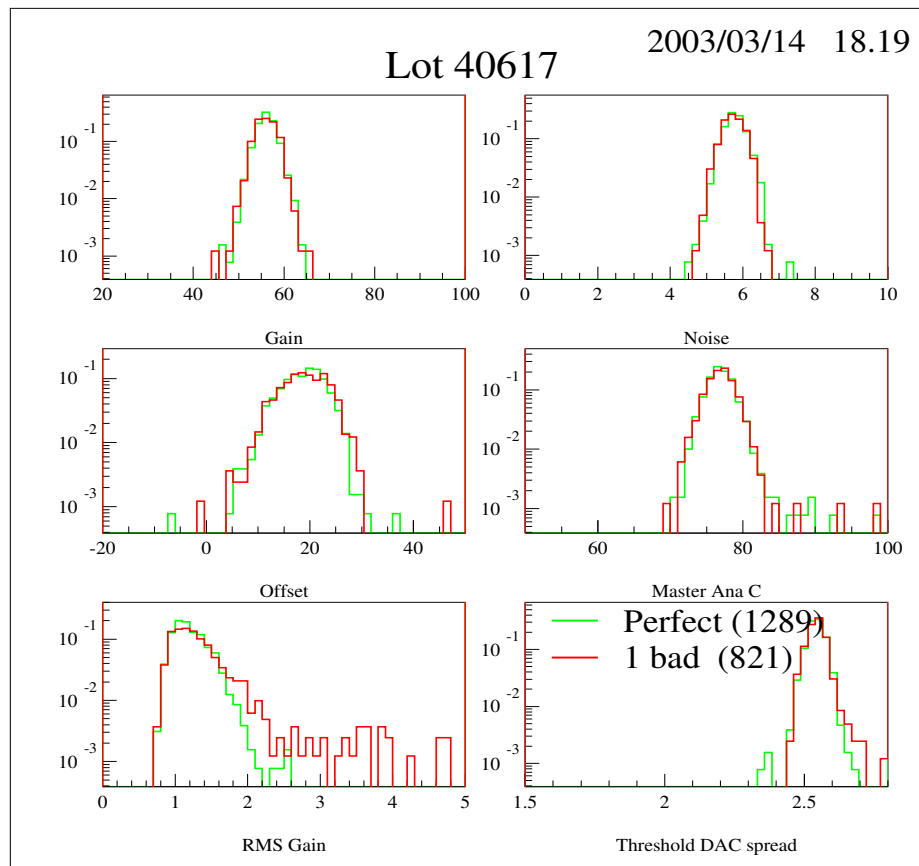
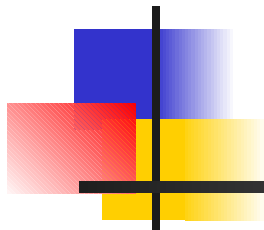


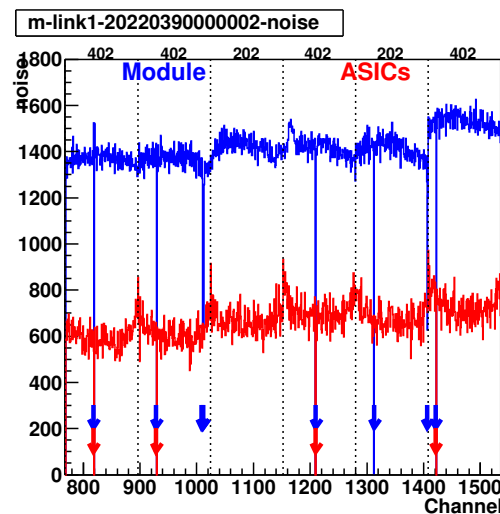
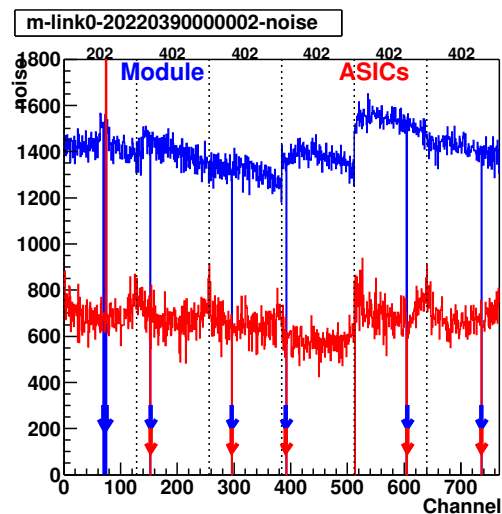
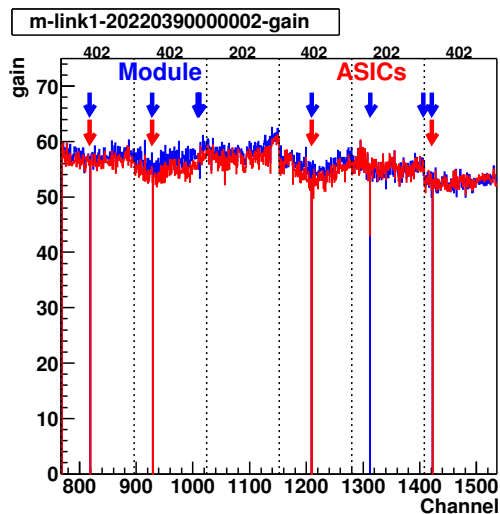
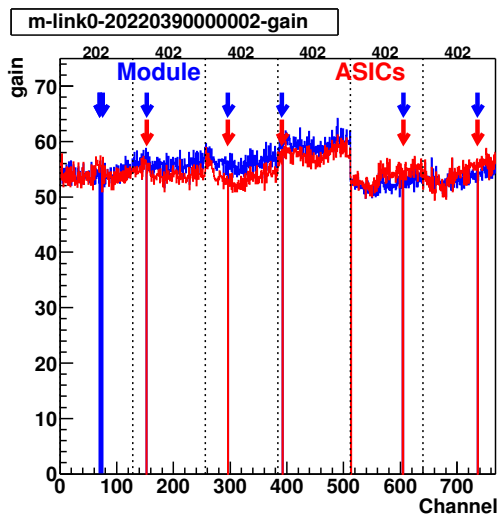
# 1-dead channel chips: Endcap

- Some results presented in June
  - ✓ Chips on the wafer seem to work as perfect...
  - ✓ They have a *bad* channel



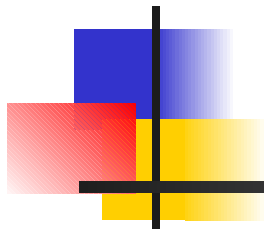


# Performance comparison



- No difference
  - ✓ Same gain
  - ✓ Noise structure
  - ✓ power

chip	Status	digC	anaC	Thrs	Pre.	Shaper
M0	202	0.055	0.074	2.54	2.00	1.32
S1	402	0.039	0.072	2.52	2.00	1.27
S2	402	0.039	0.072	2.52	2.00	1.29
S3	402	0.039	0.075	2.54	2.00	1.33
S4	402	0.039	0.073	2.52	2.00	1.27
E5	402	0.039	0.074	2.53	2.00	1.27
M8	402	0.056	0.073	2.55	2.00	1.33
S9	402	0.039	0.071	2.53	2.00	1.29
S10	202	0.039	0.074	2.50	2.00	1.29
S11	402	0.038	0.073	2.49	2.00	1.28
S12	202	0.039	0.075	2.52	2.00	1.30
E13	402	0.038	0.074	2.53	2.00	1.29
<hr/>						
Total	curr.	0.497	0.879			
Chips	PC	2.398	3.076	-> 5.475		
Module	PC	2.360	3.515	-> 5.875		

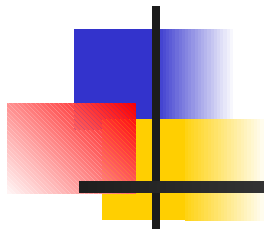


# More 1-dead channel

```
#### Module 20220130000001
chip Status digC anaC Thrs Pre. Shaper
-----
M0      402 0.058 0.078 2.53 2.00 1.44
S1     200002 0.038 0.076 2.51 2.00 1.38
S2      202 0.039 0.078 2.57 2.00 1.46
S3      402 0.039 0.076 2.56 2.00 1.39
S4      402 0.039 0.075 2.52 2.00 1.34
E5     200002 0.038 0.077 2.47 2.00 1.38
M8      402 0.058 0.079 2.53 2.00 1.45
S9      202 0.039 0.077 2.52 2.00 1.41
S10    200002 0.039 0.077 2.50 2.00 1.37
S11     402 0.039 0.078 2.51 2.00 1.44
S12     202 0.039 0.076 2.53 2.00 1.39
E13     402 0.039 0.077 2.56 2.00 1.39
-----
Total curr. 0.505 0.923
Chips PC    2.431 3.229 -> 5.660
Module PC   2.280 3.395 -> 5.675
```

```
#### Module 20220130000002
chip Status digC anaC Thrs Pre. Shaper
-----
M0     200202 0.056 0.078 2.55 2.00 1.39
S1      402 0.039 0.076 2.60 2.00 1.36
S2    30004a2 0.040 0.076 2.55 2.00 1.40
S3      402 0.039 0.078 2.48 2.00 1.37
S4      402 0.039 0.079 2.48 2.00 1.44
E5     200202 0.039 0.076 2.54 2.00 1.37
M8      402 0.054 0.072 2.53 2.00 1.39
S9      402 0.039 0.078 2.54 2.00 1.41
S10    200002 0.039 0.076 2.58 2.00 1.43
S11     402 0.038 0.075 2.50 2.00 1.42
S12     402 0.039 0.077 2.52 2.00 1.42
E13    200002 0.038 0.076 2.55 2.00 1.42
-----
Total curr. 0.499 0.917
Chips PC    2.406 3.211 -> 5.617
Module PC   2.280 3.341 -> 5.621
```

```
#### Module 20220130000004
chip Status digC anaC Thrs Pre. Shaper
-----
M0      402 0.058 0.075 2.47 2.00 1.32
S1      402 0.040 0.072 2.50 2.00 1.27
S2      402 0.040 0.076 2.50 2.00 1.27
S3      402 0.039 0.074 2.53 2.00 1.27
S4     200002 0.040 0.075 2.50 2.00 1.31
E5      402 0.040 0.074 2.48 2.00 1.30
M8      202 0.060 0.077 2.50 2.00 1.31
S9      402 0.040 0.075 2.51 2.00 1.27
S10    200002 0.040 0.075 2.49 2.00 1.28
S11     402 0.040 0.074 2.49 2.00 1.28
S12     202 0.040 0.075 2.53 2.00 1.29
E13     402 0.040 0.074 2.53 2.00 1.28
-----
Total curr. 0.517 0.896
Chips PC    2.479 3.137 -> 5.615
Module PC   2.280 3.535 -> 5.815
```



# Perfect

```
#### Module 20220130000008
chip Status digC anaC Thrs Pre. Shaper
-----
M0      2 0.057 0.075 2.54 2.00 1.34
S1      2 0.039 0.075 2.58 2.00 1.32
S2      2 0.039 0.077 2.54 2.00 1.33
S3      2 0.039 0.076 2.53 2.00 1.33
S4      2 0.037 0.076 2.58 2.00 1.37
E5      2 0.038 0.075 2.56 2.00 1.35
M8      2 0.057 0.076 2.55 2.00 1.35
S9      2 0.037 0.076 2.54 2.00 1.39
S10     2 0.039 0.077 2.53 2.00 1.36
S11     2 0.039 0.076 2.54 2.00 1.32
S12     2 0.038 0.077 2.57 2.00 1.34
E13     2 0.038 0.071 2.56 2.00 1.40
-----
Total curr. 0.495 0.907
Chips PC   2.392 3.175 -> 5.566
Module PC  2.308 3.465 -> 5.773
```

```
#### Module 20220130000009
chip Status digC anaC Thrs Pre. Shaper
-----
M0      2 0.058 0.074 2.50 2.00 1.37
S1      2 0.041 0.074 2.49 2.00 1.35
S2      2 0.039 0.074 2.52 2.00 1.37
S3      2 0.039 0.075 2.53 2.00 1.38
S4      2 0.039 0.076 2.50 2.00 1.40
E5      2 0.039 0.073 2.50 2.00 1.40
M8      2 0.058 0.079 2.49 2.00 1.36
S9      2 0.039 0.079 2.48 2.00 1.40
S10     2 0.040 0.073 2.49 2.00 1.39
S11     2 0.040 0.076 2.47 2.00 1.36
S12     2 0.040 0.079 2.50 2.00 1.36
E13     2 0.039 0.075 2.50 2.00 1.39
-----
Total curr. 0.509 0.907
Chips PC   2.446 3.176 -> 5.622
Module PC  2.400 3.445 -> 5.845
```

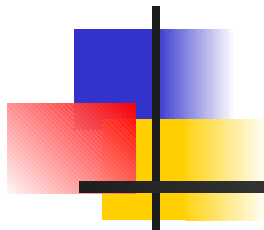
```
#### Module 20220130000010
chip Status digC anaC Thrs Pre. Shaper
-----
M0      2 0.060 0.075 2.52 2.00 1.41
S1      2 0.039 0.080 2.48 2.00 1.41
S2      2 0.037 0.074 2.49 2.00 1.35
S3      2 0.039 0.078 2.50 2.00 1.33
S4      2 0.038 0.076 2.53 2.00 1.33
E5      2 0.038 0.078 2.52 2.00 1.45
M8      2 0.054 0.075 2.52 2.00 1.36
S9      2 0.038 0.077 2.49 2.00 1.33
S10     2 0.038 0.078 2.51 2.00 1.35
S11     2 0.039 0.076 2.55 2.00 1.32
S12     2 0.039 0.081 2.53 2.00 1.35
E13     2 0.039 0.077 2.53 2.00 1.32
-----
Total curr. 0.497 0.925
Chips PC   2.397 3.236 -> 5.633
Module PC  2.440 3.500 -> 5.940
```



# Defect Matching

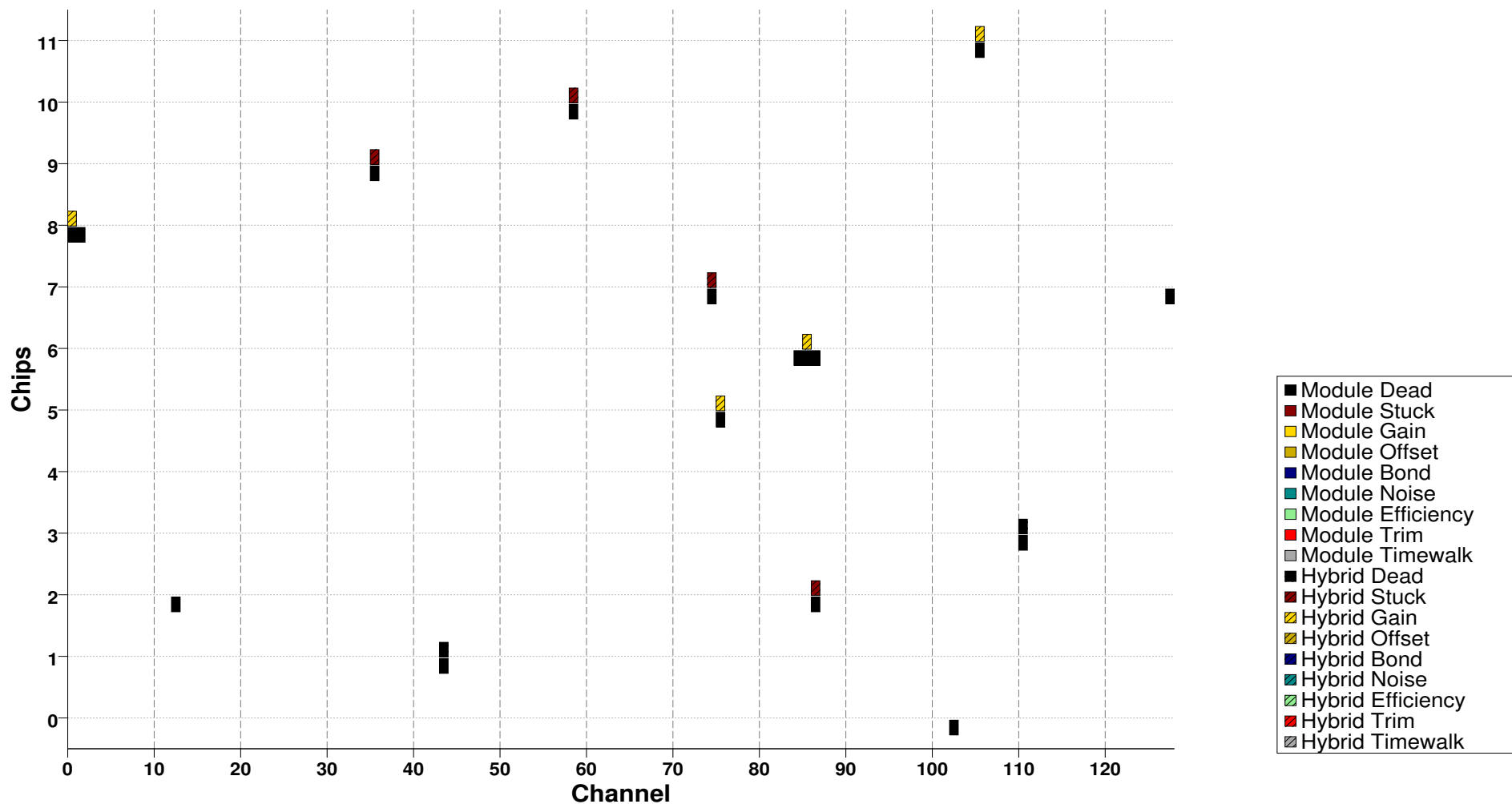
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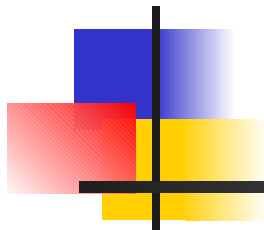
- The main worries:
  - ✓ Will the defective channels develop additional defects ?
- Comparison of defective channels at hybrid and module level
  - ✓ Difficult since
    - ✧ Different measurement conditions
    - ✧ Skills improve with time and it is not easy to distinguish between operator and dead channels as a source of new defects
  - ✓ However, it is worth trying and one observes interesting things
- Statistics:
  - ✓ 32 modules,
  - ✓ 269 1-dead channel chips



# Module 20220130000007

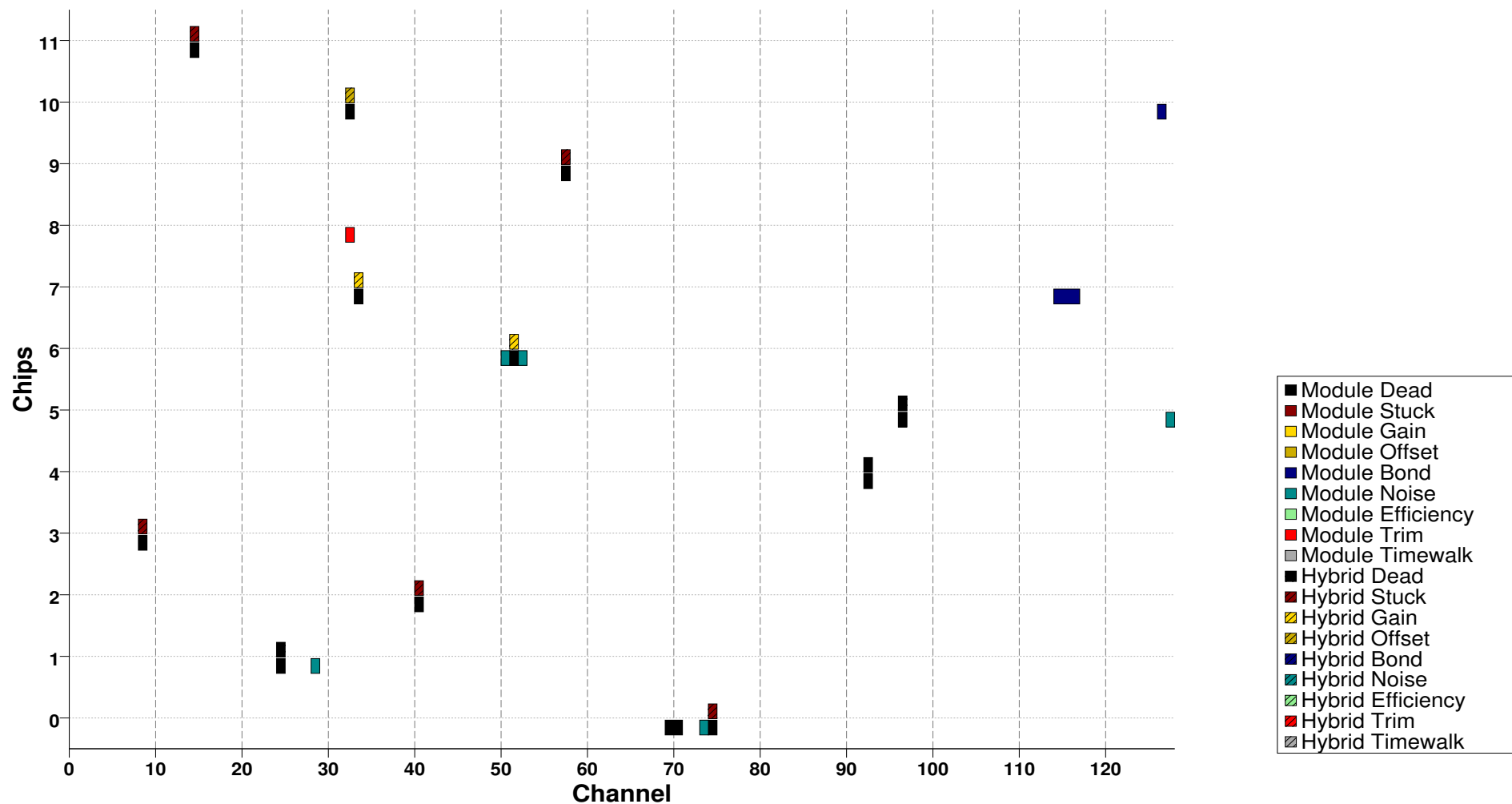
Module 20220130000007

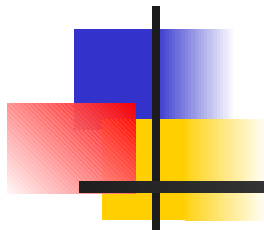




# Module 20220390000002

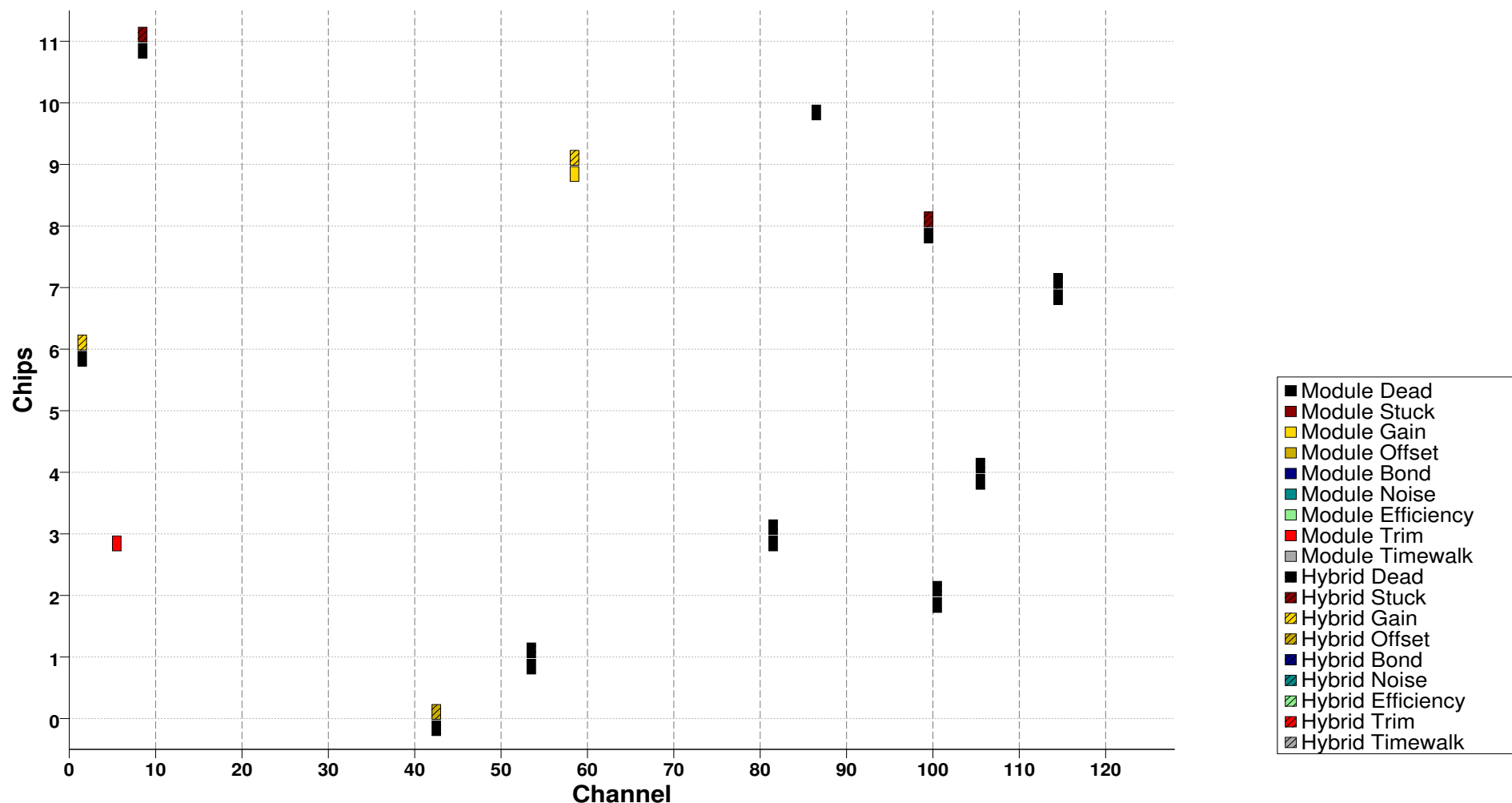
Module 20220390000002



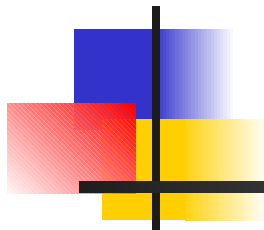


# Module 20220240100030

Module 20220240100030

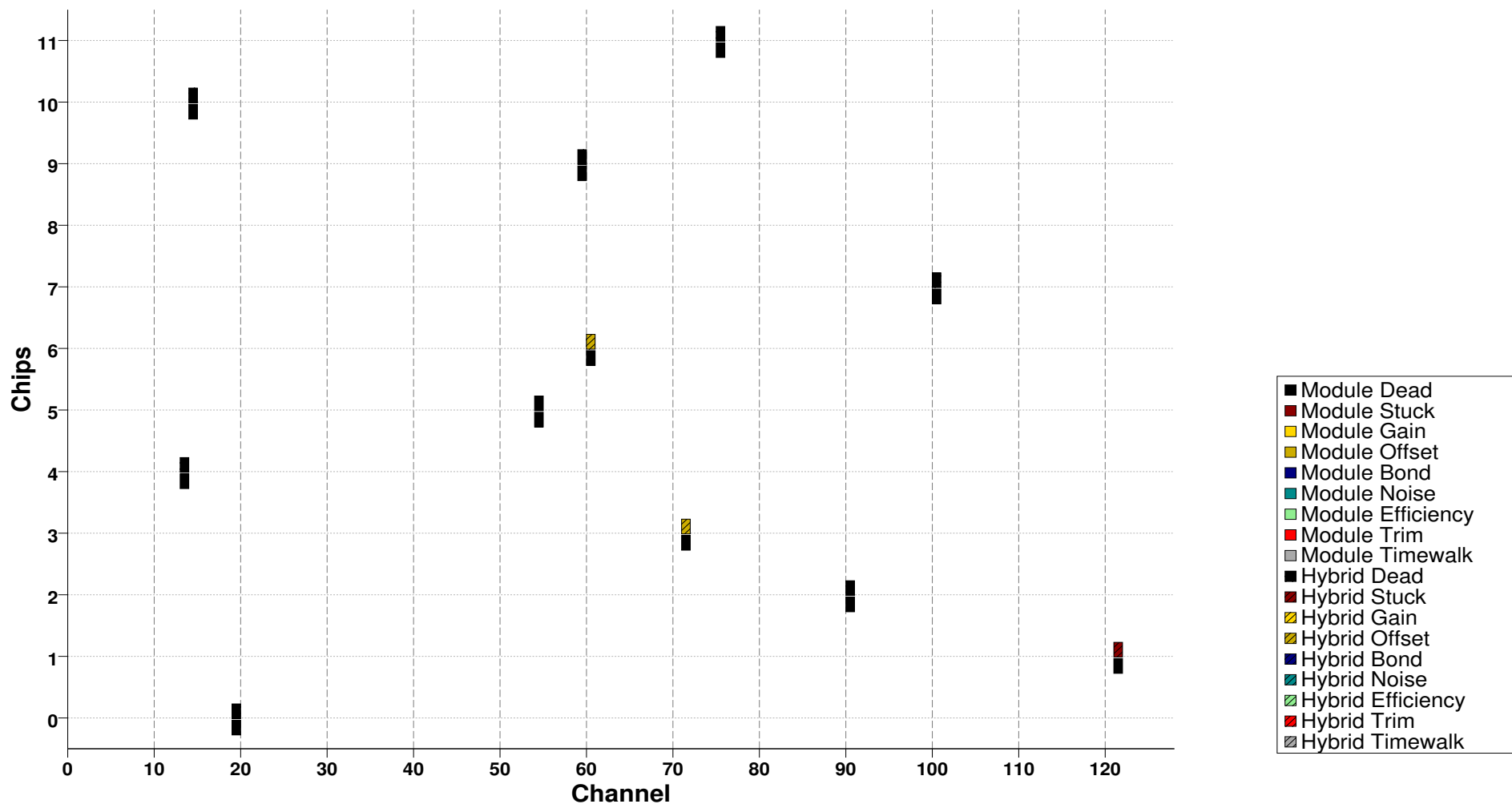


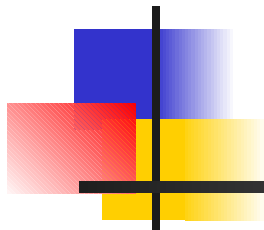




# Module 20220240100034

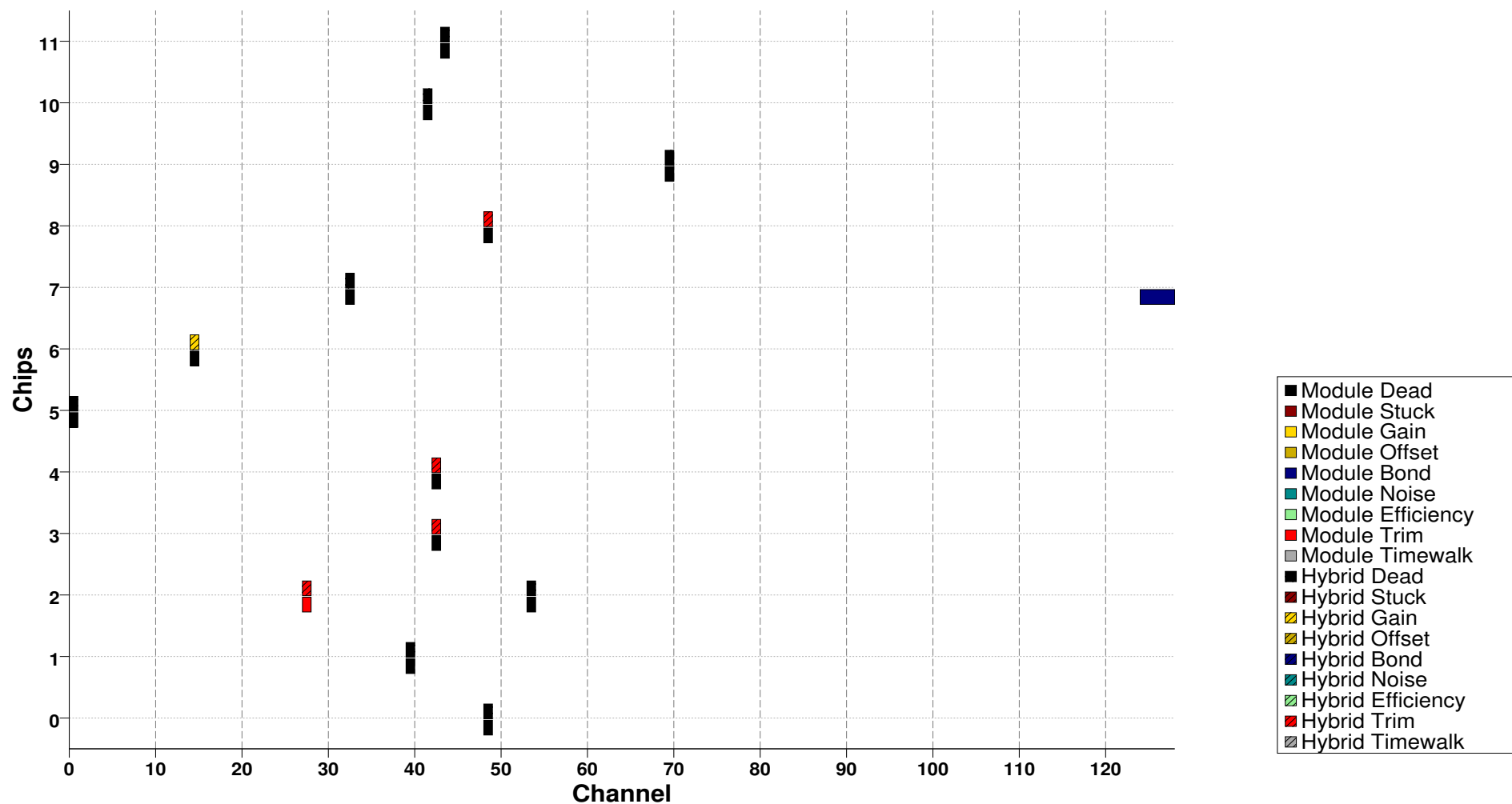
Module 20220240100034





# Module 20220281001001

Module 20220281001001





# Conclusions

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- 4 modules show clusters developing around a *dead* channel.
  - ✓ A total of 6 of those clusters found ~2.2% of 1-dead channel chips
  - ✓ The modules are *old* ones from pre-qualification.
- No difference observed in performance